GENERAL DESCRIPTION

NOTES

GENERAL DESCRIPTION

The Vadem VG230 is a one-chip PC platform which provides a highly battery-efficient basis for OEMs to develop cost sensitive, DOS-based personal electronic products. The chip contains all standard XT peripherals, additional high-value peripherals and an ISA bus. For long battery life, the VG230 offers extensive and proven power management capability. In addition to a +5V version, a version is offered which operates at +3V.

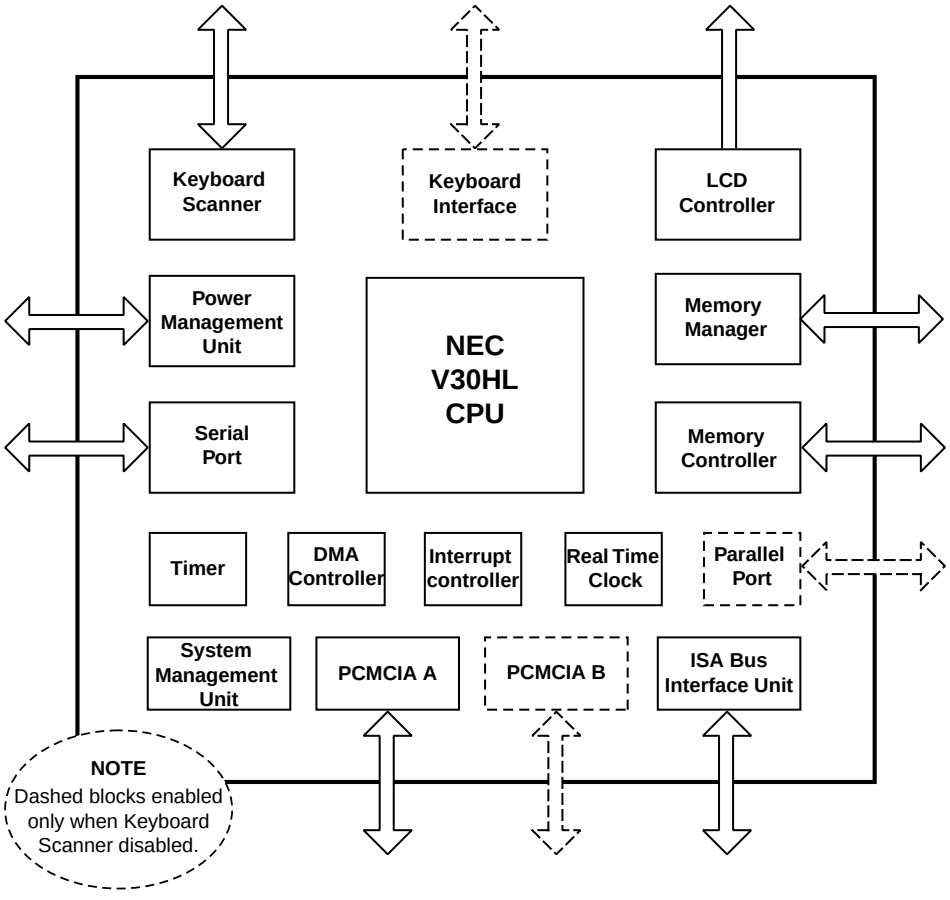
The VG230 contains the 8086-compatible 16 MHz NEC V30HL processor. It also embodies a standard XT architecture combined with hardware and software features facilitating the rapid design of products with extensive ROM-based software. PC Card mass storage and miniature peripherals (I/O cards) following the PCMCIA 2.1 (JEIDA 4.1) standard are supported. The VG230 is packaged in a single 160-pin CMOS chip and handles all PC functions including 16-bit CPU, XT core logic, LCD controller, keyboard scanner and PC Card controller. All that is required for a basic system is the VG230, memory, power supply, display and associated packaging.

PRODUCT OVERVIEW

- Single-chip permits glueless implementation of a fully compatible PC-XT.
- Standard-design 16-bit, 16 MHz NEC V30HL processor core integrated on-chip.
- Complete hardware and firmware support for memory-saving “execute-in-place” ROM applications.
- Field-proven, industry standard power management based on activity monitoring lengthens battery life.
- Scans up to 101 keys without an external keyboard controller.
- Integrated CGA LCD controller and 640x400 AT&T standard controller. Supports a wide variety of panel resolutions from below CGA to 400-line displays.
- LCD controller supports hardware “ink plane” for pen-based applications.
- Dual PCMCIA 2.1 (JEIDA 4.1) PC Card slot support allowing “hot” insertion/removal (with external buffers).
- Integrated serial port, real-time clock, programmable interrupt controller, DMA controller and internal timer.
- Deactivating keyboard scan enables a second PCMCIA card slot, a bi-directional parallel. port and a standard XT keyboard interface.
- Support for DRAM, SRAM and PSRAM memory.
- Supports up to eight 8-bit RAM banks and up to six 16-bit RAM banks.
- ICE support simplifies debugging of system designs.
- 8250 compatible UART.
- XT keyboard interface.

- EMS 4.0 compatible memory subsystem, supports up to 64Mbytes.
- Real Time Clock with CMOS RAM
- Vadem Power Management Unit (PMU)
- Optionally combines with external VG-660 single-chip LCD VGA controller to drive 640x480 and lower resolution VGA compatible LCD panels.

VG230 BLOCK DIAGRAM

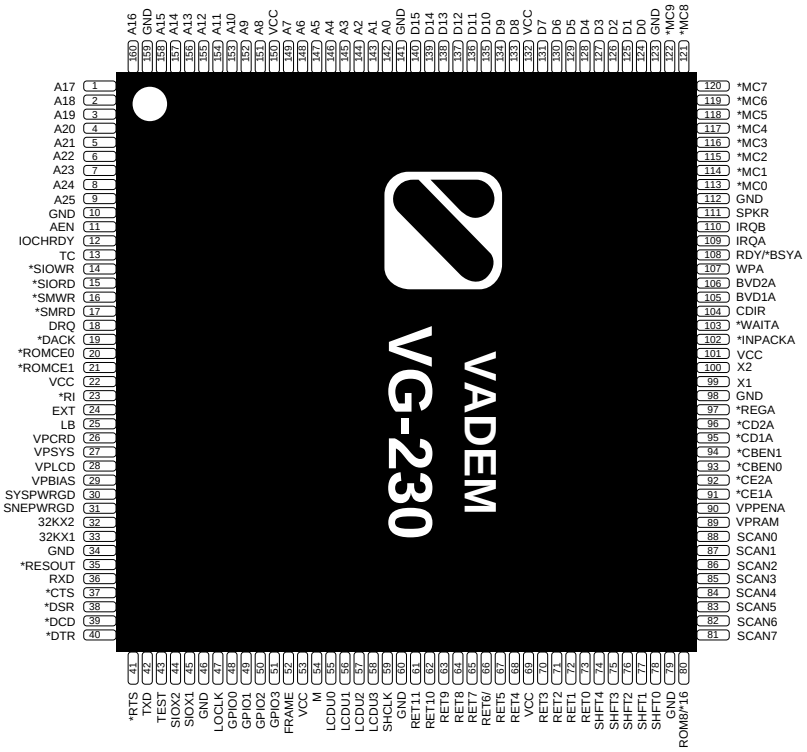


CONNECTION AND PIN DESCRIPTIONS

NOTES

VG230 PIN ASSIGNMENT

D E F A U L T P I N A S S I G N M E N T



A L T E R N A T I V E P I N D E F I N I T I O N S

PIN #	DEFAULT	ALTERNATIVE(S)
48	GPIO0	LCDL0, *DACK0
49	GPIO1	LCDL1, ALE
50	GPIO2	LCDL2, SYSCLK
51	GPIO3	LCDL3
54	M	*DACK0
61	RET11	PDOE
62	RET10	VPPENB
63	RET9	AFD
64	RET8	SLCT
65	RET7	*ERR
66	RET6	SEL
67	RET5	PE
68	RET4	ACK
70	RET3	BUSY
71	RET2	*RDY/BSYB, IREQB
72	RET1	WPB
73	RET0	*WAITB

PIN #	DEFAULT	ALTERNATIVE(S)
74	SHFT4	*CD1B
75	SHFT3	*CD2B
76	SHFT2	BVD1B, *STSCHGB
77	SHFT1	BVD2B, *SPKRB
78	SHFT0	*INPACKB
81	SCAN7	KBCLK
82	SCAN6	KBDAT, IRQ1
83	SCAN5	*CE1B
84	SCAN4	*CE2B
85	SCAN3	*REGB
86	SCAN2	PDCLKU, PDCLKB
87	SCAN1	INIT
88	SCAN0	STB
105	BVD1A	STSCHGA
106	BVD2A	*SPKRA
107	WPA	*IOIS16A
108	RDY/*BSYA	*IREQA

NOTE: The VG-230 does not contain pull-up/pull-down resistors.
All unused inputs should be terminated.

PIN DESCRIPTIONS

The VG 230 Pin Descriptions Table contains the VG230 pin definitions in alphabetical order by pin name. Pins which have alternative functions are listed under each function's symbol. Alternative functions are enabled and disabled by setting various VG230 registers. These are:

- Keyboard Mode Register (08H)
- GPIO Mode Register (32H)
- PC Card Slot 0 Control Register (21H)
- PC Card Slot 1 Control Register (27H)
- LCD Configuration Control Register (07H)
- PIO Mode Register (18H)

VG230 Pin Descriptions Table

Symbol	Type	Pin Number	Description
32KX[2:1]	XTL	32,33	32.768 KHz crystal connection.
A[25:0]	O	9-1, 158-151, 149-142	System Address Bus. All external memory and I/O devices attach to this common address bus. The function of this bus is dynamically set according to the device type addressed: DRAM, SRAM, PC Card, ROM, I/O, or Expansion memory.
*ACK	I	68	Parallel port *ACK input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET4.
AEN	O	11	Address Enable. Output from 8237A DMA Controller Macro.
AFD	O	63	Parallel port AFD control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). AFD must be inverted using a 74XX05-type open collector device. The default definition of this pin is RET9.
ALE	O	49	Address Latch Enable signal (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL1 for 400-line LCD panels may be enabled using this register. The default definition of this pin is GPIO1.

Symbol	Type	Pin Number	Description
BUSY	I	70	Parallel port BUSY input (when the keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET3.
BVD[2:1]A	I	106,105	Battery voltage status inputs for slot 'A' PC memory cards. May be re-defined for I/O cards to *SPKRA and STSCHGA respectively by the PC Card Slot 0 Control Register (21H).
BVD[2:1]B	I	77,76	Battery voltage status inputs for slot 'B' PC memory cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). Pins [2:1] may be set to *SPKRB and STSCHGB respectively for I/O cards by using the PC Card Slot 1 Control Register (27H). The default definitions of these pins are SHFT[1:2] respectively.
*CBEN[1:0]	O	94,93	Enable signal for PC Card Odd and Even Byte data buffers.
CDIR	O	104	Direction control for PC Card Odd and Even Byte data buffers.
*CD[2:1]A	I	96,95	Card detect status inputs from slot 'A' PC Card.
*CD[2:1]B	I	75,74	Card detect status inputs from slot 'B' PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definitions of these pins are SHFT[3:4] respectively.
*CE[2:1]A	O	92,91	PC Card Even/Odd byte chip select signals for slot 'A.'
*CE[2:1]B	O	84,83	PC Card Even/Odd byte chip select signals for slot 'B' (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definitions of these pins are SCAN[4:5] respectively.
*CTS	I	37	Serial Port clear to send.

Symbol	Type	Pin Number	Description
D[15:0]	I/O	140-133, 131-124	Bi-directional System Data Bus. All external memory and I/O devices attach to this common data bus. 8 bit devices will reside on the D[7:0] half of the system data bus.
*DACK	O	19	DMA Acknowledge. Output from 8237A DMA Controller Macro. Selected from one of *DACK[3:1] depending upon which of DRQ[3:1] is programmed by user.
*DACK0	O	48	Internal *DACK0 signal REFRESH (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL0 for 400-line LCD panels may be enabled by this register. The default definition of this pin is GPIO0.
*DACK0	O	54	Internal *DACK0 signal REFRESH (when LCD controller disabled by LCD Configuration Control Register, 07H). The default definition of this pin is M.
*DCD	I	39	Serial Port data carrier detect.
DRQ	I	18	DMA Request. Input to 8237A DMA Controller Macro. User programmable to be one of DRQ[3:1].
*DSR	I	38	Serial Port data set ready.
*DTR	O	40	Serial Port data transmit ready.
*ERR	I	65	Parallel port *ERR input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET7.
EXT	I	24	External switch input. To activate SUSPEND/RESUME.
FRAME	O	52	Frame clock to LCD.

Symbol	Type	Pin Number	Description
GPIO{3:0]	I/O	51-48	General Purpose Input/Output signals. Data direction is set by the GPIO Mode Register (32H). This register also enables other definitions for these pins. See LCDL, SYSCLK, ALE and *DACK0 for further information.
INIT	O	87	Parallel port INIT control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). This output must be inverted using a 74XX05 type open collector device. The default definition of this pin is SCAN1.
*INPACKA	I	102	Input acknowledge from slot 'A' PC I/O cards.
*INPACKB	I	78	Input acknowledge from slot 'B' PC I/O Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SHFT0.
IOCHRDY	I	12	I/O Channel Ready. Input OR'ed with internal ready sources to insert CPU wait states.
*IOIS16A	I	107	Register width status from slot 'A' PC I/O Cards. Enabled by the PC Card Slot 0 Control Register. The default definition of this pin is WPA.
*IOIS16B	I	72	Register width status from slot 'B' PC I/O Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H and I/O mode enabled using PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is WPB. When the scanner is enabled, the definition of this pin is RET1.
IRQ1	I/O	82	Interrupt signal from external keyboard controller (when reads from VG230 keyboard registers disabled by Keyboard Mode Register, 08H). When reads are enabled, pin definitions SCAN6 (default) or KBDAT may be set by the Keyboard Mode Register.

Symbol	Type	Pin Number	Description
IRQA, IRQB	I	109,110	System interrupt request. Interrupt request inputs to internal 8259A Macro. User programmable to be one of IRQ[7:2].
KBCLK	I/O	81	External keyboard KBCLK input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN7.
KBDAT	I/O	82	External keyboard KBDAT input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN6.
LB	I	25	Low Battery warning input.
LCDL[3:0]	O	51-48	Display data for lower half of 400 line LCDs (when enabled by GPIO Mode Register, 32H). This register may also be used to select other definitions for these pins. See LCDL, SYSCLK, ALE, *DACK0 and GPIO (default) for further information.
LCDU[3:0]	O	58-55	Display data for 200-line LCDs or for the upper half of 400 line LCDs.
LOCLK	O	47	Load clock to LCD.
M	O	54	Low frequency clock to LCD. When the LCD controller is disabled by the LCD Configuration Control Register (07H), this pin becomes *DACK0.
*MC[9:0]	O	122-113	System RAM control. Outputs defined in Table 1-2.
*PDCLKB	O	86	Active low bidirectional parallel port data clock (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). Asserted during accesses to the Parallel Port Data Register. *PDCLKB must be qualified externally with *SIOWR using a 74XX32 ‘R’ gate to write data and with PDOE to control a 74XX244 to read data. The default definition of this pin is SCAN2.

Symbol	Type	Pin Number	Description
PDCLKU	O	86	Unidirectional parallel port data clock (when keyboard scanner disabled by Keyboard Mode Register, 08H). Internally qualified with *SIOWR to drive directly the CLK pin of an external 74XX374 octal D F/F for latching printer data. When the PIO Mode Register (18H) enables bidirectional operation, this pin becomes *PDCLKB. The default definition of this pin is SCAN2.
PDOE	O	61	Parallel Port Output Enable (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). The default definition of this pin is RET11.
PE	I	67	Parallel port PE input (when keyboard scanner disabled by Keyboard Mode Register, 08H and bidirectional operation enabled by PIO Mode Register, 18H). The default definition of this pin is RET5.
RDY/*BSYA	I	108	Ready/*Busy status input from slot ‘A’ PC memory cards. PC Card Slot 0 Control Register (21H) may be used to redefine this pin as *IREQA for I/O cards.
RDY/*BSYB	I	71	Ready/*Busy status input from slot ‘B’ PC Memory Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). PC Card Slot 1 Control Register (27H) may be used to redefine this pin as *IREQB for I/O cards. The default definition of this pin is RET2.
*REGA	O	97	PC Card register select signal for slot ‘A.’
*REGB	O	85	PC Card register select signal for slot ‘B’ (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN3.
*RESOUT	O	35	Active low system RESET output.

Symbol	Type	Pin Number	Description
RET[11:0]	I	61-68, 70-73	Return inputs from external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See PDOE, VPPENB, AFD, SLCT, *ERR, SEL, PE, *ACK, BUSY, RDY/*BSYB, *IREQB, WPB, *IOIS16B and *WAITB for more information.
*RI	I	23	Serial Port ring indicator.
ROM8/*16	I	80	Strap pin option. Allowing selection of BIOS ROM width. When strapped low, BIOS ROM is 16 bits wide.
*ROMCE[1:0]	O	21,20	ROM chip enable outputs. *ROMCE0 is always asserted for memory accesses to the BIOS ROM (address range F000:0-FFFF:F). Assertion of ROM chip enable outputs [1:0] for other address ranges may be specified using the VG230's EMS addressing.
*RTS	O	41	Serial Port request to send.
RXD	I	36	Serial Port receive data.
SCAN[7:0]	I/O	81-88	Scan outputs for external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See KBCLK, KBDAT, *CE[2:1]B, *REGB, PDCLKB, *PDCLKU, INIT and STB for more information.
SEL	I	66	Parallel port SEL input (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET6.
SHCLK	O	59	Shift clock to LCD.
SHFT[4:0]	I/O	74-78	Shift key return inputs from external key matrix. The Keyboard Mode Register (08H) also enables other definitions for these pins. See *CD[2:1]B, BVD[2:1]B, *STSCHGB, *SPKRB and *INPACKB for more information.

Symbol	Type	Pin Number	Description
*SIORD	O	15	System I/O Read strobe. This output is used to inform external I/O devices to put their data onto the data bus. The VG230 may be programmed to inhibit this output during I/O read cycles to the VG230 internal devices.
*SIOWR	O	14	System I/O Write strobe. This output is used to inform external I/O devices that data is available on the data bus. The VG230 may be programmed to inhibit this output during I/O write cycles to the VG230 internal devices.
SIOX[2:1]	XTL	44,45	Serial Port crystal input/output.
SLCT	O	64	Parallel port SLCT control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). This output must be inverted using a 74XX05-type open collector device. The default definition of this pin is RET8.
*SMRD	O	17	System Memory Read strobe. This output is used to inform external memory devices to put their data on the data bus. *SMRD is not asserted during reads from system RAM, ROM, or PC Cards.
*SMWR	O	16	System Memory Write strobe. This output is used to inform expansion memory devices that data is available on the data bus. *SMWR is not asserted during writes to system RAM, ROM, or PC Cards.
SNEPWRGD	I	31	VG230 power good input. This pin should be driven low when power to the VG230 falls below the recommended operating thresholds. SNEPWRGD is used to initialize the internal registers, peripherals, RTC, and microprocessor of the VG230. It will also generate a system reset on the *RESOUT output.
SPKR	O	111	Speaker data output. This output should be buffered and then input to a low pass filter. The output of the filter connects to a speaker.

Symbol	Type	Pin Number	Description
*SPKRA	I	106	Speaker signal from slot 'A' PC I/O cards. Enabled by the PC Card Slot 0 Control Register (21H). The default definition of this pin is BVD2A.
*SPKRB	I	77	Speaker signal from slot 'B' PC I/O cards (when keyboard scanner disabled by Keyboard Mode Register, 08H, and I/O mode enabled by PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is BVD2B. When the scanner is enabled, the definition of this pin is SHFT1.
STB	O	88	Parallel port STB control output (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is SCAN0.
*STSCHGA	I	105	Status changed signal from slot 'A' PC I/O cards. Enabled by the PC Card Slot 0 Control Register (21H). The default definition of this pin is BVD1A.
*STSCHGB	I	76	Status changed signal from slot 'B' PC I/O cards (when keyboard scanner disabled by Keyboard Mode Register, 08H, and I/O mode enabled using PC Card Slot 1 Control Register, 27H). When the keyboard scanner is disabled, the default definition of this pin is BVD1B. When the scanner is enabled, the definition of this pin is SHFT2.
SYSCLK	O	50	XT Bus Clock signal (when enabled by GPIO Mode Register, 32H). Alternatively, LCDL2 for 400-line LCD panels may be enabled by this register. The default definition of this pin is GPIO2.
SYSPWRGD	I	30	System Power Good input. This pin should be driven low when the system VCC falls below the recommended operating thresholds. SYSPWRGD is used to initialize the external system peripherals, via the *RESOUT signal, and re-start the internal VG230 clocks.

Symbol	Type	Pin Number	Description
TC	O	13	Terminal Count. Output from 8237A DMA Controller Macro.
TEST	I	43	Test Mode.
TXD	O	42	Serial Port transmit data.
VPBIAS	O	29	BIAS power gate for LCD panel.
VPCRD	O	26	VCC power gate for PC Cards.
VPLCD	O	28	VCC power gate for LCD panel.
VPPENA	O	90	Program Voltage Enable for slot ‘A’ PC Card.
VPPENB	O	62	Program Voltage Enable output to power source for slot ‘B’ PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET10.
VPRAM	O	89	VCC power gate for RAM array.
VPSYS	O	27	Main System power gate for system power supply.
*WAITA	I	103	Extend bus cycle for slot ‘A’ PC Cards.
*WAITB	I	73	Wait status input from slot ‘B’ PC Card (when keyboard scanner disabled by Keyboard Mode Register, 08H). The default definition of this pin is RET0.
WPA	I	107	Write protect input from slot ‘A’ PC memory cards. PC Card Slot 0 Control Register (21H) may be used to redefine this pin as *IOIS16A for I/O cards.

Symbol	Type	Pin Number	Description
WPB	I	72	Write protect status input from slot 'B' PC memory Cards (when keyboard scanner disabled by Keyboard Mode Register, 08H). PC Card Slot 1 Control Register (27H) may be used to redefine this pin as *IOIS16B for I/O cards. The default definition of this pin is RET1.
X[2:1]	XTL	100,99	Main clock crystal inputs. X1 is an input for a passive crystal circuit. X1 may be driven at either 32.215905 MHz or 28.63636 MHz. X2 is the inverted output of X1.

FUNCTIONAL DESCRIPTION

NOTES

OVERVIEW

This section describes the main functional blocks of the VG230 Single-Chip PC Platform. The VG230 is designed for easy development of cost-sensitive, battery operated products which contain substantial amounts of ROM-based software. In addition to the functional blocks which support basic XT compatibility, also provided are a matrix keyboard scanner, a CGA/AT&T LCD controller, a sophisticated memory manager which is programmed using a compatible superset of LIM 4.0 registers, PCMCIA 2.1 controllers, an industry-proven power management unit, a system management unit to aid in integration of non-standard peripherals, a serial port and a parallel port. Standard V30H ICE support for faster debugging is also integrated.

SINGLE-BUS ARCHITECTURE

The VG230 Single-Chip PC Platform embodies a Single Bus Architecture (pat. pend.). All external memory and I/O devices share the same address bus and data bus. A control bus is reserved for interfacing Expansion Memory and Expansion I/O devices. Expansion in this case means memory or I/O devices not directly controlled by the VG230 Single-Chip PC Platform. The single bus architecture minimizes cost and power requirements while still providing high performance. The single bus architecture minimizes cost and power requirements while significantly boosting video performance.

The Address Bus operates in 5 modes depending upon the device type accessed. Logic internal to the VG230 Single-Chip PC Platform enables the appropriate addressing mechanism for the selected device. The addressing modes are in the VG230 Addressing Modes Table.

The Single Bus supports 8 or 16 bit memory, 8 bit I/O, 16 bit PC memory cards and 8 or 16 bit PC I/O cards. The data width of System RAM and System ROM are set by VG230 Single-Chip PC Platform register bits and a configuration pin. When 8-bit system RAM or 8-bit system ROM configurations are selected, these devices are installed on the lower half of the data bus, D[7:0].

VG230 Addressing Modes Table

Device Type	Address Format	Address Type
System RAM DRAM SRAM/PSRAM	 Multiplexed Row/Column Latched	 Mappable RAM Memory Address Mappable RAM Memory Address
System ROM0	Latched	Mappable ROM0 Memory Address
System ROM1	Latched	Mappable ROM1 Memory Address
PC Memory Card 1	Latched	Mappable PC Card 1 Memory Address
PC Memory Card 2	Latched	Mappable PC Card 2 Memory Address

PROCESSOR

The VG230 Single-Chip PC Platform is built around a standard, fully 8086-compatible NEC V30HL CPU macro. With its maximum clock rate of 16 MHz, the V30HL rivals all industry standard processors in speed. It is especially designed for low power consumption, and supports complete clock stoppage under power management. The V30HL is designed to operate over a range including +3V (reduces maximum clock rate to 8MHz) and +5V.

Basic Peripherals and Core Logic

The VG230 Single-Chip PC Platform contains the following PC Core logic and other peripherals:

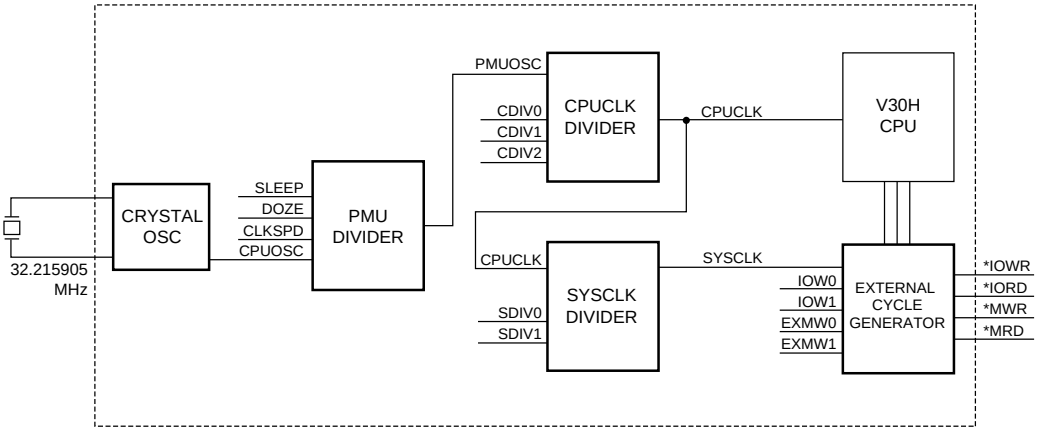
- Serial Port
- Parallel Port
- Real Time Clock (RTC)
- Standard PC Core logic peripherals
- DMA Controller
- Interrupt Controller
- Timer
- Keyboard Interface

Bus Cycle Generator (BCG)

The Bus Cycle Generator (BCG) controls the system timing for all I/O and memory accesses. The BCG can be configured for various memory and I/O wait states through registers located in the VG230's configuration space.

CPUOSC is the frequency of the crystal oscillator connected to the X1 and X2 pins. There are two possible frequencies at which the VG230 can run, 32.215905 MHz and 28.63636 MHz. CPUOSC is routed through the PMU to the CPUCLK divider. The PMU will divide the clock from 1 to 8 times depending on its state and the CLKSPD bit. PMUOSC is divided from 2 to 8 times to create CPUCLK. CPUCLK is used as the timebase for all VG230 controlled RAM and ROM accesses. SYSCLK is generated from CPUCLK and can equal CPUCLK or be divided 2, 3 or 4 times. SYSCLK is used for all I/O cycles and expansion memory cycles. The Clock Distribution Figure illustrates the clock divider circuitry in the VG230.

Clock Distribution Figure



CPUCLK is derived from CPUOSC, and is configured through the BCG mode register at offset 01H. CDIV[2:0] select the divisor for CPUCLK. The default is CPUOSC/4.

CLK14/*16 selects the CPUOSC frequency of 32.21 MHz or 28.63 MHz. This option configures the internal divider chain to provide a PC-compatible 1.19MHz timer clock.

The LTCHADR bit enables address latching for certain cycles. Latching of the address reduces switching on the external address bus. Reduced switching reduces the power consumption.

The BINH bit disables bus cycles for internal I/O accesses. This reduces activity on the external bus, thereby reducing power consumption.

SYSCLK is generated from CPUCLK and can equal CPUCLK or be divided 2, 3 or 4 times. SYSCLK is used for all I/O cycles and expansion memory cycles. The SDIV[1:0] bits control the generation of SYSCLK. Divisors of 1, 2, 3 and 4 are selectable. The default is CPUCLK/2.

The BCG Wait State Control 1 Register selects the number of wait states for the various I/O and memory subsystems. ROMW[1:0] control the number of wait states for ROMs connected to *ROMCE0 and *ROMCE1. RAMW[1:0] control the number of wait states for all RAM. IOW[1:0] control the number of SYSCLK wait states for all I/O cycles. EXMW[1:0] control the number of SYSCLK wait states for all expansion memory cycles. *For Register Description, see Index 02H.*

Clocks

The VG230 Single-Chip PC Platform requires three clock sources:

- Main clock 32.215905 MHz or 28.63636 MHz
- SIO clock 3.6864 MHz
- Power Management Unit/ RTC clock 32.768 KHz

The Main clock generates the processor clock (CPUCLK), the LCD Controller's clock (VIDCLK) and the Timer clock (TCLK). The RTC and PMU share the same time base, which is the only oscillator running when the VG230 Single-Chip PC Platform is in the SUSPEND or OFF Power Management modes.

DMA

The VG230 provides two pins for DMA support. Because of pin limitations, only a single DMA channel is supported. The DMA pins, DRQ and *DACK are configurable for DRQ/*DACK[1:3]. Selection of the desired DMA channel is made through bits DRQS[1:0] in the DMA mode register located at index 0EH.

DMA Controller

An 8237A PC/XT compatible DMA Controller is included. One DMA channel is provided for the external system bus. System software may configure this channel to be one of DRQ/*DACK1, DRQ/*DACK2 or DRQ/*DACK3. Channel 0 (DRQ/*DACK0) of the DMA controller is reserved by the VG230. When setting up refresh, Port 42H of the 8254 timer must be initialized before refresh will begin.

Command Delay and DMA Clock Control

In some applications it may be desirable to delay the *IOWR and *MWR strobes during DMA. These strobes may be delayed from 0 to 3 SYSCLK cycles. Command delay is programmed through WDLY[1:0] in the DMA mode register.

To reduce current consumption, the VG230 has a provision to disable the internal 8237's clock during idle times. When the STPDCLK bit in the DMA mode register is cleared (0), the internal DMA clock always runs. When set, the clock is enabled only during DMA cycles.

General Purpose I/O Pins (GPIO)

The VG230 provides up to 4 GPIO pins when 200 line or smaller LCD panels are used. The LCDL[3:0] pins are only used when 400 line panels are used. When configured for GPIO these pins can provide general purpose input or output bits which can be used to control peripherals or monitor status. Some examples of possible uses include:

- LCD backlight control
- Additional low battery monitoring
- LED indicator control
- Serial EEPROM interface
- FLASH EPROM programming voltage control

The GPIO is enabled through the GPIO mode register at index 32H. Each of the LCDL[3:0] pins can be individually programmed as LCDL bits, GPIO bits or one of the listed internal signals. The default configuration is GPIO configured as input.. Each pin must first be configured for GPIO through the GPIO mode register. Control of the state of the pins is through the GPIO control register at index 33H.

Also, the Parallel Port (available when the VG230's internal keyboard scanner is disabled) may be configured to appear at a non-standard address. This allows use of the port's pins by dedicated applications for general purpose input and general purpose output (GPI and GPO).

Interrupt Controller

The Interrupt Controller is PC/XT compatible and based upon the 8259 PIC. The VG230 provides two external interrupt request inputs, IRQA and IRQB. System software may assign each of these lines to any of IRQ2 through IRQ7 using the ICU Mode Register (0DH).

The remaining interrupt lines are inputs internally assigned as follows:

- IRQ0 System Timer Interrupt
- IRQ1 Keyboard
- IRQ2 RTC Alarm
- IRQ3 SIO programmed to appear at 2F8H-2FFH
- IRQ4 SIO programmed to appear at 3F8H-3FFH
- IRQ7 Parallel Port

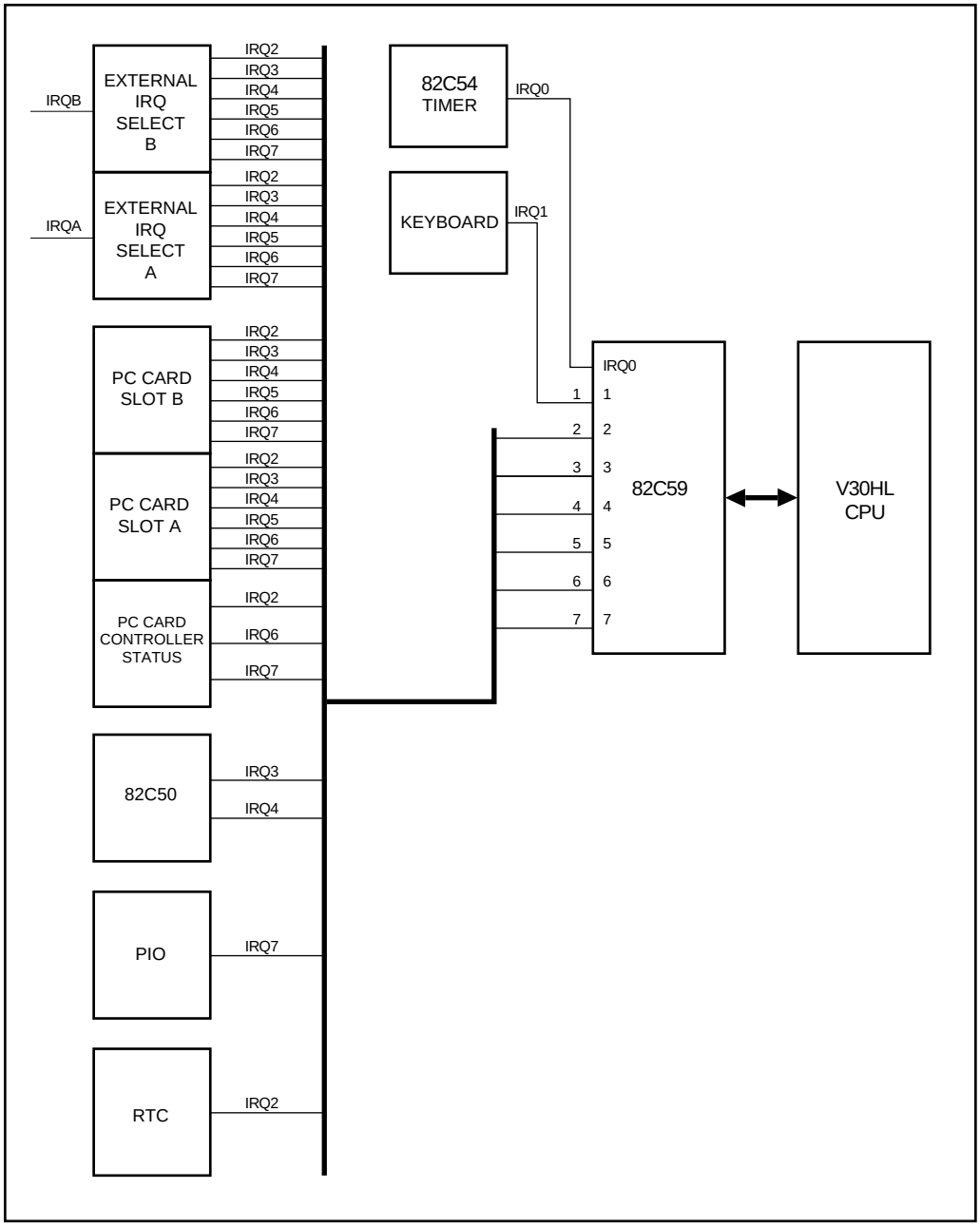
Interrupts

The VG230 has many sources of internal interrupts in addition to two external interrupt sources. The Internal Interrupt Configuration Figure illustrates the sources of the internal and external interrupts. The following table lists the internal interrupts and the control/status register associated with each.

Internal Interrupts and Their Control/Status Registers Table

Source	Levels (IRQ)	Control	Status
Internal COM1	4	3F9	3FA
Internal COM2	3	2F9	2FA
Parallel Port	7	37A	379
82C54 Timer	0	20,21H	20H
Keyboard	1	20,21H	20H
IRQA	2-7	Index 0DH	20H
IRQB	2-7	Index 0DH	20H
PCCARD Status	2,6,7	Index 20H	Index 22H, 28H
PCCARD A I/O	2-7	Index 21	20H
PCCARD B I/O	2-7	Index 27H	20H
Real Time Clock	2	Index 79H	Index 7AH

Internal Interrupt Configuration Figure



Two pins, IRQA and IRQB, provide support for the standard IRQ inputs. Each one of these inputs can support IRQ2-IRQ7. The selection of which IRQ input level is gated to the IRQA or IRQB inputs is controlled through the ICU mode register at index 0DH.

Keyboard

The VG230 Single-Chip PC Platform provides two types of Keyboard interfaces:

- Internal Keyboard Scanner to control switch matrix
- PC/XT serial keyboard interface to connect to a stand-alone PC/XT keyboard subsystem.

When the Keyboard Scanner is enabled, it supports an external key matrix composed of up to 101 keys. Of these keys, 96 are organized in an 8 x 12 matrix and 5 are dedicated shift keys. When the Keyboard Scanner is disabled, some of the pins it controls are assigned to other internal functions. These functions are the Parallel Port, the PC/XT serial Keyboard interface, and control for a second PC Card Slot. The PC/XT Serial Keyboard Interface itself may also be disabled, allowing use of a separate keyboard controller. In this mode the KBDAT pin is defined as IRQ1. *For Register Description, see Index 08H.*

LCD Controller

The LCD Controller supports all CGA Text and Graphics display modes as well as AT&T 640x400 two-color graphics mode. AT&T “double-scanning” of 200 line text and graphics is also supported. For lower-resolution panels, the controller provides hardware support for windowing into the CGA or AT&T frame. This allows software to utilize 200 or 400 line display modes regardless of panel size.

For 200 line panels or smaller, an Ink Plane feature useful for pen-based applications is supported. A separate 200 line buffer receives ink traces which are superimposed on the main display buffer.

The LCD Controller supports a global enable/disable function. While disabled, all clocks within the LCD Controller are stopped to reduce power consumption, and the LCD Controller will not respond to either I/O or memory operations, except accesses to the LCD Configuration Control Register.

The LCD Controller uses main system memory. This provides very high video performance and eliminates the need for a separate display memory. The uppermost bank of RAM is used as the display buffer. CPU accesses to B800:0H are mapped by the VG230 hardware to this bank. *For Register Description, see Index C0H.*

VG230 Examples of Supported LCDs Table

640x400	Sharp	LM64060F
	Optrex	DMF666AN
	Hitachi	LMG6111XTFR
640x200	Casio	MD232TS01-00
	Epson	TCMA9108 9043D
	Hitachi	LMG6273XNFR
	Matsushita	EDMDG648A 33D
	Sanyo	LCM5205
640x100	Hitachi	LM266XW
480x128	Toshiba	TLX1241
320x200	Epson	EG7500B-LS
320x240	Optrex	DMF5008IN
	Sharp	LM320081
240x128	Optrex	DMF66ON
	Sharp	LM24009W, LM24010Z
240x64	Optrex	LM24013W
	Sharp	LM258XB
128x128	Optrex	DMF6116
128x64	Optrex	DMF697N

Note: *For unlisted panels or sizes, please contact Vadem.*

Memory Controller and Memory Manager

The VG230 supports DRAM, SRAM, PSRAM, ROM and FLASH memory devices. Timing for accesses to memory is based on the processor clock, CPUCLK.

In general, memory device types and sizes cannot be mixed. FLASH banks, however, can be installed above SRAM or PSRAM banks as long as data width and device sizes are consistent. The memory controller automatically allocates memory from the uppermost RAM bank for LCD video memory functions.

Memory management hardware is provided which facilitates the use of large ROMs, PCMCIA 2.1 (JEIDA 4.1) compatible cards, and expanded memory. As a compatible superset of LIM 4.0, its command set is easy to support. The memory manager is also compatible with the PCMCIA 2.1 LIM XIP (“execute-in-place”) specification for applications which execute directly out of ROM.

- Over and above base memory, five categories of memory are addressable.
  - Expanded memory (64MB address space).
  - Heavy-access ROM (highly power efficient, 1MB address space limitation).
  - Normal-access ROM (64MB address space).

  - PCMCIA 2.1 Card A (64MB address space).
  - PCMCIA 2.1 Card B (64MB address space).
- Addressing is paged, via 26 mapping registers.
  - Except for the non-mappable 32KB display memory (B800:0H-BFFF:FH), each 16KB "page" of the 1MB 8086 address space between 8000:0H and EFFF:FH is represented by its own mapping register.
  - Each mapping register includes a memory type specifier, which determine what memory category (expanded memory, heavy-access ROM, normal-access ROM, PC Card A or PC Card B) is being mapped to its page.
  - Mapping may be enabled/disabled globally, or on a page-by-page basis.
- Two ROM Chip Select outputs, *ROMCE0 and *ROMCE1, are available.
  - *ROMCE0 (heavy-access ROM) is always generated during BIOS ROM accesses (addresses F000:0H through FFFF:FH) and may also be generated during accesses to the ROM0 memory address space as specified in the Memory Mapping Registers.
  - *ROMCE1 (normal-access ROM) is an optional ROM Chip Select which may be used to implement ROM disks, ROMDOS, or embedded XIP applications.

VG230 Memory Combinations Table

RAM Device Size	32K x 8		128Kx 8		512K x 8		Max # RAM Banks	
Bus Bit Width	**8**	**16[1]**	**8**	**16[1]**	**8**	**16[1]**	**8**	**16[1]**
SRAM (bytes/bank)	32K	64K	128K	256K	512K	1M	8	6
PSRAM (bytes/bank)	32K	64K	---	---	512K	1M	7	6
PSRAM (bytes/bank)	---	---	128K	256K	---	---	6	4

[1] Bus bit width of 16 utilizes two 8bit parts in parallel.

DRAM Device Size	Bus Bit Width		Max # RAM Banks	
	8	**16**	**8**	**16**
256K x 1 (bytes/bank)	256K (8 devices wide)	512K (16 devices wide)	**6**	**5**
256K x 4 (bytes/bank)	512K (2 devices wide)	1M (4 devices wide)	**6**	**5**
512K x 8 (bytes/bank)	512K (1 device wide)	1M (2 devices wide)	**6**	**5**
1M x 1 (bytes/bank)	1M (8 devices wide)	2M (16 devices wide)	**6**	**5**
1M x 4(bytes/bank)	1M (2 devices wide)	2M (4 devices wide)	**6**	**5**
4M x 1 (bytes/bank)	4M (8 devices wide)	8M (16 devices wide)	**6**	**5**
4M x 4 (bytes/bank)	4M (2 devices wide)	8M (4 devices wide)	**6**	**5**
256K x 16 (bytes/bank)[2]		512K (1 device)		**6[2]**

[2] Extra bank with x16 DRAM.

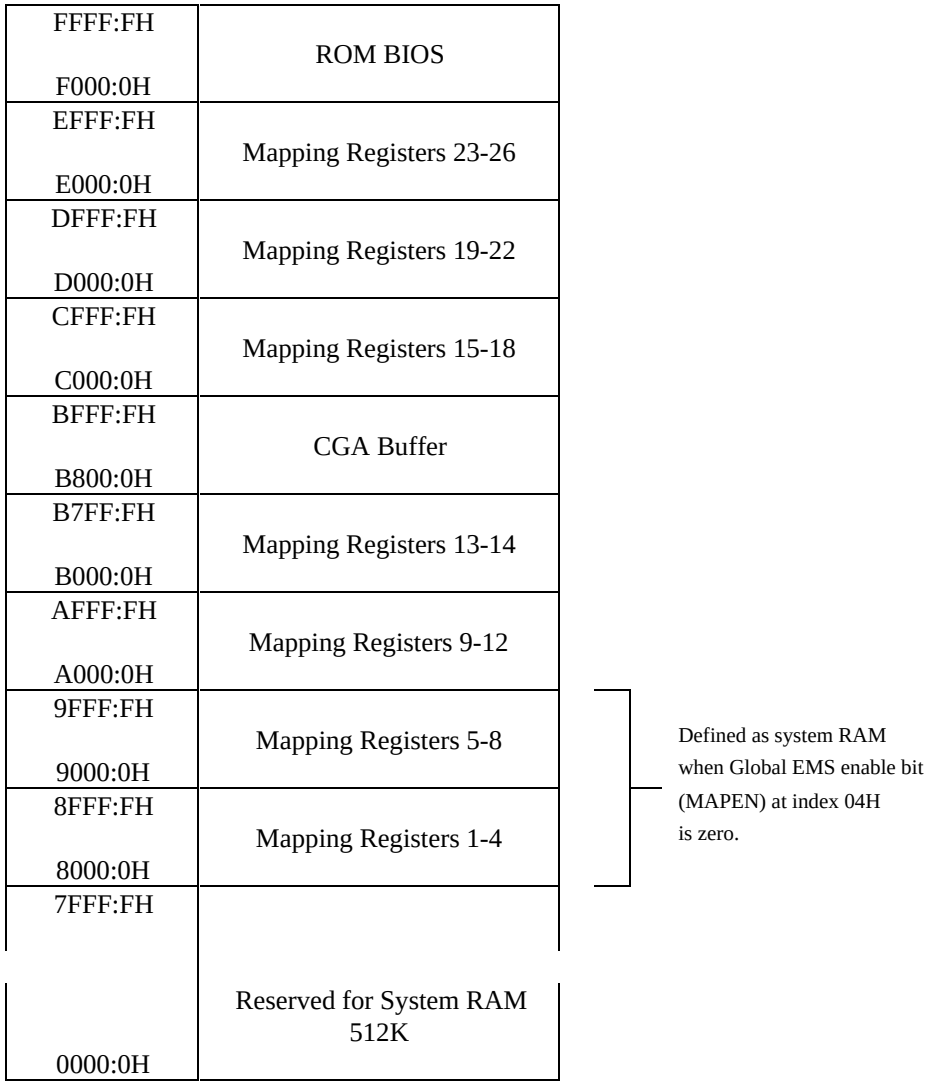
NOTE: *The above table describes RAM that is directly supported by the VG230. External logic can be used to utilize the full 64Mbyte of address space.*

Software may open a window into any of the five VG230 memory categories using Memory Mapping Registers. Each Mapping Register controls a 16 Kbyte page in the 1MB memory address space which is directly addressed by the 8086-compatible V30 CPU (see diagram on next page). Memory Mapping Registers may also be disabled. In this case, the 16KB page controlled by the Register directly addresses the standard 1MB V30/8086 memory address space.

Each Memory Mapping Register pair is composed of 16 bits. Of these, 12 bits define the offset into the memory space and are used to generate the memory address on the A25 - A14 lines, 3 bits define which of the five memory spaces will be accessed, and 1 bit acts as a page map enable/disable.

Accessing the VG230 Memory Mapping Registers involves three bytes in the CPU I/O address space. A particular Memory Mapping Register is accessed by first writing its CPU segment address into the Map Address Register at I/O address 06CH, and then reading from or writing to the Map Low Byte Data Register at I/O address 06EH or the Map High Byte Data Register at I/O address 06FH.

VG230 Memory Map Figure



System RAM Control Outputs Table

	DRAM			**SRAM**		**PSRAM**			
						32Kx8 or 512Kx8		**128Kx8**	
	8	16	256Kx16	8	16	8	16	8	16
*MC0	*CAS0	*CAS0	*RAS0	*CS0	*CS0	*CS0	*CS0	*CS0	*CS0
*MC1	*CAS1	*CAS1	*RAS1	*CS1	*CS1	*CS1	*CS1	*CS1	*CS1
*MC2	*CAS2	*CAS2	*RAS2	*CS2	*CS2	*CS2	*CS2	*CS2	*CS2
*MC3	*CAS3	*CAS3	*RAS3	*CS3	*CS3	*CS3	*CS3	*CS3	*CS3
*MC4	*CAS4	*CAS4	*RAS4	*CS4	*CS4	*CS4	*CS4	*CS4	*REFL
*MC5	*CAS5	*RASL	*RAS5	*CS5	*CS5	*CS5	*CS5	*CS5	*REFH
*MC6	*RASL	*RASH	*CASL	*CS6	*OEL	*CS6	*OEL	*REFL	*OEL
*MC7	*RASH	*OE	*CASH	*CS7	*OEH	*OEL	*OEH	*REFH	*OEH
*MC8	*OE	*WEL	*OE	*OE	*WEL	*OEH	*WEL	*OE	*WEL
*MC9	*WEL	*WEH	WE	*WE	*WEH	*WE	*WEH	*WE	*WEH

Notes: **RASH, *OEH and *WEH are asserted during Odd Byte and Word accesses for 16 bit RAM arrays, or during accesses to Odd numbered banks (1,3,5...) for 8 bit RAM arrays. *RASL, *OEL, and *WEL are asserted during Even Byte and Word accesses for 16 bit RAM arrays, or during accesses to Even numbered banks (0,2,4...) for 8 bit RAM arrays.*

*For PC memory cards, MC8 is defined as *OE and MC9 as *WE.*

DRAM Address Muxing Table *8 BIT BUS*

	256K		512K		1M		4M	
ADDRESS	**R**	**C**	**R**	**C**	**R**	**C**	**R**	**C**
0	0	9	0	9	0	9	0	9
1	1	10	1	10	1	10	1	10
2	2	11	2	11	2	11	2	11
3	3	12	3	12	3	12	3	12
4	4	13	4	13	4	13	4	13
5	5	14	5	14	5	14	5	14
6	6	15	6	15	6	15	6	15
7	7	16	7	16	7	16	7	16
8	8	17	8	17	8	17	8	17
9			18	X	18	19	18	19
10							20	21

DRAM Address Muxing Table *16 BIT BUS*

	256K		512K		1M		4M	
ADDRESS	**R**	**C**	**R**	**C**	**R**	**C**	**R**	**C**
0	1	10	1	10	1	10	1	10
1	2	11	2	11	2	11	2	11
2	3	12	3	12	3	12	3	12
3	4	13	4	13	4	13	4	13
4	5	14	5	14	5	14	5	14
5	6	15	6	15	6	15	6	15
6	7	16	7	16	7	16	7	16
7	8	17	8	17	8	17	8	17
8	9	18	9	18	9	18	9	18
9			19	X	19	20	19	20
10							21	22

Parallel Port

The Parallel Port is PC/XT compatible and is only enabled when the Keyboard Scanner is disabled. An external 74XX374 is required for latching parallel data. The parallel port is also software configurable to appear at LPT1, LPT2 or LPT3 and supports the standard PC/XT PIO interrupt (IRQ7). Optionally, the parallel port may be configured for full 8 bit bidirectional capability with the addition of external components.

The Parallel Port may be similarly configured to appear at a non-standard I/O address. This allows use of the port's pins by dedicated applications for general purpose input and general purpose output (GPI and GPO).

PC Card Controller

The VG230 Single-Chip PC Platform PC Card Controller provides support for up to two PCMCIA 2.1 (JEIDA 4.1) card slots. Both I/O and memory cards are supported, as is the memory-saving XIP ('execute-in-place') standard. A single PC Card slot is always supported by the VG230. A second PC Card slot is supported when the internal Keyboard Scanner is disabled.

Access to PC Card memory on the VG230 uses a superset of LIM 4.0. Memory mapping for PC Cards follows the same approach as memory mapping for expanded memory and uses the same registers. This flexibility simplifies driver design, allowing generic routines to access any memory type. For I/O cards, an I/O window can be defined anywhere within the 64KB address space. I/O is not paged.

The PC Card Controller provides power management functions for PC Cards. When enabled by software, power may be automatically removed from the Cards after a programmable period of inactivity. Optionally, the PC Card Controller may generate an interrupt to inform the CPU that the PC Card is idle. Software may then remove power to the Card if desired. Power also can be removed from the Cards when the Power Management Unit (see pg. 36) indicates SLEEP mode.

Besides generating an interrupt to inform the CPU of the PC Card's activity status, the PC Card Controller also may generate an interrupt (when enabled by software) for the following conditions:

- Low Battery warning from PC Card
- Battery Fail Alarm from PC Card
- Card Removal
- IREQ signal from I/O Cards
- Status changed signal (STSCHG) from I/O Cards

Each of the above sources is individually maskable by system software.

The PC Card Controller supports "hot" insertion and removal of PC Cards when external buffers are added. *For Register Description, see Pg. 99.*

PCMCIA PC Card Support

PCMCIA version 2.1 is fully supported in the VG230. If the internally scanned keyboard is enabled, a single PC card slot is supported. If the scanned keyboard is disabled, two PC card slots are supported. Version 2.1 of the PCMCIA standard supports the following:

- I/O cards
- Up to 64 Mbytes of memory
- Flash memory
- Execute in place (XIP)

The PC Card Slot 0 Control Register at index 21H sets various operating modes for the PC card. IO8BIT sets the I/O word length for the PC card in slot 0 when configured in the I/O mode. When cleared, data is transferred on D[7:0] and when set, data is transferred on D[15:0].

IO/*M sets whether the card in slot 0 is configured for I/O or memory interface. This bit is reset (to a memory configuration) when the PC Card is powered off or a card is changed.

The *REG bit controls the *REGA pin on the PC Card interface. When cleared, the *REGA pin is forced low, enabling the PC card's attribute memory. This memory is accessed through the memory space and contains details on the PC card physical and logical configuration.

The IRCRD[2:0] bits select the interrupt level for a PC card configured for I/O. These bits are only valid when the IO/*M bit is set. For example, a modem card will use IRQ4 for COM1 or IRQ3 for COM2.

The CDLY[1:0] bits select the memory read command delay for accesses to the PC Card. Default is 1 CPUCLK cycle.

The PC Card Slot 0 Status Register at index 22H indicates various status items of the card in slot 0.

***BUSY/*CRDINT -** in memory mode this is a read-only bit reflecting the state of the RDY/*BSYA input. When cleared, the card is busy.

In I/O mode, this bit indicates the presence of a pending interrupt. The pending interrupt status is cleared by writing a 1 to this bit.

BVD2/*AUDIO - In memory mode with status interrupts disabled, this bit reflects the state of the BVD2A (Battery Voltage Detect Pin 2). When status interrupts are enabled, this bit indicates a pending status interrupt. The pending interrupt is cleared by writing a 1 to this bit.

In I/O mode, this bit reflects the state of the *SPKR input. This input can be monitored to see if the I/O card is generating any audio.

BVD1/*STSCHG - In the memory mode with status interrupts disabled, this bit reflects the state of the BVD1A (Battery Voltage Detect Pin 1). When status interrupts are enabled, this bit indicates a pending status interrupt. The pending interrupt is cleared by writing a 1 to this bit.

In the I/O mode, this bit reflects the state of the *STSCHG input. When interrupts are enabled, this bit indicates that a *STSCHG interrupt is pending. Writing a 1 to this bit will clear the status change interrupt.

***PRESENT -** This bit indicates that a card is properly inserted into the PC card socket. When low both *CD2A and *CD1A are active indicating that both sides of the card are properly seated in the socket.

***CRDCHG -** This bit is cleared when a card change occurs. It is cleared on the rising edge of either *CD[2:1]A. When status interrupts are enabled, this bit indicates a pending interrupt. Writing a 1 to this bit clears the pending interrupt.

CRDTM0 - This bit indicates that the PC card activity timer has timed out and an interrupt is pending. Writing a 1 to this bit clears the pending interrupt.

WP/NU - This bit reflects the state of the WPA input pin. This pin is only used in the memory interface and is not used when in I/O mode. When this bit is a 1, the card is write-protected.

CRDOFF - Status bit indicating that the power to both PC cards is off. A 1 in this bit indicates that power to the interface is off.

Power Management Unit

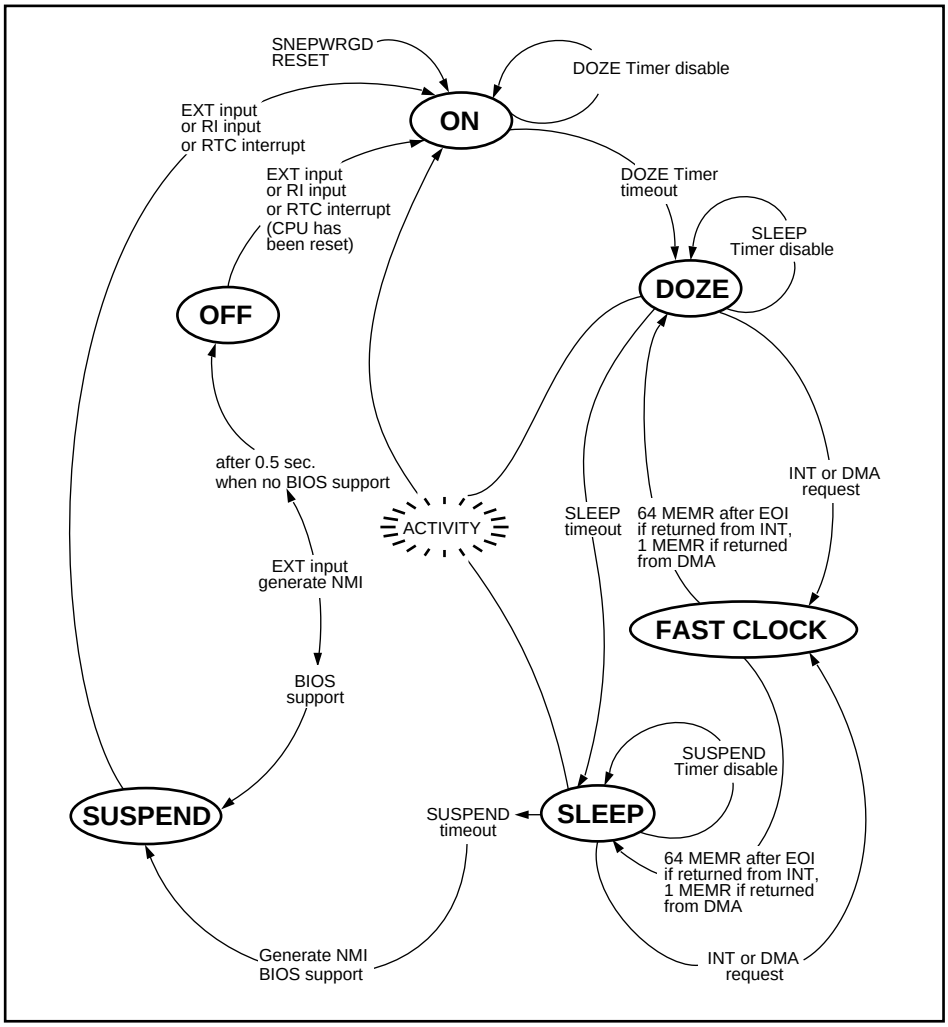
The Power Management Unit (PMU) of the VG230 Single-Chip PC Platform is based on the field-proven Vadem VG-647 (Intel™ 82347) notebook power management chip. It reduces overall system power consumption, lengthening battery life significantly. Several types of system activity are monitored and the appropriate power management mode (ON, DOZE, SLEEP, SUSPEND or OFF) is selected based on built-in criteria refined through the VG-647 experience. From ON to DOZE and then to SLEEP, the CPU clock may be slowed or stopped. In SUSPEND, power is removed from all functional system blocks except the VG230 and system RAM. In OFF, only the VG230 is powered. Total operation power is reduced automatically during periods of inactivity. Inactivity is determined by hardware in the PMU or through software control.

It is important to note that following a hard reset or a RESUME from SUSPEND or OFF modes, the PMU registers are write protected. Software must read the PMU Supply Register at Index C1H to unlock these registers.

The PMU also manages power to the various peripherals. For example, control of the LCD power is shared between the PMU and the LCD Controller. The PMU performs activity monitoring and generates a Power On/Off signal to the LCD Controller. The LCD controller uses this signal to trigger LCD power sequencing.

The PMU also monitors the battery voltage status and produces a maskable interrupt on Low Battery. *For Register Description, see Index C4H.*

VG230 PMU State Diagram



Activity Monitor

The activity monitor determines when the PMU changes states. The activity monitor can monitor access to the following PC I/O devices:

Activity Monitor Address Table

Parallel Printer Port LPT1 LPT2 LPT3	I/O R/W access to LPT1-LPT3 378H - 37FH 278H - 27FH 3BCH - 3BEH
Keyboard Port	I/O Reads to port 60H
Real Time Clock	I/O R/W access to port 70H/71H
Serial I/O COM1 COM2	I/O R/W access to COM1 and COM2 3F8H - 3FFH 2F8H - 2FFH
Floppy Disk	I/O R/W access to 3F5H
Hard Disk XT Disk AT Disk	I/O R/W access to XT or AT hard disk 320H - 323H 1F0H - 1F8H
Video Memory Access	Access to CGA video memory
Programmbale I/O	See description of PMU I/O Range register IORNG
Note: *The Real Time Clock activity bit does not monitor access to the VG230's internal real time clock. Access to the standard "PC/AT" RTC at I/O address 70H/71H is monitored. If the designer wishes to trigger the activity monitor for accesses to the VG230's internal RTC, the RTC's BIOS routine can do a "dummy" read from 70H or 71H.*	

Power Control Registers

Each power management mode has an associated power control register. These registers determine the state of the power control pins (VP pins) during the various modes. The power control registers are 8 bits in width, however only 4 of these bits are used in the VG230.

PWRON C6H	PWRDOZE C7H	Bit	PWRSLEEP C8H	PWRSUSPEND C9H	Description
0	1	0	0	0	VPLCD and VPBIAS control.
1	1	1	0	0	Not used.
1	1	2	1	0	VPSYS control.
1	1	3	1	0	VPCARD control.
1	1	4	0	0	Not used.
1	1	5	0	0	Not used.
1	1	6	0	0	Not used.
1	1	7	0	0	VPRAM control.

The power registers are as follows:

PWRON	at C6H	with a default of FEH
PWRDOZE	at C7H	with a default of FFH
PWRSLEEP	at C8H	with a default of 0CH
PWRSUSPEND	at C9H	with a default of 00H

The default polarity of each power control bit is **high true** except polarity of VP0, but may be changed individually by programming the PMU POLARITY register (index CAH). This is primarily intended to simplify LCD power control logic. After a hard reset, the VG230 automatically tri-states the VPLCD and VPBIAS outputs so that external pullup or pulldown resistors (depending on polarity) on the VPLCD and VPBIAS controls can force the power control devices to their off state. This allows firmware to set power control bit polarity to **low true** if appropriate. LCD power-up sequencing after hard reset begins only after both the SEQEN bit of the PMU LCD Sequence Register (D4H) and the VIDE bit of the Mode Select Register A (3D8H) are set high. VPSYS, VPRAM and VPCARD are not tri-stated by the VG230. *For Register Descriptions, see Index C6H-69H.*

Power Management Status

The BIOS can interrogate the state of power management by checking the value of the STATE bits located in the PMU Status Register at index C0H. Bits D0 and D1 reflect the current state of the PMU. These bits can also be written to force the PMU into the desired state.

Real Time Clock

The VG230 Single-Chip PC Platform's Real Time Clock (RTC), besides timekeeping, provides 64 bytes of CMOS RAM to store system set-up information. The RTC contains CMOS static RAM from index 80H to BFH. This RAM is accessed through the VG230's Indexed registers. The RAM is valid as long as the VALID bit is set at index 7AH. The RTC RAM contains a write protect feature that is enabled via the *RAMEN bit located in the RTC Mode Register at index 79H. When the *RAMEN bit is cleared, RAM reads and writes are enabled. When *RAMEN is set, all read and write accesses are disabled. This feature prevents inadvertent writes to the CMOS RAM.

Real Time Clock Alarm Wake-Up Feature

The VG230 can be placed into the ON state from the OFF or SUSPEND state through the internal RTC alarm. The alarm is enabled through the Real Time Clock configuration registers at indeces 75H-79H.

System Management Unit

The System Management Unit (SMU) of the VG230 Single-Chip PC Platform helps solve certain system issues arising in super-portable PC compatibles. For example, power managing peripheral devices might require shutdown. Using the SMU and appropriate firmware, a VG230 based system can intercept application accesses to the shut-down device, reapply power, restore any lost set-up parameters, and only then restore control to the application, shielding it from the need to know the power state of the device. Another use might be to make a non-standard I/O device look to applications like a standard PC device. In this case, the SMU would intervene in I/O situations, invoking a firmware routine which would emulate the device's standard behavior in software.

In general, when software-enabled, the SMU monitors the CPU, looking for I/O activity on up to three selectable port ranges. When execution of an I/O instruction on a target range is imminent, the SMU hardware interrupts the CPU. After invoking system management functions written in standard 8086 code, it guarantees resumption of the interrupted routine at the proper point. In other words, the functioning of the system management firmware can be made completely invisible to user software.

System Power Management

The VG230 contains power management logic which controls five separate functional blocks; System, RAM, LCD, PC Card, and the Serial port.

This is the primary means of controlling power in the VG230 and the overall system. System power management is composed of five basic power states; ON, DOZE, SLEEP, SUSPEND, and OFF. The table following indicates the different modes and their effect upon the system.

System Power Management Modes Table

Mode	OSC	LCD	CPU Clock	I/O Pins	Memory I/F	Wakeup By
ON	On	On	Full Speed	Active	Active	---
DOZE	On	On	Stopped (Static mode) or Divided by 4 or 8 (Slow Clock mode)	Active	Active	Static mode: Interrupt or DMA Request or Slow Clock mode: Interrupt, DMA Request, or programmed activity (See Note 2)
SLEEP	On	Off	Stopped (Static mode) or Divided by 4 or 8 (Slow Clock mode)	Active (See Note 1)	Active	Static mode: Interrupt or DMA Request or Slow Clock mode: Interrupt, DMA Request, or programmed activity (See Note 2)
SUSPEND	Stopped	Off	Stopped	Input pins inactive, Outputs drivenHi-Z	Active, providing automatic refresh	EXT or RI inputs, or internal RTC alarm
OFF	Stopped	Off	Stopped	Input pins inactive, Outputs drivenHi-Z	Off, Driven Hi-Z	EXT or RI inputs, or internal RTC alarm

Note 1: *During SLEEP mode, the behavior of the system control logic is the same as DOZE mode behavior. In SLEEP mode, however, functional blocks such as the PC Card and LCD may be automatically powered down on entering the mode.*

Note 2: *An interrupt or DMA request does not cause the VG230 to exit the current power management mode. Instead, the CPU clock will temporarily return to full speed to service the interrupt or DMA cycle. Only programmed activity will force a return to the ON state.*

The ON State

The ON state is the full power, full performance state of the VG230 system. To conserve maximum power it is desirable to remain in the ON state only during computational intensive periods. During the ON state, all I/O peripherals are powered up with clocks supplied.

The DOZE State

The DOZE state is the first level of power management. DOZE state is typically entered within a few seconds of inactivity. It is entered when the DOZE timer at index CCH expires. The DOZE state reduces the operating frequency of the internal V30HL CPU. This reduction is controlled by

the DOZE divider value specified in the PMU Resume Status Register located at Index DAH. Any write to this register also enables the EXT NMI.

The DOZE state can be entered through program control by writing the DOZE command to the STATUS register at index C0H. DOZE state exits to the ON state when activity is detected. DOZE state exits to the SLEEP state when the SLEEP timer expires. Activity type is determined from the PMU Activity Status Register (DBH).

The SLEEP State

SLEEP state is the lowest power state available without going into the SUSPEND state. Sleep is typically entered within 2 - 5 minutes after the DOZE state. There are three ways to enter the SLEEP state:

1) Under program control from the DOZE state when the SLEEP timer times out and generates an NMI as a result of lack of activity. This will be referred to as NMI SLEEP state.
2) Under program control from the ON or DOZE state at any time.
3) Automatically from the slow clock DOZE state when the SLEEP timer times out as a result of lack of activity.

The SLEEP state reduces the operating frequency of the internal V30HL CPU. This reduction is controlled by the SLEEP divider value specified in the PMU Resume Status Register located at index DAH. Any write to this register also enables the EXT NMI.

SLEEP State Via NMI

This mode of SLEEP state is software controlled. This allows power control of I/O devices with register controlled power down modes. To enable NMI SLEEP mode, unmask the SLEEP timeout bit (bit 4) in the NMIMASK register (C4H).

When the SLEEP timer expires, an NMI is generated to inform the BIOS that it's time to power down certain parts of the system. The NMI handler would interrogate the VG230 STATUS register cause code and determine that the SLEEP state NMI has been generated. The NMI routine will reset the NMI by clearing the NMI cause code in the STATUS register. The NMI is cleared by reading the NMI register at index C4H. At this point the BIOS needs to mask the activity monitor to prevent exiting the DOZE state when powering down devices. The BIOS now puts devices in the low power mode. Now the activity monitor can be re-enabled. The BIOS will then put the VG230 into SLEEP state by setting SLEEP state in the STATUS register.

SLEEP State Via Software Command

This method of entering the SLEEP state involves writing the SLEEP command directly to the STATUS register at index C0H. SLEEP can be entered from the ON or DOZE states at any time through this method.

Automatic SLEEP State

Automatic SLEEP state can be entered automatically via the SLEEP timer. When no activity is detected for the time specified in the PMU SLEEP Timer register at index CDH and the NMI SLEEP timeout bit is masked in the NMIMASK register, the PMU will enter the SLEEP mode. In the SLEEP mode, the LCD and the PC card can be powered down. The SLEEP state also maintains the reduced clock to the CPU. The SLEEP state is exited through the detection of activity or through software command.

When the BIOS puts the VG230 into SLEEP state, power to the LCD can be controlled. Selection of the LCD or Card power off during SLEEP state is controlled through the PWRSLEEP register (C8H). SLEEP state will maintain the reduced clock mode of the DOZE state.

The SUSPEND State

The VG230 supports the saving of all external chip status to memory for resumption at a later time. This is called SUSPEND/RESUME. The SUSPEND state can be user-invoked via a signal on the EXT pin or automatically invoked by via the SUSPEND timer. The BIOS detects a request to enter SUSPEND state through an NMI. The BIOS then interrogates the VG230 STATUS register to determine if the NMI is the result of a SUSPEND request. After allowing the system to finish any DMA or interrupt activity it then saves the system status. The BIOS is also responsible for saving the states of all external devices to non-volatile memory. The BIOS sets the SUSPEND status field in the STATUS register located at index C0H. At this point the VG230 enters SUSPEND state. Power control devices activated by VP pins will be turned off according to the PWRSUSPEND register (C9H).

The BIOS command to SUSPEND is followed by a loop which polls the PMU Status Register, looking for the WAKEUP state.

Less than 15 microseconds of instructions may be executed between the BIOS command to SUSPEND and the moment the clock is actually stopped.

SUSPEND Via Hardware Timeout

The following procedure describes the entrance into SUSPEND state via an internal hardware timer (SUSPEND timer).

1) Enable SUSPEND timer by writing a non-zero value to the SUSPEND register at index CEH.
2) Enable SUSPEND NMI by clearing bit 5 of the NMIMASK register at index C4H.

   An NMI will be generated after the VG230 is in the SLEEP state for the time specified in the SUSPEND REGISTER.
3) After the NMI is received, the STATUS register (C0H) should be read to determine the NMI source. The NMI is cleared by reading the NMIMASK register at index C4H.
4) Save system status and place VG230 into SUSPEND state by writing the PMU Status Register.

5) The CPU should wait until the WAKEUP CODE is present in the PMU Status Register and PMUREF is low in the PMU Resume Status Register (DAH).

6) Restore system and VG230 status.

SUSPEND Via EXT Input

The following procedure describes the entrance into SUSPEND state via an external switch input (EXT input).

1) Enable EXT NMI by clearing bit 1 of the NMIMASK register at index C4H. An NMI will be generated after the VG230 detects a positive transition on the EXT input.

Follow steps 3 to 6 above.

SUSPEND Via Software Command

The system may be placed into the SUSPEND mode from the ON, DOZE or SLEEP state by writing a 03H into the STATUS register (index C0H). Software should follow the procedure outlined above.

RESUME

The VG230 will enter the ON state when one of the following events happens: an EXT input, a Real Time Clock Alarm Input, or a modem Ring Indicate.

The RESUME source identification will be stored in the WU[1:0] status located in the STATUS register (C0H). Normally, RESUME does not reset the CPU. The CPU will restart executing the code it was executing when it was suspended.

The BIOS is responsible for reading the RESUME bit in the STATUS register to determine if a cold boot or return from SUSPEND is requested. If return from SUSPEND is indicated, the BIOS should restore any external devices and verify that the main memory and video memory is still valid. If main memory, video memory or I/O is corrupted, then a cold boot should be performed. Otherwise RESUME can be continued. Note that reading the RESUME bit in the STATUS register resets the RESUME bit..

The OFF State

The OFF state is similar to the SUSPEND state, except that the DRAM refresh feature is disabled. The OFF state is used when the contents of the system RAM are not required. In the OFF state, the VG230's RTC and internal CMOS RAM are maintained. Transition from the OFF state to the ON state results only in resetting the CPU. This transition is treated by the BIOS as a cold boot.

Power Sequencing

In power management modes SLEEP, SUSPEND and OFF, the VG230 itself remains powered at all times. As a result, care must be taken when configuration VG230 pins during these modes, both to protect the system against possible latch-up and to prevent excessive current consumption.

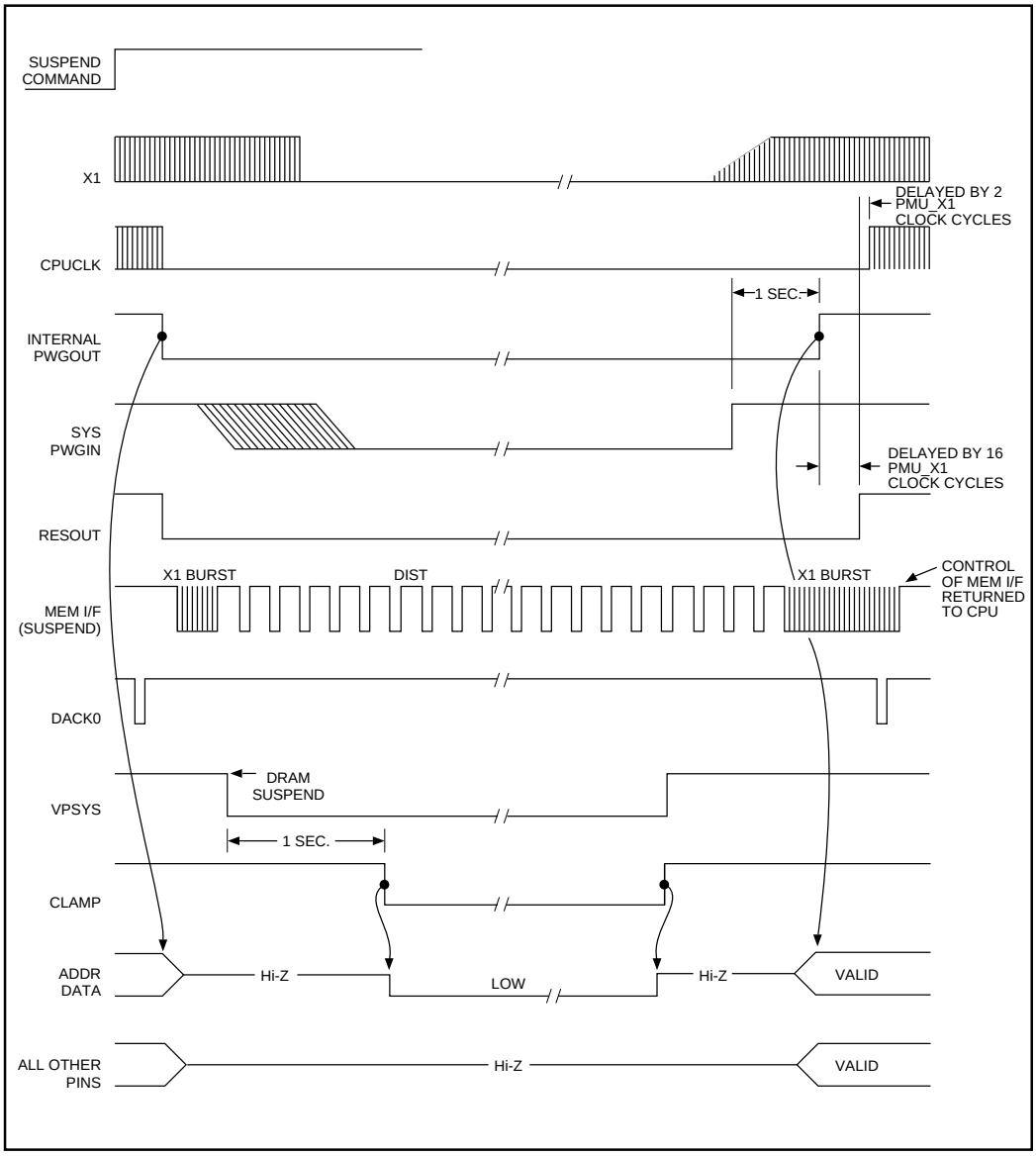
In general, all output pins are driven Hi-Z while power to devices connected to them is removed. The exceptions are A[25:0] and D[15:0], which will be driven low during SUSPEND to prevent excessive current consumption of the system RAM. An internal signal from the power management unit (PMU) called *CLAMP controls the state of A[25:0] and D[15:0]. During OFF mode, these pins will be driven Hi-Z along with the rest of the VG230's pins.

Entering SUSPEND Mode (DRAM/PSRAM systems)

For DRAM and PSRAM systems, when software commands the PMU into the SUSPEND mode, the PMU begins its SUSPEND sequence.

- On the rising edge of *DACK0 (Internal refresh signal), the PMU takes control of the memory interface.
- Internally the refresh clock is switched from the main 32MHz clock to the 32.768KHz clock
- On the falling edge of PWGOUT, the internal CPUCLK is stopped.
- The *RESOUT pin is driven low.
- All VG230 output pins are driven Hi-Z, including A[25:0] and D[15:0].
- Following the completion of the Burst refresh cycle, the PMU will drive the VPSYS pin inactive and begin generating refresh cycles timed from the 32KHz clock. The 32MHz oscillator will continue to run until the power sequencing to the LCD is complete.
- Approximately 1 second after VPSYS is driven inactive, the PMU will assert an internal *CLAMP signal. At this time the A[25:0] and D[15:0] pins will be switched from Hi-Z to low driven outputs and the transition from ON to SUSPEND will be complete.

Entering / Exiting SUSPEND - DRAM System Figure



Exiting SUSPEND mode (DRAM/PSRAM systems)

The transition from the SUSPEND mode to ON mode requires a RESUME operation which repowers the external bus, switches the refresh time base from 32KHz to CPUCLK and re-enables the VG230 output pins.

- EXT input
- *RI input
- Internal RTC alarm interrupt

Once any one of these sources triggers a RESUME, the internal *CLAMP signal is immediately driven high, forcing the A[25:0] and the D[15:0] pins Hi-Z, VPSYS is driven active, and the 32MHz oscillator is restarted. The PMU then waits for the system power supply to return SYSPWRGD before beginning a burst refresh of the system RAM.

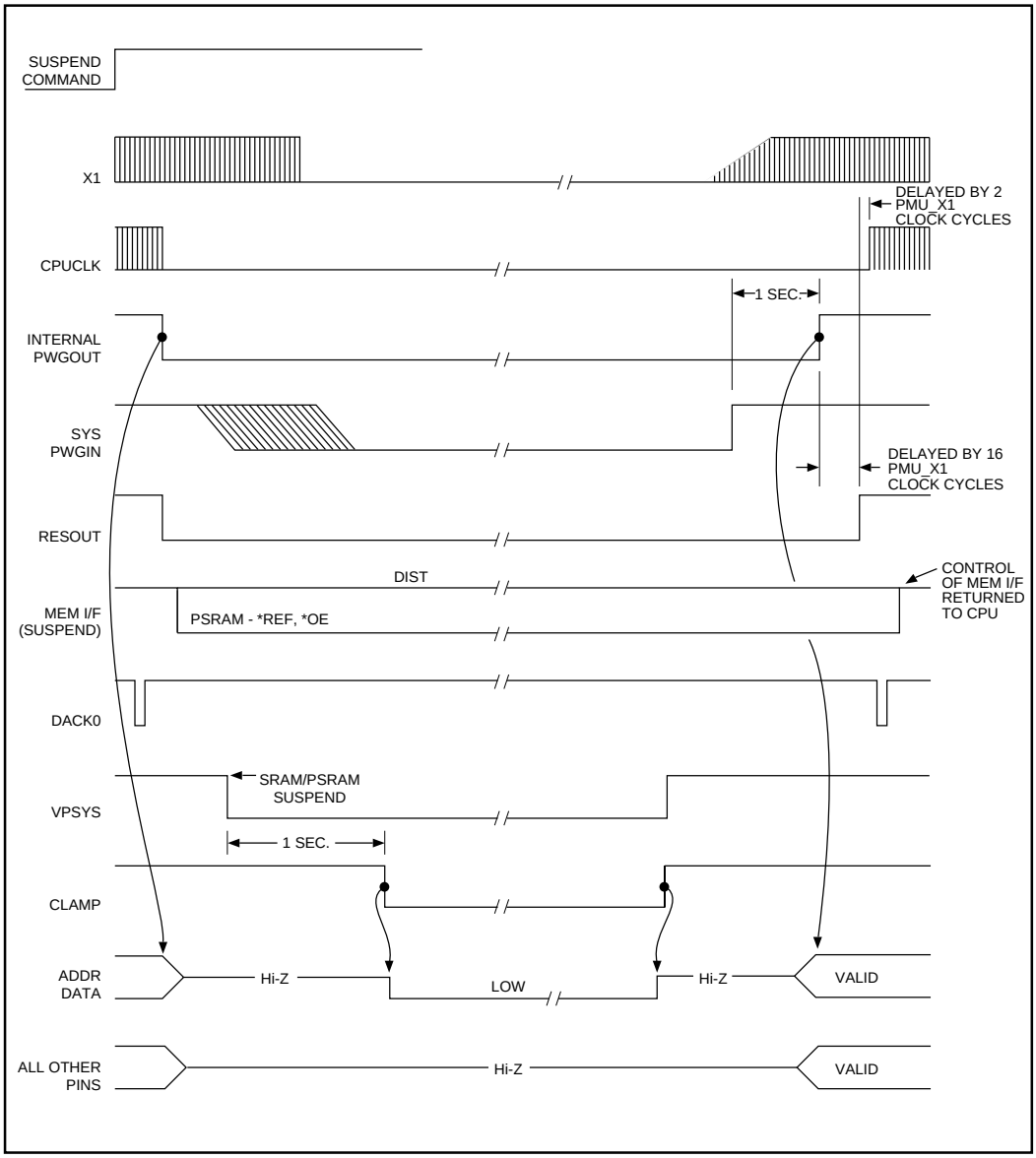
Approximately 1 second after the system returns SYSPWRGD, the PMU will re-enable all VG230 output pins. After 16 X1 clock cycles the *RESOUT signal to the external bus will be deasserted and two X1 clock cycles later the CPUCLK will be re-enabled. At this time the RESUME operation will be complete and the system will be in the ON state.

Entering SUSPEND Mode (SRAM)

For SRAM systems, when software commands the PMU into the SUSPEND mode, the PMU starts its SUSPEND sequence.

- All *MC[9:0] and A[25:0] and D[15:0] are driven Hi-Z
- PMU deasserts VPSYS
- The *RESOUT pin is driven low
- All other I/O lines are driven to a Hi-Z state
- Approximately 1 second after VPSYS is driven inactive, the PMU will assert an internal *CLAMP signal. At this time the A[25:0] and D[15:0] pins will be switched from Hi-Z to low driven outputs and the transition from ON to SUSPEND will be complete.

Entering / Exiting SUSPEND - SRAM / PSRAM System Figure



Exiting SUSPEND Mode (SRAM)

The transition form the SUSPEND mode to ON mode requires a RESUME operation which repowers the external bus, switches the refresh time base from 32KHz to CPUCLK and re-enables the VG230 output pins.

RESUME may be initiated from the following sources:

- EXT input
- *RI input
- Internal RTC alarm interrupt

Once any one of these sources triggers a RESUME, the internal *CLAMP signal is immediately driven high, forcing the A[25:0] and the D[15:0] pins Hi-Z, VPSYS is driven active, and the 32MHz oscillator is restarted. Approximately 1 second after the system returns SYSPWRGD, the PMU will re-enable all VG230's output pins. After 16 X1 clock cycles the *RESOUT signal to the external bus will be deasserted and two X1 clock cycles later the CPUCLK will be re-enabled. At this time the RESUME operation will be complete and the system will be in the ON state.

Entering OFF Mode (All RAM types)

When software commands the PMU into the OFF mode, the PMU immediately deasserts VPSYS and begins the system power down cycle.

- PMU deasserts VPSYS and VPRAM
- The *RESOUT pin is driven low
- All I/O pins driven Hi-Z
- CPU is reset

Power Down Considerations

During Suspend mode, the VG230 and the RAM array remain powered. This keeps the real time clock operating and system setup configuration stored. During this state the VG230 will consume less than 100uA. Care must be taken in the design to prevent any current leakage paths between the powered up sections of the system and powered down. The VG230 leakage control circuitry drives certain inputs to prevent excessive current consumption. Also certain outputs are driven low or tri-stated to terminate inputs outside of the VG230.

Low Battery Input (LB)

A single Low Battery Input (LB) provides monitoring for the primary battery source. The LB input is a standard TTL level input, to which an external comparator circuit should supply a low level when the battery condition is at a good level. A high on LB input will initiate an NMI within 15 seconds if the LB NMI bit in the NMIMASK register is unmasked. When the LB input stays high and is not masked, the LB interrupts will be generated every 60 seconds. The status of the Low Battery Input can be read in the PMU Supply Register (index C1H). *For Register Descriptions, see Pg. 127.*

Modem Ring Indicator Input (RI)

The VG230 can be placed into the ON state from the OFF or SUSPEND state through the modem ring-in signal. The signal must be supplied as a TTL level signal and be a filtered square wave. The RI input is a positive edge triggered input. The VG230 will go into the ON state after the number of positive transitions on the RI line specified in the PMU CONTROL register (index C2H). If not used, the RI input should be tied low.

Suspend Mode Support of DRAM Refresh

Refresh pulses are generated automatically in the SUSPEND state when the DRAM memory type is selected. When the BIOS places the VG230 into the SUSPEND mode, a power down sequence is initiated. All *CAS lines are driven low and the VG230 begins generating CAS before RAS refresh cycles. *RAS cycles are generated every 15µS. If the SLWREF bit in PMU control register at index C2H is set, the VG230 supplies refresh pulses every 120µS. During the SUSPEND state all Address lines during these DRAM cycles are clamped low. Data lines are forced to tri-stated.

System Power Control - VPSYS

The VPSYS signal controls the main power to the system. VPSYS is typically used to control power to the peripherals and ROM. VPSYS can be used to control a switching power supply or enable power via a MOSFET switch.

External Input (EXT)

The EXT input is used to turn on/off the system power. This signal is typically connected to a momentary contact switch. The EXT input is internally debounced and can be directly connected to a mechanical switch. When the system is in the SUSPEND state and the EXT switch is low for more than 60ms, and then becomes high, the VG230 will be placed into the ON state.

When the VG230 is in the ON, DOZE or SLEEP state, a positive transition on the EXT input, after it has been low for 60ms, will cause an NMI to be generated to inform the system that a request to power down has been received. The BIOS can place the system into the SUSPEND or OFF state. If the NMI is not serviced within 1/2 second, the system will enter the OFF state automatically.

PC Card Power Management

The PC Card controller also supports two power states; ON and SLEEP. The PC Card SLEEP state may be triggered independently of the System power management control. An internal activity timer monitors accesses to the PC Cards and may interrupt system software when the programmable time-out expires, or alternatively may automatically remove power to the PC Cards. The PC Card power management logic also allows PC Cards to be powered down when the system enters SLEEP mode. The table following indicates the two PC Card power modes and their effect upon the system.

PC Card Power Management Table

Mode	PC Card	PC Card I/F	Wakeup By
ON	On	Active	---
SLEEP	Off	Hi-Z	Software command

Serial Port Power Management

The serial port provides power management in the form of both internal serial clock control and control of the serial port oscillator. Power reduction may be realized under normal operation by stopping the internal serial clock. Control of the serial clock oscillator must be controlled by software due to the latencies involved with restarting the oscillator. The Serial Port SLEEP State may be triggered independently of the System power management control. An internal activity timer monitors accesses to the serial port transmit buffer and/or serial inputs and may automatically stop the serial port clock. The table following indicates the three serial port power modes and their effect upon the system.

Serial Port Power Management Modes Table

Mode	Serial OSC	Serial Port Clock	Wakeup By
ON	On	Full Speed	---
SLEEP with oscillator enabled	On	Stopped	Write to Transmit Buffer and/or Activity on Serial Port Inputs
SLEEP with oscillator disabled	Off	Stopped	Software command

Timer

The VG230 Single-Chip PC Platform's Timer is based on the PC/XT compatible 8254. The Timer clock is generated by dividing the clock source to produce a 1.19318 MHz TCLK.

Channel 0	Reserved for System Timer (18 Hz periodic interrupt)
Channel 1	Reserved for Memory Refresh (DRQ0 generation)
Channel 2	Controls the System Speaker

LCD Power Management

The LCD controller supports two power states: ON and SLEEP. The LCD SLEEP state may be triggered independently of the System power management control. An internal activity timer monitors keyboard activity and write operations to the video display buffer. When the programmable time-out expires (Index CFH), the LCD panel is automatically powered down. Alternatively, the LCD may be powered down when the system enters SLEEP mode. For proper system operation, software must power-down the LCD prior to entering SUSPEND mode. The table following indicates the two LCD power modes and their effect upon the system.

LCD Power Management Table

Mode	LCD Clock	LCD	Display RAM	LCD I/F	Wakeup By
ON	Full Speed	On	Active	Active	---
SLEEP	Stopped	Off	Accessible by CPU but LCD Display is OFF	Driven Low	Keyboard Input or Write to Video Memory

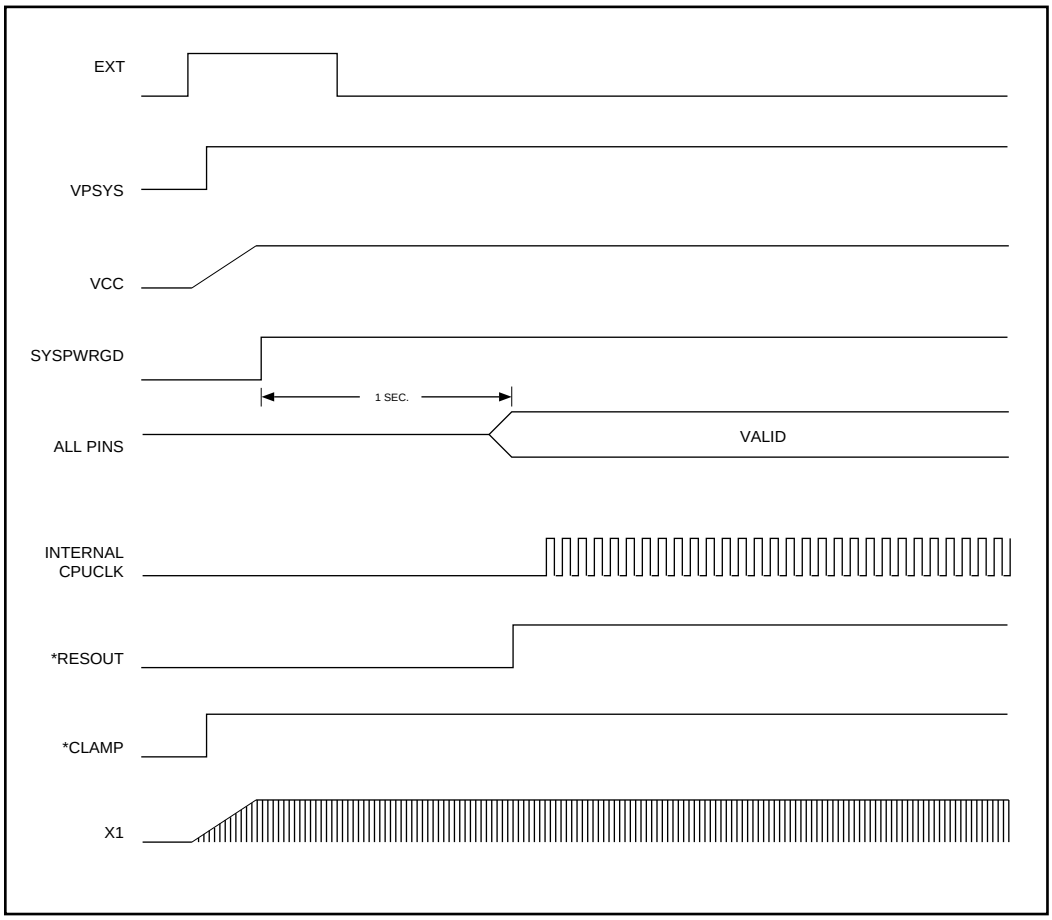
LCD Power Control - VPLCD and VPBIAS

LCDs are typically powered by two power sources. A main VCC and a negative BIAS voltage. Proper sequencing of the power sources and the control signal are required to prevent damage to the LCD panel. The PMU provides automatic power sequencing of the LCD panel during all power up/down phases and power management modes.

PC Card Power Control - VPCRD, VPPENA and VPPENB

There are three power controls for the PC card interface. VPCRD controls the VCC power to both card slots. VPPENA and VPPENB control programming power to slots A and B. To prevent damage to the PC cards, the designer should insure that when VPCRD is not active, VPPENA and VPPENB cannot enable programming power to the PC cards. Sources for programmable PC card voltage generators include Maxim and Linear Technology.

Power On Sequence Figure



SNEPWRGD and SYSPWRGD

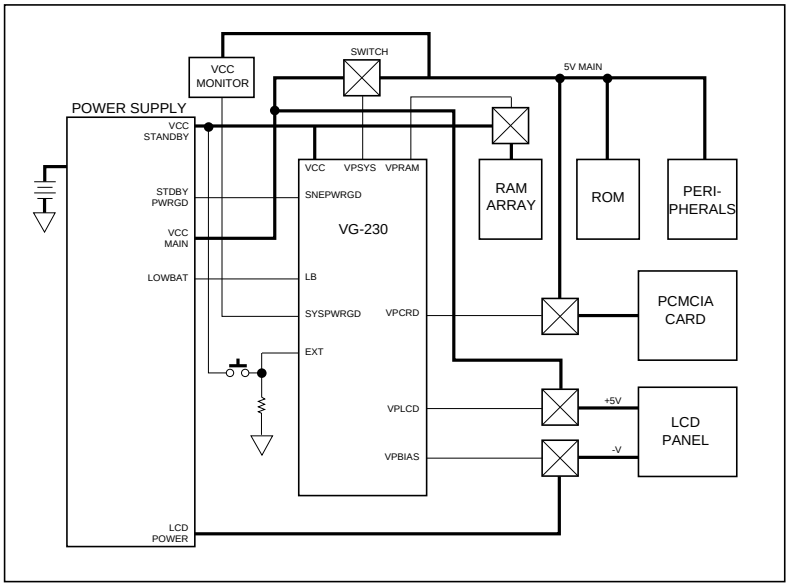
The VG230 provides two power-good inputs. These inputs inform the VG230 when the operating power is stabilized. The SNEPWRGD input is a high true input that is driven when the power to the VG230 has stabilized. This input is used as the initial power-good signal and is used to reset all internal registers, the Real Time Clock, CPU and all peripherals. SNEPWRGD is usually only at a low state when the batteries are being changed or have been depleted.

The second power good input, SYSPWRGD, is used to inform the VG230 that the system power is good and that the system is ready for operation. SYSPWRGD is used to initialize the external system peripherals, via the *RESOUT signal, and re-start the VG230 clocks. Unexpected loss of SYSPWRGD forces VG230 into OFF mode. See the Power On Sequence Figure for power up sequence of the VG230.

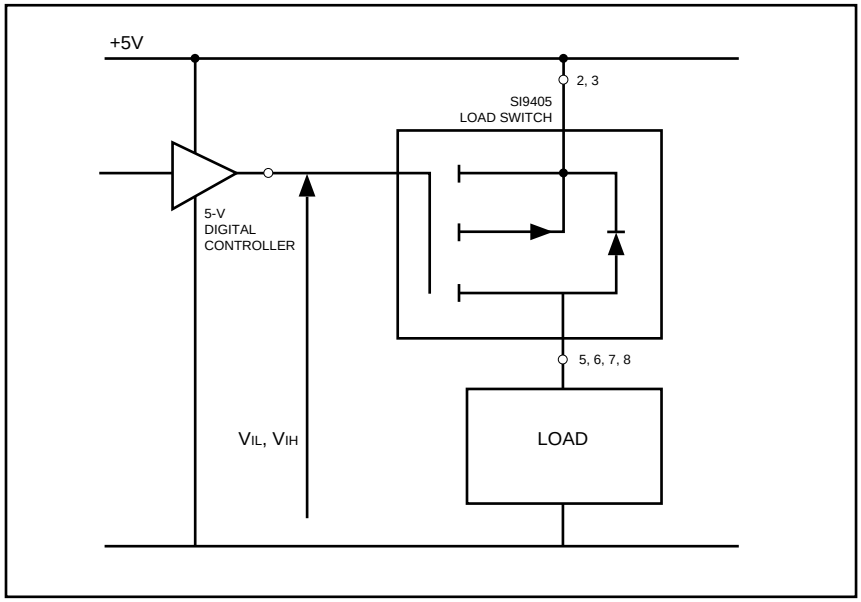
Power Switching

There are several off-the-shelf solutions for switching power to peripheral devices ranging from relays to MOSFETs. For portable system design, one solution is the Littlefoot family of MOSFET switches from Siliconix. These are high side switches in 8 pin SO packages which can be directly controlled by the VG230's power control pins. Note that the processor must be running code to change the polarity of the VPSYS and VPRAM power control pins. Therefore if a Littlefoot device is being used to control the system or RAM power, the solution requires default polarity and an external hardware inverter on the control signal.

Power Supply Interface Figure



Load Switch Example Figure



Load Switch Truth Table V+ = 5.0 V, $T_A = 25^{\circ}C$			
Input	Min V_{IH} (V)	Min V_{IL} (V)	Status of Load
0		0.5	On
1	4.5		Off

Expansion

The VG230 implements a standard 8 bit ISA expansion bus. Standard MRD, MWR, IORD, and IOWR signals provide strobes for memory and I/O devices. Data is gated onto the D[7:0] lines and address lines A[9:0] provide address information.

The ISA bus is provided as a means for adding a small amount of custom I/O in a closed system. The VG230 was not designed to directly drive the heavy loads typically associated with a backplane; therefore address and data bus buffering is required in applications where the end user can install commercially available XT bus cards.

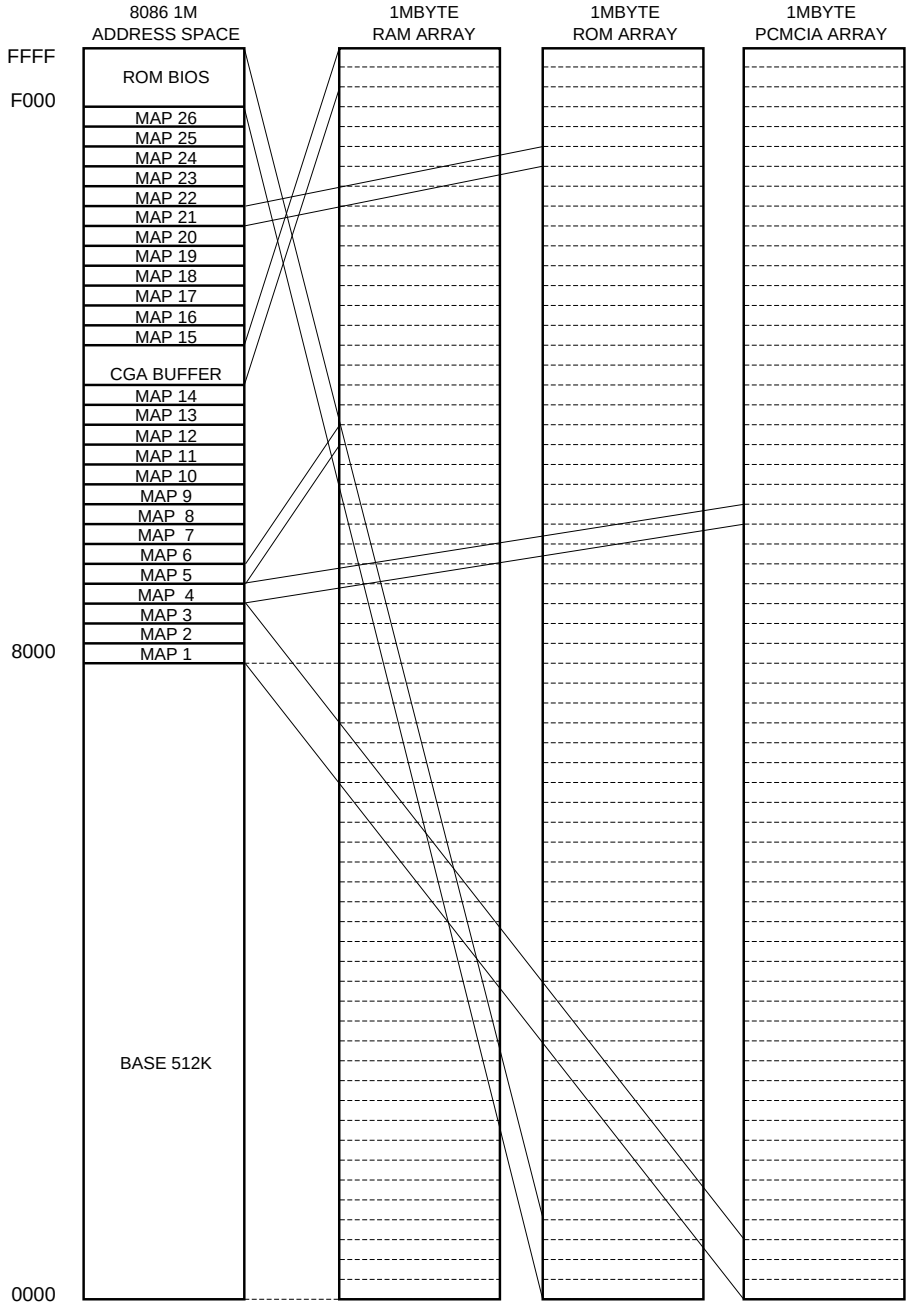
Memory Mapping

On the following page the three blocks to the right represent the three types of physical memory available. The base 512K of 8086 address space is always mapped to the bottom of the RAM array. The 32K bytes of CGA BUFFER is always mapped to the top 32K bytes of the RAM array. The ROM BIOS (64K bytes) is always mapped to the bottom 64K of the heavy access ROM array (ROMCE0).

Memory Mapping Examples

The following example illustrates the flexibility built into the VG230 memory manager. The Power Supply Interface Figure represents a memory design based on a medium sized VG230 system. This system is based on 1M byte of ROM for BIOS and DOS. 1M byte of RAM and a 1Mbyte PCMCIA card for applications code. The block to the left represents the 1Mbyte address space of the 8086.

Memory Mapping (example) Figure



Flash ROM Support

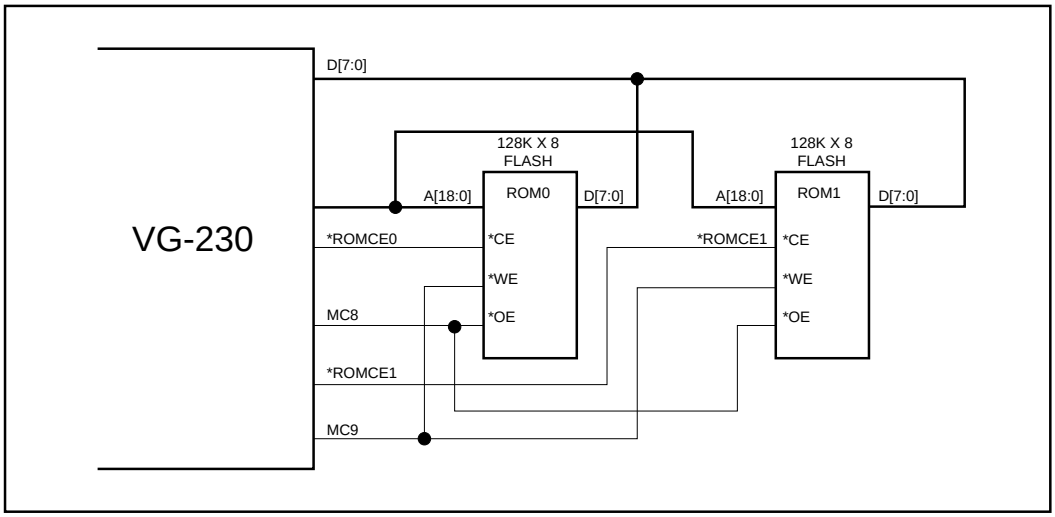
The VG230 can support FLASH EPROM in its ROM, in its main memory or in both. A FLASH programming voltage generator (VPP) and associated control are required. Control of the VPP voltage can be supplied through one of the GPIO pins. It is up to the BIOS, driver or application software to supply the necessary programming algorithm to program the FLASH devices. When using FLASH EPROM in the ROM array, it must be of the same data width as all other ROMs/EPROMs connected to its chip-enable (*ROMCE0 or *ROMCE1). The FLASH EPROM must also be no wider then the main memory array. Memory writes to any ROM address automatically generate a modified MWR strobe that is compatible with FLASH.

When FLASH ROM is used in the main memory array, it must be of the same size and data width as the RAM devices. DRAM cannot be mixed with FLASH because its addressing method is fundamentally incompatible with FLASH's row/column addressing. The VG230 reads the BANK bits of the Memory Control 1 Register (04H) in order to position video memory at the top of the main memory array. Therefore, FLASH, if used, must be placed above the top bank of RAM and the BANK bits set so as not to include the FLASH. For example, if a system has two banks of PSRAM, FLASH can be located in banks 3 and above. The BANK bits must be programmed to the binary value corresponding to one less than the number of PSRAM banks (2-1=1 or 001).

The following table illustrates the definitions of MC[9:6] for the various memory combinations:

System Configuration	**MC6**	**MC7**	**MC8**	**MC9**
8 bit RAM, 8 bit ROM			*OE	*WE
8 bit RAM, 16 bit ROM			*OEL	*OEH
16 bit RAM, 8 bit ROM (power on default)			*OE	*WE
16 bit RAM, 16 bit ROM (power on default)	*OEL	*OEH	*WEL	*WEH
8 bit DRAM, 8 bit ROM			*OE	*WE
8 bit DRAM, 16 bit ROM			*OEL	*OEH
16 bit DRAM, 8 bit ROM			*OE	*WE
16 bit DRAM, 16 bit ROM		*OE	*WEL	*WEH
x16 DRAM/ ROM			*OE	*WE

128 X 8 Flash ROM Interface Figure

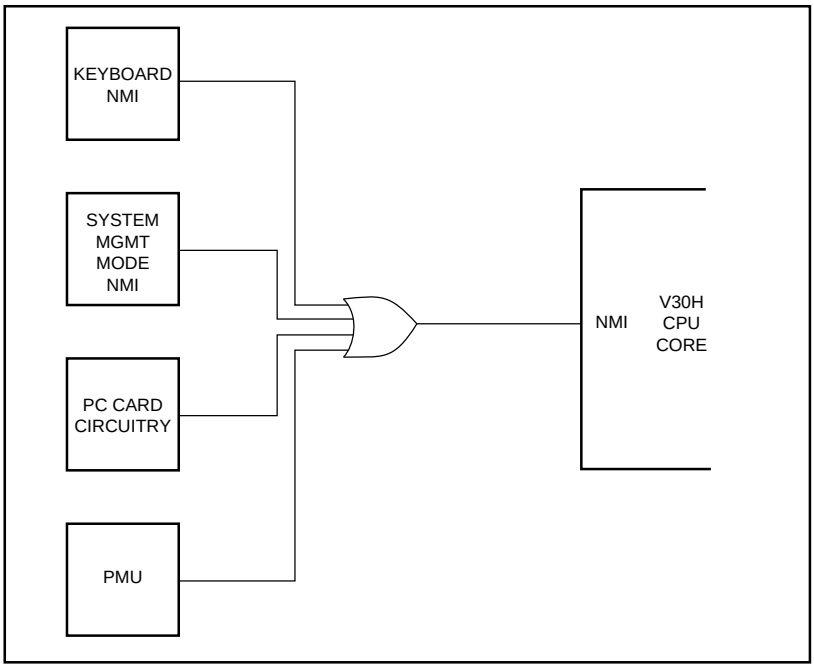


Non-Maskable Interrupts and System Management Mode (SMM)

The VG230 uses Non-Maskable Interrupts (NMI) to provide enhancements to the standard PC architecture. These enhancements include:

- Power Management
- Internally scanned keyboard
- System Management Mode (SMM)

NMI Distribution Figure



There are several NMI sources within the VG230. When an NMI occurs the NMI handler can determine the source of the NMI by first reading the Main NMI Status Register located at index 19H. The method of clearing the NMI depends on the source of the NMI.

ICE Support

The VG230 supports standard in-circuit emulation to simplify debugging of system motherboards. Any available ICE which is compatible with the VEC V30HL may be used. An ICE adaptor board (Vadem part no. VG230-ICE) connects between the system motherboard and the ICE. This arrangement brings out the local V-30 processor bus to the ICE without changing the standard VG230 pinout or functionality.

NOTES

REGISTER DESCRIPTION

NOTES 

REGISTER OVERVIEW

IBM compatible registers and peripherals are located at the standard addresses. Internal registers specific to the VG230 Single-Chip PC Platform are accessed via an Index Register located at 026H, and are read or written through a Data Register located at 027H.

VG230 I/O Map Table

Register / Peripheral			I/O Address
8237 DMA Controller			000H - 00FH
8259 Interrupt Controller			020H - 021H
VG230 Single-Chip PC Platform Index Register			026H
VG230 Single-Chip PC Platform Data Register			027H
8254 Timer			040H - 043H
XT PPIB Keyboard Data Register			060H
XT PPIB Keyboard Control			061H
XT PPIC System Status			062H
Memory Map Address Register			06CH
Memory Map Data Registers			06EH - 06FH
DMA Page Registers			081H - 083H
XT NMI Mask Register			0A0H
	Data	**Status**	**Control**
Parallel Port Data, Status and Control Registers	170H	171H	172H
	278H	279H	27AH
	378H	379H	37AH
	3BCH	3BDH	3BEH
Serial Port			2F8H - 2FFH
			3F8H - 3FFH
CGA LCD Controller			3D0H - 3DFH

VG230 Register Descriptions

Name: **PC/XT Compatible DMA Controller Registers**
Type **Read/Write**
Index: **000H-00FH**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Default	Function
D[7:0]		(See 8237 Data Sheet for descriptions of register bits)

Name: **PC/XT Compatible Interrupt Controller Registers**
Type **Read/Write**
Index: **020H-021H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Default	Function
D[7:0]		(See 8259 Data Sheet for descriptions of register bits)

Name: **Index Register**
Type **Read/Write**
Index: **026H**

D7	D6	D5	D4	D3	D2	D1	D0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Bit	Default	Function
D[7:0]	00H	Data register address bits.

Name: **Data Register**
Type **Read/Write**
Index: **027H**

D7	D6	D5	D4	D3	D2	D1	D0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Bit	Default	Function
D[7:0]	00H	Data read from or written to register addressed by VG230 Single-Chip PC Index Register.

Name: **PC/XT Compatible Timer/Counter Registers**
Type **Read/Write**
Index: **040H-043H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Default	Function
D[7:0]		(See 8237 Data Sheet for descriptions of register bits)
Note: When initializing the 8254 timer following a hard reset, channel 2 must be initialized before channel 0 (Tier Interrupt) or channel 1 (Memory Refresh) will operate.		

Name: **PC/XT Compatible PPIA Keyboard Data Register**
Type **Read/Write**
Index: **060H**

D7	D6	D5	D4	D3	D2	D1	D0
KSC7	KSC6	KSC5	KSC4	KSC3	KSC2	KSC1	KSC0

Bit	Default	Function
D[7:0]	00H	Keyboard Scan Code. Normally, the PC/XT keyboard data register is read only. This register is written by the BIOS with the translated keyboard scan code when the Keyboard Controller is programmed into the keyboard scan mode. When the *KBDENA bit of the Keyboard Mode Register is set high, this register is disabled. In this configuration, accesses to this register will be directed to the external bus D[15:0].

Name: **PC/XT Compatible PPIB Keyboard Control Register**
Type **Read/Write**
Index: **061H**

D7	D6	D5	D4	D3	D2	D1	D0
RSTKBD	KCLKEN	*IOCEN	*PAREN	HISWS	Spare	SPKDAT	TGATE

Bit	Default	Function
D7	0	0 - Enable Keyboard 1 - Clear Keyboard Data Port and IRQ1
D6	0	0 - Force Keyboard Clock Low 1 - Enable Keyboard Clock
KCLKEN is pulsed low by software to request that the keyboard perform diagnostics. In the keyboard scan mode, KCLKEN may be used to generate an NMI. Following a write to the PPIB port with the KCLKEN bit reset low, an NMI will be generated on the next write to the PPIB port with the KCLKEN bit set high. At this time the BIOS will perform a keyboard scan operation and return the results to the PPIA port.		
D5	0	0 - Enable I/O Channel Parity. 1 - Disable I/O Channel Parity.
D4	0	1 - Disable RAM Parity.
D3	0	0 - Enable System Switches SW1 - SW4. 1 - Enable System Switches SW5 - SW8.
D2	0	Spare Read/Write bit.
D1	0	0 - Disable Speaker Output. 1 - Enable Speaker Output.
D0	0	0 - Disable Timer Channel 2. 1 - Enable Timer Channel 2.

D7	D6	D5	D4	D3	D2	D1	D0
PARERR	IOERR	TOUT2	*SPKR	SW4_8	SW 3_7	SW 2_6	SW 1_5

Name: **PC/XT Compatible PPIC System Status Register**
Type **Read Only**
Index: **062H**

Bit	Default	Function
D7	0	Onboard Parity Status. (Forced low to indicate NO RAM Parity Errors)
D6	0	I/O Channel Parity Status. (Forced low to indicate NO I/O Channel Parity Errors)
D5	X	State of 8254 TOUT2. (Speaker Clock)
D4	1	Inverted state of the SPKR output pin. 0 - Speaker is ON. 1 - Speaker is OFF.
D3	1	SW4 - RAM Size High. (Hardwired High) SW8 - Drive Count High. (Set by bit in Keyboard Mode Register)
D2	1	SW3 - RAM Size Low. (Hardwired High) SW7 - Drive Count Low. (Set by bit in Keyboard Mode Register)
D1	0	SW2 - Coprocessor Installed. (Hardwired High) SW6 - Display High. (Set by bit in Keyboard Mode Register)
D0	1	SW1 - Loop on POST. (hardwired High) SW5 - Display Low. (Set by bit in Keyboard Mode Register)

Memory Mapping Register Description Table

Map register 1 - 80H 8000:0 - 83FF:F	Map register 14 - B4H B400:0 - B7FF:F
Map register 2 - 84H 8400:0 - 87FF:F	Map register 15 - C0H C000:0 - C3FF:F
Map register 3 - 88H 8800:0 - 8BFF:F	Map register 16 - C4H C400:0 - C7FF:F
Map register 4 - 8CH 8C00:0 - 8FFF:F	Map register 17 - C8H C800:0 - CBFF:F
Map register 5 - 90H 9000:0 - 93FF:F	Map register 18 - CCH CC00:0 - CFFF:F
Map register 6 - 94H 9400:0 - 97FF:F	Map register 19 - D0H D000:0 - D3FF:F
Map register 7 - 98H 9800:0 - 9BFF:F	Map register 20 - D4H D400:0 - D7FF:F
Map register 8 - 9CH 9C00:0 - 9FFF:F	Map register 21 - D8H D800:0 - DBFF:F
Map register 9 - A0H A000:0 - A3FF:F	Map register 22 - DCH DC00:0 - DFFF:F
Map register 10 - A4H A400:0 - A7FF:F	Map register 23 - E0H E000:0 - E3FF:F
Map register 11 - A8H A800:0 - ABFF:F	Map register 24 - E4H E400:0 - E7FF:F
Map register 12 - ACH AC00:0 - AFFF:F	Map register 25 - E8H E800:0 - EBFF:F
Map register 13 - B0H B000:0 - B3FF:F	Map register 26 - ECH EC00:0 - EFFF:F

Name: **Map Address Register**
Type **Read/Write**
Index: **06CH**

D7	D6	D5	D4	D3	D2	D1	D0
PA7	PA6	PA5	PA4	PA3	PA2	N/U	N/U

Bit	Default	Function
D[7:2]	00H	Page address of the Mapping register to access through the Map Data registers. Valid entries are: 80, 84, 88 & 8C 90, 94, 98 & 9C A0, A4, A8, & AC B0 & B4 C0, C4, C8, & CC D0, D4, D8, & DC E0, E4, E8, & EC
D[1:0]	0	Not used. Ignored when written and zero when read.

Name: **Map Low Byte Data Register**
Type **Read/Write**
Index: **06EH**

D7	D6	D5	D4	D3	D2	D1	D0
MAP21	MAP20	MAP19	MAP18	MAP17	MAP16	MAP15	MAP14

Bit	Default	Function
D[7:0]	00H	Least significant byte of the memory map address.

Name: **Map High Byte Data Register**
Type **Read/Write**
Index: **06FH**

D7	D6	D5	D4	D3	D2	D1	D0
PEN	DTYP2	DTYP1	DTYP0	MAP25	MAP24	MAP23	MAP22

Bit	Default	Function			
D7	0	0 - Disable mapping for this page. 1 - Enable mapping for this page.			
D[6:4]	000	DTYP2	DTYP 1	DTYP0	Page Memory Device Type
		0	0	0	None (external bus cycle)
		0	0	1	RAM (specified by MTYP[3:0]
		0	1	0	ROM #0
		0	1	1	ROM #1
		1	0	0	PC Card A
		1	0	1	PC Card B
		1	1	0	Reserved
		1	1	1	Reserved
D[3:0]	0H	Most significant nibble of memory map address.			

Name: **PC/XT Compatible DMA Page Registers**
Type **Read/Write**
Index: **081H-083H**

D7	D6	D5	D4	D3	D2	D1	D0
N/U	N/U	N/U	N/U	A19	A18	A17	A16

Bit	Default	Function
D[7:4]	0H	Not used.
D[3:0]	0H	DMA memory page address. I/o port address as follows: Channel 1: 083H Channel 2: 081H Channel 3: 082H

Name: **PC/XT Compatible NMI Mask Register**
Type **Read/Write**
Index: **0A0H**

D7	D6	D5	D4	D3	D2	D1	D0
NMIENA	N/U	N/U	N/U	N/U	N/U	N/U	N/U

Bit	Default	Function
D7	0	0 - Disable NMIs. 1 - Enable NMIs.
D[6:0]	00H	Not used.

Name: **PC/XT Compatible Parallel Port Data Register**
Type **Read/Write**
Index: **170H, 278H, 378H, or 3BCH**
(Depending on setting of PPSEL bits of PIO mode Register, Index 18H, & KBDMODE bit of Keyboard Mode Register, Index 08H)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Bit	Default	Function
D[7:0]	00H	**Parallel Data.** In uni-directional mode, during reads from the Parallel Port Data Register, data is sourced from the PD[7:0] bits. During writes, data is captured in both this register and an external octal "D" type F/F controlled by the PDCLK pin. In bi-directional mode, the BIDIR bit of the PIO mode register (18H) is set high. The PPDIR bit of the Parallel Port Control Register determines the source of the data read from this port. When the PPDIR bit is low, data is read from the internal source. When PPDIR is high, the external parallel port data is read.

Name: **PC/XT Compatible Parallel Port Status Register**
Type **Read Only**
Index: **171H, 279H, 379H, or 3BDH**
(Depending on setting of PPSEL bits of PIO mode Register, Index 18H & KBDMODE bit of Keyboard Mode Register, Index 08H)

D7	D6	D5	D4	D3	D2	D1	D0
*BUSY	*ACK	PE	SEL	*ERROR	IRQSTA	N/U1	N/U0

Bit	Default	Function
D7	X	Inverted state of the BUSY input pin.
D6	X	Driven directly from the *ACK input pin.
D5	X	Driven directly from the PE input pin.
D4	X	Driven directly from the SEL input pin.
D3	X	Driven directly from the *ERR input pin.
D2	0	Interrupt Status. 1 - PIO Interrupt Pending.
D[1:0]	00	Not used. Always read back Low.

Name: **PC/XT Compatible Parallel Port Control Register**
Type **Read/Write**
Index: **172H, 27AH, 37AH, or 3BEH**
(Depending on setting of PPSEL bits of PIO mode Register, Index 18H & KBDMODE bit of Keyboard Mode Register, Index 08H)

D7	D6	D5	D4	D3	D2	D1	D0
N/U7	N/U6	PPDIR	IRQENA	SELECT	*INIT	AUTOFD	STROBE

Bit	Default	Function
D[7:6]	000	Not Used. Ignored when written and Zero when read.
D5	0	Parallel Port direction control. When the BIDIR bit of the PIO Mode register (18H) is set high, the parallel port is configured for bi-directional operation and this bit is used to externally control the OE of the printer data latch and read-back path as follows: 0 - Write data to external parallel I/O device. (PDOE output driven low) 1 - Read data from external parallel I/O device. (PDOE output driven high) This bit is a don't care when the DIDIR bit is reset low.
D4	0	PIO Interrupt Enable. 1 - Enabled. 0 - Disabled.
D3	0	Inverted and drives *SLCT output pin.
D2	0	Directly drives *INIT output pin.
D1	0	Inverted and drives *AFD output pin.
D0	0	Inverted and drives *STB output pin.

Care must be taken to prevent the printer device from sourcing current into the VG230-based system. When selecting parallel data and control drivers, the designer must insure that a high level on any I/O lines will not be gated onto the system power bus. The designer must insure that the logic family used to interface to the external parallel printer device be latchup proof. The VG230 parallel printer inputs are designed to avoid such a problem.

Name: **8250 Serial Port Registers**
Type **Read/Write**
Index: **2F8H, 2FFH, 3F8H, or 3FFH**
(Depending on setting of SPSEL bit of SIO mode Register (10H))

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Default	Function
D[7:0]		See 8250 Data Sheet for register definitions.

Following is the list of indexed registers specific to the VG230 Single-Chip PC Platform:

VG230 Indexed Register Summary Table

REGISTER	INDEX
Revision Register	00H
Bus Cycle Generator Mode Register	01H
Bus Cycle Generator Wait State Control 1 Register	02H
Bus Cycle Generator Wait State Control 2 Register	03H
Memory Control 1 Register	04H
Memory Control 2 Register	05H
Alt. Display Buffer Start Address Register	06H
LCD Configuration Control Register	07H*
Keyboard Mode Register	08H
Keyboard Scan Control Register	09H
Keyboard Return Status Low Register	0AH
Keyboard Return Status High Register	0BH
Keyboard Shift and NMI Status Register	0CH
ICU Mode Register	0DH
DMA Mode Register	0EH
SIO Mode Register	10H
SIO Power Control Register	11H
Timer Mode Register	13H
PIO Mode Register	18H
Main NMI Status Register	19H
Port 1 NMI Trap Address Low Register	1AH
Port 1 NMI Trap Address High Register	1BH
Port 2 NMI Trap Address Low Register	1CH
Port 2 NMI Trap Address High Register	1DH

REGISTER	INDEX
Port 3 NMI Trap Address Low Register	1EH
Port 3 NMI Trap Address High Register	1FH
PC Card Controller Mode Register	20H
PC Card Slot 0 Control Register	21H
PC Card Slot 0 Status Register	22H
PC Card Slot 0 Interrupt Mask Register	23H
PC Card Slot 0 I/O High Address Register	24H
PC Card Slot 0 I/O Low Address Register	25H
PC Card Slot 0 I/O Address Range Register	26H
PC Card Slot 1 Control Register	27H
PC Card Slot 1 Status Register	28H
PC Card Slot 1 Interrupt Mask Register	29H
PC Card Slot 1 I/O High Address Register	2AH
PC Card Slot 1 I/O Low Address Register	2BH
PC Card Slot 1 I/O Address Range Register	2CH
PC Card Power Control Register	2DH
PC Card Activity Timer Register	2EH
Reserved	2FH
BIOS Time Base Low Register	30H
BIOS Time Base High Register	31H
GPIO Mode Register	32H
GPIO Control Register	33H
Reserved	34H - 6FH
Top of Memory Register	38H
ICU Shadow Register	40H
RTC Seconds Register	70H
RTC Minutes Register	71H
RTC Hours Register	72H
RTC Day Low Register	73H
RTC Day High Register	74H
RTC Alarm Seconds Register	75H
RTC Alarm Minutes Register	76H
RTC Alarm Hours Register	77H
RTC Alarm Day Register	78H
RTC Mode Register	79H
RTC Status Register	7AH
Reserved	7BH - 7FH
RTC CMOS RAM	80H - BFH
PMU Status Register	C0H
PMU Supply Register	C1H
PMU Control Register	C2H
PMU Activity Mask Register	C3H
PMU NMI Mask Register	C4H

REGISTER	INDEX
PMU I/O Range Register	C5H
PMU Power On Register	C6H
PMU Power Doze Register	C7H
PMU Power Sleep Register	C8H
PMU Power Suspend Register	C9H
PMU Polarity Register	CAH
PMU Output Register	CBH
PMU Doze Timer Register	CCH
PMU Sleep Timer Register	CDH
PMU Suspend Timer Register	CEH
PMU LCD Timer Register	CFH
LCD Sequence Register	D4H
PMU Resume Status	DAH
PMU Activity Status Register	DBH
Reserved	
***Note:** Additional indexed registers have been added to the "6845" in the CGA space to support LCD operation.*	

Revision Register

The VG230 contains a revision register to identify versions of the silicon. This register is accessed through the index register at index 00H. Contact Vadem for information regarding version identification.

Name: **Revision Register**
Type **Read Only**
Index: **00H**

D7	D6	D5	D4	D3	D2	D1	D0
REVD7	REVD6	REVD5	REVD4	REVD3	REVD2	REVD1	REVD0

Bit	Default	Function
D[7:0]		VG230 Single-Chip PC Platform Silicon Revision Number.

Name: **Bus Cycle Generator Mode Register**
Type **Read/Write**
Index: **01H**

D7	D6	D5	D4	D3	D2	D1	D0
CDIV2	CDIV1	CDIV0	CLK14/*16	LTCHADR	BINH	SDIV1	SDIV0

Bit	Default	Function			
D[7:5]	010	CDIV2	CDIV1	CDIV0	CPUCLK Divisor
		0	0	0	CPUOSC/2
		0	0	1	CPUOSC/3
		0	1	0	CPUOSC/4 default
		0	1	1	CPUOSC/6
		1	0	0	CPUOSC/8
		1	0	1	Reserved
		1	1	0	Reserved
		1	1	1	Reserved
D4	0	0 - Max. CPUCLK frequency = 16MHz. (32MHz input clock) 1 - Max. CPUCLK frequency = 14.3MHz. (28.6MHz input clock)			
D3	0	0 - Disable A[25:0] latches. A[25:0] valid for all CPU cycles. 1 - Enable A[25:0] latches A[25:11] invalid for DRAM c ycles and A[25:20] only valid for PC Card or ROM1 cycles.			
D2	0	0 - Enable external bus for all bus cycles. 1 - Disable external bus during accesses to internal devices.			
D[1:0]	10	SDIV1	SDIV0	SYSCLK Divisor	
		0	0	CPUCLK/4	
		0	1	CPUCLK/3	
		1	0	CPUCLK/2 default	
		1	1	CPUCLK	

***NOTE**: LTCHADR shoud be set to 0 if not using upper address to save power.*
SDIV[1:0] changes the speed of I/O processing.

Name: **Bus Cycle Generator Wait State Control 1 Register**
Type **Read/Write**
Index: **02H**

D7	D6	D5	D4	D3	D2	D1	D0
ROMW1	ROMW0	RAMW1	RAMW0	IOW1	IOW0	EXMW1	EXMW0

Bit	Default	Function		
D[7:6]	11	ROMW1	ROMW0	ROM Wait States
		0	0	0 CPUCLK Wait States
		0	1	1 CPUCLK Wait States
		1	0	2 CPUCLK Wait States
		1	1	3 CPUCLK Wait States
D[7:6]	01	RAMW1	RAMW0	RAM Wait States
		0	0	0 CPUCLK Wait States
		0	1	1 CPUCLK Wait States
		1	0	2 CPUCLK Wait States
		1	1	3 CPUCLK Wait States
D[3:2]	01	IOW1	IOW0	I/O Wait States
		0	0	0 SYSCLK Wait States
		0	1	1 SYSCLK Wait States
		1	0	2 SYSCLK Wait States
		1	1	3 SYSCLK Wait States
D[1:0]	00	EXMW1	EXMW0	Expansion Memory Wait States
		0	0	0 SYSCLK Wait States
		0	1	1 SYSCLK Wait States
		1	0	2 SYSCLK Wait States
		1	1	3 SYSCLK Wait States

Name: **Bus Cycle Generator Wait State Control 2 Register**
Type **Read/Write**
Index: **03H**

D7	D6	D5	D4	D3	D2	D1	D0
PCAW2	PCAW1	PCAW0	Reserved	PCBW2	PCBW1	PCBW0	PCIODLY

Bit	Default	Function			
D[7:5]	111	PCW2	PCW 1	PCW 0	PC Card 'A' Wait States
		0	0	0	0 CPUCLK Wait States
		0	0	1	1 CPUCLK Wait States
		0	1	0	2 CPUCLK Wait States
		0	1	1	3 CPUCLK Wait States
		1	0	0	4 CPUCLK Wait States
		1	0	1	5 CPUCLK Wait States
		1	1	0	6 CPUCLK Wait States
		1	1	1	7 CPUCLK Wait States
D4	0	Reserved for future use.			
D[3:1]	111	PC Card 'B' Wait States. Decoding is same as for PC Card 'A'.			
D0	0	0 - No I/O command delay. 1 - PC Card I/O Command Delay one Bus Clock (SYSCLK) cycle.			

Name: **Memory Control 1 Register**
Type **Read/Write**
Index: **04H**

D7	D6	D5	D4	D3	D2	D1	D0
MAPEN	BANK2	BANK1	BANK0	MTYP3	MTYP2	MTYP1	MTYP0

Bit	Default	Function				
D7	0	0 - Disable Memory Mapping. 1 - Enable Memory.				
D[6:4]	111	BANK2	BANK 1	BANK 0	No. of RAM Banks Installed	
		0	0	0	1	
		0	0	1	2	
		0	1	0	3	
		0	1	1	4	
		1	0	0	5	
		1	0	1	6	
		1	1	0	7	
		1	1	1	8	
		Note: FLASH banks can be installed above SRAM or PSRAM banks as long as data widths and device sizes are consistent. In this case, the BANK setting must not include the number of FLASH banks.				
D[3:0]	0H	MTYP3	MTYP2	MTYP1	MTYP0	Density and Type
		0	0	0	0	32K x 8 SRAM
		0	0	0	1	128K x 8 SRAM
		0	0	1	0	512K x 8 SRAM
		0	0	1	1	32K x 8 PSRAM
		0	1	0	0	128K x 8 PSRAM
		0	1	0	1	512K x 8 PSRAM
		0	1	1	0	256K x 1/4 DRAM
		0	1	1	1	512K x 8 DRAM
		1	0	0	0	1M x 1/4 DRAM
		1	0	0	1	4M x 1/4 DRAM
		1	0	1	0	256K x 16 DRAM
		1	0	1	1	Reserved for future use
		1	1	X	X	

Name: **Memory Control 2 Register**
Type **Read/Write**
Index: **05H**

D7	D6	D5	D4	D3	D2	D1	D0
RAMSIZ	ROM0SIZ	ROM1SIZ	SLWREF	SRFDRAM	Reserved	*ROMOE	*MRASDLY

Bit	Default	Function
D7	0	0 - RAM is 16 bits wide. 1 - RAM is 8 bits wide.
D6	X	Read Only bit reflecting state of ROM8/*16 pin. 0 - BIOS ROM is 16 bits wide. 1 - BIOS ROM is 8 bits wide
D5	1	0 - Option ROM is 16 bits wide. 1 - Option ROM is 8 bits wide.
D4	0	0 - Normal Refresh Rate DRAM. *(Only applies during SUSPEND)* 1 - Slow Refresh Rate DRAM. *(Only applies during SUSPEND)*
D3	0	1 - Self Refresh DRAM. During Suspend, CAS before RAS cycles are not generated. Refresh is performed by DRAM.
D2	0	Reserved for future use.
D1	0	ROM Output Enable Function. 0 - Enable ROMOE Function. 1 - Disable ROMOE Function.
D0	0	0 - Delay mapper memory cycles until CPU T3 state. 1 - Begin mapper memory cycles at CPU T2 state.

Name: **Alternate Display Buffer Start Address Register**
Type **Read/Write**
Index: **06H**

D7	D6	D5	D4	D3	D2	D1	D0
ALTDBREN	DBA21	DBA20	DBA19	DBA18	DBA17	DBA16	DBA15

Bit	Default	Function
D7	0	Alternate Display Buffer Refresh Enable. 0 - Use top 32 Kbytes of upper memory bank for LCD Controller display refresh operations. 1 - Use 32 Kbytes beginning at offset into upper memory bank specified by DBA[21:15] for LCD Controller display refresh operations.
D[6:0]	0	Alternate Display Buffer Start Address.

Name: **LCD Configuration Control Register**
Type **Read/Write**
Index: **07H**

D7	D6	D5	D4	D3	D2	D1	D0
*ENALCD	VIDSPD1	VIDSPD0	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Default	Function
D7	0	Sub-Notebook Engine LCD Enable/Disable Bit. 0 - Enable SNE LCD Controller. 1 - Disable SNE LCD Controller.
D[6:5]	00	These bits determine the access speed of system RAM during video refresh cycles as follows: VIDSPD1 VIDSPD0 Clocks per video cycle 0 0 4-8 bit RAM/5-16 bit RAM (normal) 0 1 5-8 bit RAM/6-16 bit RAM (slow) 1 0 3-8 bit RAM/4-16 bit RAM (fast) 1 1 Reserved.
D[4:0]	0H	Reserved for future use.

Name: **Keyboard Mode Register**
Type **Read/Write**
Index: **08H**

D7	D6	D5	D4	D3	D2	D1	D0
SW8	SW7	SW6	SW5	KBDMODE	*KBDENA	SCLK1	SCLK0

Bit	Default	Function
D[7:4]	0H	Software programmable bits used to select the setting of system switches SW[8:5] (display type and floppy drive count).
D3	0	0 - Select Keyboard Scanner pin configuration. 1 - Redefine Keyboard Scanner pins.
D2	0	0 - Enable PC/XT serial keyboard I/F. 1 - Disable PC/XT serial keyboard I/F. Only meaningful when Keyboard Scanner pins are redefined (KBDMODE=1). Setting *KBDENA high directs port 60H accesses to the external data bus D[15:0] and further redefines KBDAT pin as IRQ1.
D[1:0]	00	SCLK1 SCLK0 NMI Scan Rate 0 0 51.2Hz 0 1 64Hz 1 0 85.3Hz 1 1 128Hz

The Scan Control register is used when the VG230 is configured to use the internal keyboard scanner.

Name: **Keyboard Scan Control Register**
Type **Read/Write**
Index: **09H**

D7	D6	D5	D4	D3	D2	D1	D0
S7	S6	S5	S4	S3	S2	S1	S0

Bit	Default	Function
D[7:0]	00H	SCAN[7:0] output enabled. 0 - Associated SCAN[7:0] pin is driven Hi-Z. 1 - Associated SCAN[7:0] pin driven low.
Note: *In PC/XT serial I/F mode the Keyboard Scan logic is disabled (S[7:0] forced low) allowing the SCAN[7:0] output buffers to be controlled by other logic.*		

S[7:0] are sequentially set high during an active keyboard scan. The Return Status registers are checked to determine if a key has been pressed. The rate at which the keyboard is scanned is determined by the setting of SCLK[1:0] in the keyboard Mode register.

When the keyboard scan completes without finding that a key has been pressed, S[7:0] are all set high. Thereafter, if a key is pressed, an NMI is generated and the keyboard scan routine begins again.

The Return Status Low Register is used to read the status of the RET[7:0] inputs.

Name: **Keyboard Return Status Low Register**
Type **Read/Write**
Index: **0AH**

D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	R3	R2	R1	R0

Bit	Default	Function
D[7:0]	FFH	RET[7:0] input status. 0 - Associated RET[7:0] switch position is closed. 1 - Associated RET[7:0] switch position is open.
Note: *In PC/XT serial I/F mode this register is ignored.*		

The bits in this register reflect the state of the RET[7:0] inputs. A low indicates the corresponding RET[7:0] switch position is closed. A high indicates the corresponding RET[7:0] switch position is open. This register should be ignored when the VG230 is configured for the PC/XT serial keyboard interface.

The Return Status High Register is used to read the status of four of the five Shift key inputs, SHFT[3:0] and the status of RET[11:8]

Name: **Keyboard Return Status High Register**
Type **Read Only**
Index: **0BH**

D7	D6	D5	D4	D3	D2	D1	D0
SH3	SH2	SH1	SH0	R11	R10	R9	R8

Bit	Default	Function
D[7:4]	FH	SHFT[3:0] input status. 0 - Associated SHFT[3:0] switch position is closed. 1 - Associated SHFT[3:0] switch position is open.
D[3:0]	FH	RET[11:8] input status. 0 - Associated RET[11:8] switch position is closed. 1 - Associated RET[11:8] switch position is open.
Note: *In PC/XT serial I/F mode this register is ignored.*		

The bits in this register reflect the state of the SHFT[3:0] and RET[11:8] input pins. A low on SH[3:0] indicates the corresponding SHFT[3:0] switch position is closed. A high indicates the SHFT[3:0] switch position is open. A low on R[11:8] indicates the corresponding RET[11:8] switch position is closed. A high indicates the switch position is open. This register should be ignored when the VG230 is configured for the PC/XT serial keyboard interface mode.

The Shift and NMI Status Register is used for both the internal keyboard scanner and PC/XT serial keyboard modes. It contains bits that enable keyboard related NMIs as well as bits that show the cause of the NMI.

Name: **Keyboard Shift and NMI Status Register**
Type **Read/Write**
Index: **0CH**

D7	D6	D5	D4	D3	D2	D1	D0
KEYNMI	STMONMI	PPIBNMI	KNMIEN	SNMIEN	PNMIEN	Reserved	SH4

Bit	Default	Function
D7	0	1 - NMI caused by Keyboard Input. Writing this register with bit D7 set high will clear both the NMI signal and the KEYNMI bit.
D6	0	1 - NMI caused by Keyboard Scan Time Out. Writing this register with bit D6 set high will clear both the NMI signal and the STMONMI bit.
D5	0	1 - NMI caused by write to PPIB port requesting Keyboard Diagnostics. Writing this register with bit D5 set high will clear both the NMI signal and the PPIBNMI bit.
D4	0	1 - Enable Keyboard Input NMIs.
D3	0	1 - Enable Periodic NMIs generated by the Scan Timer.
D2	0	1 - Enable NMIs caused by writes to PPIB port requesting Keyboard Diagnostics.
D1	0	Reserved for future use.
D0	0	SHFT input status. 0 - SHFT4 switch position is closed. 1 - SHFT4 switch position is open.
		Note: *In PC/XT serial I/F mode, this register is ignored.*

Bits D[7:5] are used to determine the cause of the keyboard NMI. A high on KEYNMI (D7) indicates a keyboard NMI was caused when a key was pressed when the keyboard was not being actively scanned. A high on STMONMI (D6) indicates the keyboard NMI was caused by the keyboard scan rate logic. A high on PPIBNMI (D5) indicates a keyboard NMI was caused by a software write to the PPIB Keyboard Control Register (061H) requesting keyboard diagnostics. Writing this register with the appropriate bit set high will clear both the NMI signal and the NMI cause bit.

Note*: KNMIEN must drive scan lines low (Index 09H) before writing 1.*
By writing 0 to D4, D3, D2 also clears D7, D6, D5.

Bits D[4:2] are used to enable the keyboard NMIs. A high written to KNMIEN (D4) allows a NMI, generated by a key being pressed, to be passed on to the CPU. When this bit is low, no NMI will be generated. When set high, SNMIEN (D3) enables keyboard scan time-out NMIs to be passed on to the CPU. And when set high, PNMIEN (D2), allows NMIs caused by keyboard diagnostic requests to be passed on to the CPU.

SH4 (D0) reflects the state of the SHFT4 input pin. A low indicates the corresponding SHFT4 switch position is closed. A high indicates the switch is open. This bit is ignored when the VG230 is configured for the PC/XT serial keyboard interface.

Name: **ICU Mode Register**
Type **Read/Write**
Index: **0DH**

D7	D6	D5	D4	D3	D2	D1	D0
IRAS2	IRAS1	IRAS0	Reserved	IRBS2	IRBS1	IRBS0	Reserved

Bit	Default	Function			
D[7:5]	101	IRAS2	IRAS 1	IRAS 0	IRQA Interrupt
		0	0	0	Illegal
		0	0	1	Illegal
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
D4	0	Reserved for future use.			
D[3:1]	110	IRBS2	IRBS 1	IRBS 0	IRQB Interrupt
		0	0	0	Illegal
		0	0	1	Illegal
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
D0	0	Reserved for future use.			

Name: **DMA Mode Register**
Type **Read/Write**
Index: **0EH**

D7	D6	D5	D4	D3	D2	D1	D0
REFW2	REFW 1	REFW 0	STPDCLK	WDLY1	WDLY0	DRQS1	DRQS0

Bit	Default	Function			
D[7:5]	111	REFW2	REFW 1	REFW 0	Refresh Wait States
		0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
D4	0	0 - DMA clock runs always. 1 - DMA clock runs only during DMA cycles.			
D[3:2]	01	WDLY1	WDLY0	IOWR/MWR Command Delay	
		0	0	0 SYSCLK cycles	
		0	1	1 SYSCLK cycles	
		1	0	2 SYSCLK cycles	
		1	1	3 SYSCLK cycles	
		Note: *For each SYSCLK cycle command delay specified by WDLY[1:0] one bus wait state will be added to the DMA cycle.*			
D[1:0]	10	DRQS1	DRQS0	DMA Channel Select	
		0	0	Illegal	
		0	1	DRQ1/*DACK1	
		1	0	DRQ2/*DACK2	
		1	1	DRQ3/*DACK3	

Name: **SIO Mode Register**
Type **Read/Write**
Index: **10H**

D7	D6	D5	D4	D3	D2	D1	D0
SIOENA	STPSCLK	SPSEL	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Default	Function
D7	1	0 - Disable internal Serial Port. 1 - Enable internal Serial Port.
D6	0	0 - Enable SIO crystal oscillator. 1 - Disable SIO crystal oscillator.
D5	0	0 -SIO Port appears at I/O 3F8H - 3FFH and uses IRQ4. 1 - SIO Port appears at I/O 2F8H - 2FFH and uses IRQ3.
D[4:0]	00H	Reserved for future use.

During normal SIO operation, there may be long periods of time where no characters are being transmitted or received. The VG230 allows the designer to automatically stop the internal 8250 clocks after a programmable inactive time (from 1 to 120 seconds). These power management controls are located in the SIO Power control register located at index 11H.

Power management is enabled by setting TMO[3:0] to a non-zero number. If TCLKSEL is set to zero TMO[3:0] selects the clock timeout value in 1 second intervals. If TCLKSEL is set to one TMO[3:0] selects the clock timeout value in 8 second intervals. The SIO activity is defined by either writes to the SIO transmit buffer, or transitions on any of the SIO's input lines (RXD, DCD, RI, DSR, or CTS). Either of these events will retrigger the activity timer and place the SIO into the full power mode. Selection of which events will retrigger the activity monitor is accomplished through the INPMSK and the TXDMSK bits in the SIO power control register.

Name: **SIO Power Control Register**
Type **Read/Write**
Index: **11H**

D7	D6	D5	D4	D3	D2	D1	D0
INPMSK	TXDMSK	Reserved	TCLKSEL	TMO3	TMO2	TMO1	TMO0

Bit	Default	Function
D7	0	0 - Retrigger Serial Port clock timer on high to low transition of RXD, *DCD, *RI, *DSR, or *CTS inputs. 1 - Mask above inputs from retriggering Serial Port clock.
D6	0	0 - Retrigger Serial Port clock timer on writes to transmit buffer. 1 - Mask above writes from retriggering Serial Port clock.
D5	0	Reserved for future use.
D4	0	0 - Timer range is from 1 to 15 seconds (1 sec. resolution). 1 - Timer range is from 8 sec. to 2 min. * sec. resolution).
D[3:0]	0H	SIO Clock time-out value. Setting this register to 0 disables the timer.

Name: **Timer Mode Register**
Type **Read/Write**
Index: **13H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	STPTCLK

Bit	Default	Function
D[7:1]	0	Reserved for future use.
D0	0	0 - 8254 Timer clock, TCLK, runs always. 1 - 8254 Timer clock, TCLK, stopped during Doze/Sleep.

Parallel Printer Interface

When the internal keyboard scanner is disabled, the free pins may be used as a standard parallel printer I/O port. The VG230 supports all three of the standard PC compatible LPT ports. Selection of port address is accomplished through the PIO Mode register located at index 18H.

The implementation of a standard PC compatible printer port requires the addition of an external data latch and a control signal buffer. In addition the status inputs require external pull-up resistors.

Name: **PIO Mode Register**
Type **Read/Write**
Index: **18H**

D7	D6	D5	D4	D3	D2	D1	D0
PIOENA	Reserved	PPSEL1	PPSEL0	BIDIR	Reserved	Reserved	Reserved

Bit	Default	Function		
D7	0	0 - Disable internal Parallel Port. 1 - Enable internal Parallel Port (This bit is valid only if Keyboard Scan function is disabled. Otherwise, Parallel Port is forced to be disabled.)		
D6	0	Reserved for future use.		
D[5:4]	00	PPSEL1	PPSEL0	Parallel Port I/O Address
		0	0	278H-27AH
		0	1	378H-37AH
		1	0	3BCH-3BEH
		1	1	170H-172H
D3	0H	0 - Parallel Port is uni-directional (output only). 1 - Parallel Port is bi-directional. Setting the PPDIR bit of the Parallel Port Control register forces reads from the Parallel port data registers to be sourced from the external data bus.		
D[2:0]	0H	Reserved for future use.		

Name: **Main NMI Status Register**
Type **Read/Write**
Index: **19H**

D7	D6	D5	D4	D3	D2	D1	D0
TA3	TA2	TA1	TA0	ENMI1	ENMI0	KBDNMI	PMUNMI

Bit	Default	Function		
D[7:4]	X	NMI Trap Address bits. ISA[3:0] are latched when an NMI is generated by the System Management Unit to drive these bits.		
D[3:2]	00	ENMI1	ENMO0	System Management NMI Status
		0	0	No System Management NMI Pending
		0	1	Port 1 System Management NMI Pending
		1	0	Port 2 System Management NMI Pending
		1	1	Port 3 System Management NMI Pending
		A particular System Management NMI is cleared by writing this register with bits D[3:2] configured to select that NMI.		
D1	0	1 - NMI generated by Keyboard.		
D0	0	1 - NMI generated by PMU.		

Note: *The NMI vector is ALWAYS located and fetched from ROM. The VG230 will switch memory blocks to access this vector. The memory blocks are returned to their original state by reading the NMI Mask Register, Index C4H, to clear the NMI.*

Name: **Port 1 NMI Trap Address Low Register**
Type **Read/Write**
Index: **1AH**

D7	D6	D5	D4	D3	D2	D1	D0
P1TA7	P1TA6	P1TA5	P1TA4	P1TA3	P1TA2	P1TA1	P1TA0

Bit	Default	Function
D[7:0]	00H	Lower 8 address bits of the I/O address which will be emulated.

Name: **Port 1 NMI Trap Address High Register**
Type **Read/Write**
Index: **1BH**

D7	D6	D5	D4	D3	D2	D1	D0
P1EN1	P1EN0	P1RNG1	P1RNG0	P1MIR	Reserved	P1TA9	P1TA8

Bit	Default	Function		
D[7:6]	00	P1EN1	P1EN0	Port 1 Emulation NMI Mode.
		0	0	Disable Port 1 NMIs.
		0	1	Generate NMI on IORD from Port 1 address.
		1	0	Generate NMI on IOWR to Port 1 address.
		1	1	Generate NMI on IORD from or IOWR to Port 1 address.
D[5:4]	00	P1RNG1	P1RNG0	Port 1 Address Range.
		0	0	2 bytes
		0	1	4 bytes
		1	0	8 bytes
		1	1	16 bytes
D3	0	0 - Disable address mirroring. Port 1 decoding is based upon ISA[15:0], and is enabled only when ISA[15:10] are all low. 1 - Enable address mirroring. Port 1 decoding is based only upon ISA[9:0].		
D2	0	Reserved for future use.		
D[1:0]	00	Upper 2 address bits of the I/O address which will be emulated.		
NOTE: *To trap a port:*		*Index 1B* *0 26 16* *Write 80* *0 27 80* *Index 1C* *0 26 1C* *Trap port 6C* *0 27 6C*		

Name: **Port 1 NMI Trap Address Low Register**
Type **Read/Write**
Index: **1CH** *(See Port 1 NMI Trap Address Low Register for bit definitions)*

D7	D6	D5	D4	D3	D2	D1	D0
P2TA7	P2TA6	P2TA5	P2TA4	P2TA3	P2TA2	P2TA1	P2TA0

Bit	Default	Function
D[7:0]	00H	

Name: **Port 2 NMI Trap Address High Register**
Type **Read/Write**
Index: **1DH** *(See Port 1 NMI Trap Address High Register for bit definitions)*

D7	D6	D5	D4	D3	D2	D1	D0
P2EN1	P2EN0	P2RNG1	P2RNG0	P2MIR	Reserved	P2TA9	P2TA8

Bit	Default	Function
D[7:6]	00	
D[5:4]	00	
D3	0	
D2	0	Reserved for future use.
D[1:0]	00	

Name: **Port 3 NMI Trap Address Low Register**
Type **Read/Write**
Index: **1EH** *(See Port 1 NMI Trap Address Low Register for bit definitions)*

D7	D6	D5	D4	D3	D2	D1	D0
P3TA7	P3TA6	P3TA5	P3TA4	P3TA3	P3TA2	P3TA1	P3TA0

Bit	Default	Function
D[7:0]	00H	

Name: **Port 3 NMI Trap Address High Register**
Type **Read/Write**
Index: **1FH** *(See Port 1 NMI Trap Address High Register for bit definitions)*

D7	D6	D5	D4	D3	D2	D1	D0
P3EN1	P3EN0	P3RNG1	P3RNG0	P3MIR	Reserved	P3TA9	P3TA8

Bit	Default	Function
D[7:6]	00	
D[5:4]	00	
D3	0	
D2	0	Reserved for future use.
D[1:0]	00	

PCMCIA Register Description

There are a total of 15 registers that control the PC card interface. These registers can be placed into the following 3 groups:

Global PC Card Control

PC Card Controller Mode Register	20H
PC Card Power Control Register	2DH
PC Card Activity Timer Mode Register	2EH

Slot 0 PC Card Control

PC Card Slot 0 Control Register	21H
PC Card Slot 0 Status Register	22H
PC Card Slot 0 Interrupt Mask Register	23H
PC Card Slot 0 I/O High Address Register	24H
PC Card Slot 0 I/O Low Address Register	25H
PC Card Slot 0 I/O Address Range Register	26H

Slot 1 PC Card Control

PC Card Slot 1 Control Register	27H
PC Card Slot 1 Status Register	28H
PC Card Slot 1 Interrupt Mask Register	29H
PC Card Slot 1 I/O High Address Register	2AH
PC Card Slot 1 I/O Low Address Register	2BH
PC Card Slot 1 I/O Address Range Register	2CH

There is also an additional register described in the Bus Cycle Generator section that controls the PC card interface:

Bus Cycle Generator Wait State Control 2 Reg	03H

Global PC Card Control

The PC Card Controller Mode Register at offset 20H controls the global enable for each PC card. *SLOT0EN and *SLOT1EN enable the I/O and memory chip select decoding of the selected PC card.

The PC card controller can be configured to interrupt the CPU on status changes that occur on the PC card interface. These changes include:

- Card Change
- Battery Fail
- Low Battery
- Card Timeout

The IRSTS[1:0] bits route the status interrupt to IRQ2, IRQ6, IRQ7 or NMI. Interrupt status is presented in the PC Card Status registers at offset 22H and 28H.

These bits control the programming enable pin. VPPENA and VPPENB are asserted only under the following conditions:

- S1PGMEN or S0PGMEN are set
- VPCRD is true
- PC card is inserted into the socket

It is the responsibility of the BIOS or software drivers to provide proper programming voltage sequencing and timing for memory programming.

In this example, mapping registers 1,2 and 3 are mapped to the bottom 3 pages of the PCMCIA card.

Mapping Register 1

Map Address Register	Low Byte	High Byte
80H	0000 0000	1 100 0000

Mapping Register 2

Map Address Register	Low Byte	High Byte
84H	0000 0001	1 100 0000

Mapping Register 3

Map Address Register	Low Byte	High Byte
88H	0000 0010	1 100 0000

Mapping Register 4

Mapping register 4 is mapped to the 40th 16K page in PCMCIA.

Map Address Register	Low Byte	High Byte
8CH	0010 1001	1 100 0000

Mapping Register 5

Mapping register 5 is mapped to the 44th page in the RAM array.

Map Address Register	Low Byte	High Byte
90H	0010 1101	1 001 0000

Mapping Register 21

Mapping register 21 is mapped to 59th page of the ROM array.

Map Address Register	Low Byte	High Byte
D8H	0011 1011	1 010 0000

As you can see from this example, the VG230's flexible memory architecture allows access to very large memory arrays through the 8086's limited address space. Access can be controlled through several different memory managers including EMS driver, PCMCIA XIP drivers, ROMDOS and ROM Disk drivers.

Name: **PC Card Controller Mode Register**
Type **Read/Write**
Index: **20H**

D7	D6	D5	D4	D3	D2	D1	D0
*SLOT0EN	*SLOT1EN	IRSTS1	IRSTS0	S0PGMEN	Reserved	S2PGMEN	Reserved

Bit	Default	Function		
D7	0	0 - Enable PC Card Slot 0.		
D6	1	0 - Enable PC card Slot 1.		
		Note: *In order to enable PC Card Slot 1, the Keyboard Scan function must be disabled.*		
D[5:4]	11	IRSTS1	IRSTS0	Interrupt Channel Select for Controller Status Interrupts
		0	0	NMI
		0	0	IRQ2
		0	0	IRQ6
		0	0	IRQ7
D3	0	1 - Enable Slot 0 Programming Voltage (VPPENA).		
D2	0	Reserved bits.		
D1	0	1 - Enable Slot 1 Programming Voltage (VPPENB).		
D0	0	Reserved bits.		
Note: *Programming controls are automatically disabled when a card is removed from its socket or when Vcc to the cards has been removed.*				

Name: **PC Card Slot 0 Control Register**
Type **Read/Write**
Index: **21H**

D7	D6	D5	D4	D3	D2	D1	D0
IO8BIT	IO/*M	*REG	IRCRD2	IRCRD1	IRCRD0	CDLY1	CDLY0

Bit	Default	Function			
D7	0	1 - PC Card Slot 0 supports 8 bit I/O only. Data is transferred from the PC I/O Card on the low order data bus (D[7:0]).			
D6	0	0 - PC Card Slot 0 configured for Memory I/F. 1 - PC Card Slot 0 configured for I/O I/F.			
		*While either one of *CD[2:1]A is high indicating a PC Card is not installed, or the PC Card is powered OFF, this bit is automatically reset low and the controller is forced into the Memory I/F Mode.*			
D5	0	0 - Direct PC Card access to REG (Attribute) memory. 1 - Direct PC Card access to Common memory.			
		*Normally, the *REGA output pin is driven directly from this bit. During DMA Cycles, this bit is ignored and the *REGA output is driven high.*			
D[4:2]	111	IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)
		0	0	X	Illegal
		0	1	0	IRQ2
		0	1	1	IRQ3
		1	0	0	IRQ4
		1	0	1	IRQ5
		1	1	0	IRQ6
		1	1	1	IRQ7
D[1:0]	01	CDLY1		CDLY0	PC Card Memory Command Delay
		0		0	0 CPUCLK cycle
		0		1	1 CPUCLK cycle
		1		0	2 CPUCLK cycle
		1		1	3 CPUCLK cycle

Name: **PC Card Slot 0 Status Register**
Type **Read/Write**
Index: **22H**

D7	D6	D5	D4	D3	D2	D1	D0
*BUSY/ *CRDINT	BVD2/ *AUDIO	BVD1/ *STSCHG	*PRESENT	*CRDCHG	*CRDTM0	WP/NU	CRDOFF

Bit	Default	Function
D7	1	Read Only bit reflecting state of RDY/*BSYA input during Memory Mode or latched *IREQA for I/O Mode. 0 - Card Busy (Memory) Card Interrupt Pending (I/O) In I/O mode this bit may be set by writing this register with bit D7 set high.
D6	1	Read Only bit reflecting state of BVD2A input during Memory Mode or *AUDIOA for I/O Mode. 0 - Battery Low (Memory) Card Speaker Active (I/O). In Memory mode, this bit is driven directly from the BVD2 input pin when Low Battery interrupts are masked OFF. Or, it is driven from the latched BVD2 input when Low Battery interrupts are enabled. When interrupts are enabled, writing this register with bit D6 set high clears the Low Battery Interrupt and sets this bit. *In I/O mode the state of the I/O card signal may be read here.*
D5	1	Read Only bit reflecting state of BVD1A input during Memory Mode or *STSCHGA for I/O Mode. 0 - Battery Fail (Memory) Status Change (I/O). This bit is driven directly from the BVD1/*STSCHG input when Battery fail interrupts are masked OFF. OR, it is driven from the latched BVD1/*STSCHG input when Battery Fail interrupts are enabled. *When interrupts are enabled, writing this register with bit D5 set high clears the Battery Fail or Status Changed Interrupt and sets this bit.*
D4	X	Read Only bit reflecting state of *CD[2:1] A inputs. 0 - Card Present (Low when both *CD[2:1]A are low). While Card A is removed from its socket, PC Card Slot 0 Status bits D[7:5] will be forced high, and D1 will be forced low.
D3	1	Card Change status bit. *CRDCHG is reset on the rising edge of either *CD[2:1]A. 0 - Card has been changed. *This bit is set and the Card Change Interrupt is* cleared by *writing this register with bit D3 set high.*
D2	1	Card Activity Time-Out. 0 - Card Time-Out. *Writing this register with bit D2 set high sets this bit and clears the Card Time-Out interrupt.*
D1	X	Read Only bit reflecting state of WPA input during Memory Mode. This pin reads back low in I/O Mode. 1 - Card Write Protected.
D0	0	1 - Power to PC Card slot 0 and 1 is OFF.

Note: *Bits D2 and D3 =0 after SUSPEND/RESUME.*

The PC Card Slot 0 Interrupt Mask register at index 23H controls interrupt generation for slot 0. Both status interrupts and I/O interrupt features are controlled through this register. When IREQMSK = 1, I/O interrupts are disabled from the selected slot. The PULSED bit selects level- or pulsed-mode interrupts from the I/O card. Both of the previously described bits are “don’t care” when a memory card is inserted.

When memory mode is enabled, the LBMSK bit enables low battery status interrupts. This interrupt indicates that the battery is low and requires changing. It does not indicate that the PC Card’s memory is invalid. When I/O card is enabled, this bit is used to control the PC card audio output. When set, this bit keeps the audio signal from being ORed into the VG230’s speaker circuit. Status for this interrupt can be monitored in the BVD2/*AUDIO bit in the Status register.

When memory card is enabled, the LLBMSK bit controls the Battery fail alarm (BVD1 input) interrupt. This interrupt indicates that the PC card’s battery has failed, and data contained in the card is invalid. In I/O mode this bit controls the status change input interrupt. Status for this interrupt can be monitored in the BVD1/*STSCHG bit in the Status register.

When memory card or I/O card is enabled, the CHGMSK bit controls the card removal interrupt. Status for this interrupt can be monitored in the *CRDCHG bit of the Status register.

Name: **PC Card Slot 0 Interrupt Mask Register**
Type **Read/Write**
Index: **23H**

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	Reserved	CHGMSK	Reserved	Reserved	PULSED

Bit	Default	Function
D7	1	0 - Enable interrupts generated from Slot 0 I/O Cards.
D6	0	0 - Enable Slot 0 low battery warning interrupts (Memory Mode) or disable PC Card Audio Output (I/O Mode). *When this bit is reset Low in I/O Mode, the PC Card Audio signal is disabled and will read back High in the Status Register.*
D5	0	0 - Enable Slot 0 Battery Fail Alarm Interrupts (Memory Mode) or enable Slot 0 Status Changed Interrupts (I/O Mode).
D4	0	Reserved bit.
D3	0	0 - Enable interrupts for Card Removal from Slot 0.
D[2:1]	00	Reserved bits.
D0	0	0 - Controller supports Level Mode Interrupts from PC I/O Cards. 1 - Controller supports Pulsed Mode Interrupts from PC I/O Cards.

The next set of PC card registers control the operation of the I/O card. The VG230's I/O address interface supports a 64Kbyte address space. The PCMCIA standard allows both fixed address cards and variable address cards. The VG230 supports both. For cards that support their own internal address decoding, the *INPACK pin is driven when the card recognizes its own address range. For I/O cards that require the host to configure the address the VG230 contains three registers to configure the starting address and length of the I/O space occupied by the PC card. The selection of the type of I/O device is controlled by the *INPMSK bit in the I/O address range register at offset 26H. When this bit is set, the I/O decode address is determined by the PC card. When this bit is cleared, the I/O decode address is determined by the I/O high address reg (24H), the I/O low address register (25H) and the I/O address range reg (26H).

Name: PC Card Slot 0 I/O High Address Register
Type Read/Write
Index: 24H

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

Bit	Default	Function
D[7:0]	00H	Upper address bits for slot 0 PC Card base I/O address.

Name: PC Card Slot 0 I/O Low Address Register
Type Read/Write
Index: 25H

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bit	Default	Function
D[7:3]	00H	Low address bits for slot 0 PC Card base I/O address.
D[2:0]	000	Reserved bits.

Name: **PC Card Slot 0 I/O Address Range Register**
Type **Read/Write**
Index: **26H**

D7	D6	D5	D4	D3	D2	D1	D0
A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	Reserved	Reserved	*INPMSK

Bit	Default	Function
D[7:3]	00H	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked from the address comparison as follows:

A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	I/O Range
0	0	0	0	0	8 Bytes
0	0	0	0	1	16 Bytes
0	0	0	1	1	32 Bytes
0	0	1	1	1	64 Bytes
0	1	1	1	1	128 Bytes
1	1	1	1	1	256 Bytes

D[2:1]	000	Reserved bits.
D0	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.

Name: **PC Card Slot 1 Control Register**
Type **Read/Write**
Index: **27H**

D7	D6	D5	D4	D3	D2	D1	D0
I08BIT	I0/*M	*REG	IRCRD2	IRCRD1	IRCRD0	CDLY1	CDLY0

Bit	Default	Function			
D7	0	1 - PC Card Slot 0 supports 8 bit I/O only. Data is transferred from the PC I/O Card on the low order data bus (D[7:0]).			
D6	0	0 - PC Card Slot 0 configured for Memory I/F. 1 - PC Card Slot 0 configured for I/O I/F. *While either one of *CD[2:1]B is high indicating a PC Card is not installed, or the PC Card is powered OFF, this bit is automatically reset low and the controller is forced into the Memory I/F Mode.*			
D5	0	0 - Direct PC Card access to REG (Attribute) memory. 1 - Direct PC Card access to Common memory. *Normally, the *REGB output pin is driven directly from this bit. During DMA Cycles, this bit is ignored and the *REGB output is driven high.*			
D[4:2]	111	IRCRD2	IRCR0	IRCRD0	Interrupt Channel Select for PC Card (IREQ)
		0	0	X	Illegal
		0	1	0	IRQ2
		0	1	1	IRQ3
		1	0	0	IRQ4
		1	0	1	IRQ5
		1	1	0	IRQ6
		1	1	1	IRQ7
D[1:0]	01	CDLY1		CDLY0	PC Card Memory Command Delay
		0		0	0 CPUCLK cycle
		0		1	1 CPUCLK cycle
		1		0	2 CPUCLK cycle
		1		1	3 CPUCLK cycle
D[2:1]	000	Reserved bits.			
D0	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.			

Name: **PC Card Slot 1 Status Register**
Type **Read/Write**
Index: **28H**

D7	D6	D5	D4	D3	D2	D1	D0
*BUSY/ *CRDINT	BVD2/ *AUDIO	BVD1/ *STSCHG	*PRESENT	*CRDCHG	*CRDTM0	WP/NU	CRDOFF

Bit	Default	Function
D7	1	Read Only bit reflecting state of RDY/*BSYB input during Memory Mode or latched *IREQB for I/O Mode. 0 - Card Busy (Memory) Card Interrupt Pending (I/O). In I/O mode this bit may be set by writing this register with bit D7 set high.
D6	1	Read Only bit reflecting state of BVD2B input during Memory Mode or *AUDIOA for I/O Mode. 0 - Battery Low (Memory) Card Speaker Active (I/O). In Memory mode, this bit is driven directly from the BVD2 input pin when Low Battery interrupts are masked OFF. Or, it is driven from the latched BVD2 input when Low Battery interrupts are enabled. When interrupts are enabled, writing this register with bit D6 set high clears the Low Battery Interrupt and sets this bit. *In I/O mode the state of the I/O card signal may be read here.*
D5	1	Read Only bit reflecting state of BVD1B input during Memory Mode or *STSCHGB for I/O Mode. 0 - Battery Fail (Memory) Status Change (I./O). This bit is driven directly from the BVD1/*STSCHG input when Battery Fail interrupts are masked OFF. Or, it is driven from the latched BVD1/*STSCHG input when Battery Fail interrupts are enabled. *When interrupts are enabled, writing this register with bit D5 set high clears the Battery Fail or Status Changed Interrupt and sets this bit.*
D4		Read Only bit reflecting state of *CD[2:1]B inputs. 0 - Card Present (Low when both *CDR[2:1]B are low). While Card B is removed from its socket, PC Card Slot 0 Status bits D[7:5] will be forced high, and D1 will be forced low.
D3	1	Card Change status bit. *CRDCHG is reset on the rising edge of either *CD[2:1]B. 0 - Card has been changed. This bit is set and the Card Change Interrupt is cleared by writing this register with bit D3 set high.
D2	1	Card Activity Time-Out. 0 - Card Time-Out. Writing this register with bit D2 set high sets this bit and clears the Card Time-Out interrupt.
D1		Read Only bit reflecting state of WPA input during Memory Mode. This pin reads back low in I/O Mode. 1 - Card Write Protected.
D0	0	1 - Power to PC Card slot 0 and 1 is OFF.

Note: *(Bit D7) Wait until =1 from RESUME*

Name: **PC Card Slot 1 Interrupt Mask Register**
Type **Read/Write**
Index: **29H**

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	Reserved	CHGMSK	Reserved	Reserved	PULSED

Bit	Default	Function
D7	1	0 - Enable interrupts generated from Slot 0 I/O Cards.
D6	0	0 - Enable Slot 1 low battery warning interrupts (Memory Modes) or disable PC Card Audio Output (I/O Mode). *When this bit is reset Low in I/O Mode, the PC Card Audio signal is disabled and will read back High in the Status Register.*
D5	0	0 - Enable Slot 1 Battery Fail Alarm Interrupts (Memory Mode). 1 - Enable Slot 1 Status Changed Interrupts (I/O) Mode).
D4	0	Reserved bit.
D3	0	0 - Enable interrupts for Card Removal from Slot 1.
D[2:1]	00	Reserved bits.
D0	00	0 - Controller supports Level Mode interrupts from PC I/O Cards. 1 - Controller supports Pulsed Mode interrupts from PC I/O Cards.

Name: **PC Card Slot 1 I/O High Address Register**
Type **Read/Write**
Index: **2AH**

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

Bit	Default	Function
D[7:0]	00H	Upper address bits for slot 1 PC Card base I/O address.

Name: **PC Card Slot 1 I/O Low Address Register**
Type **Read/Write**
Index: **2BH**

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bit	Default	Function
D[7:3]	00H	Low address bits for slot 1 PC Card base I/O address.
D[2:0]	000	Reserved bits.

Name: **PC Card Slot 1 I/O Address Range Register**
Type **Read/Write**
Index: **2CH**

D7	D6	D5	D4	D3	D2	D1	D0
A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	Reserved	Reserved	*INPMSK

Bit	Default	Function
D[7:3]	00H	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked from the address comparison as follows:

A7MSK	A6MSK	A5MSK	A4MSK	A3MSK	I/O Range
0	0	0	0	0	8 Bytes
0	0	0	0	1	16 Bytes
0	0	0	1	1	32 Bytes
0	0	1	1	1	64 Bytes
0	1	1	1	1	128 Bytes
1	1	1	1	1	256 Bytes

D[2:1]	000	Reserved bits.
D0	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O card *INPACK signal. PC card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC card data buffers enabled only when chip select is asserted and *INPACK is returned from PC I/O card.

The VPEN bit allows the PMU, in addition to the PC card activity timer, to control power to the PC card interface. When set the VP3 output of the PMU is Or'ed with the PC card activity timer output to control the VPCRD output.

Name: **PC Card Power Control Register**
Type **Read/Write**
Index: **2DH**

D7	D6	D5	D4	D3	D2	D1	D0
TMOMSK	VPEN	POL	VPCRD	Reserved	Reserved	Reserved	Reserved

Bit	Default	Function
D7	1	0 - Enable interrupts for Activity Time-Out.
D6	0	0 - VP output form PMU does not control power to PC Cards. 1 - VP output is Or'ed with Activity timer to control power to PC Cards.
D5	1	0 - VPCRD output is defined as Low=ON. 1 - VPCRD output is defined as High=ON.
D4	0	PC Card On/Off bit. This bit is ignored when Time-Out interrupts are disabled or when both PC Card Slots are empty. When Time-Out interrupts are disabled, power to the PC Card is automatically removed when the PC Card Activity timer expires. When Time-Out interrupts are enabled, this bit is used by software to control power to the PC Cards.
D[3:0]	0H	Reserved bit.

The POL bit controls the polarity of the VPCRD output. The default condition is ON = VPCRD = 1.

The VPCRD bit is used to directly control the VPCRD output. This bit is only enabled when TMOMSK is set to 0 and one or more PC cards are inserted into the slots. VPCRD is used by the BIOS to control power to the PC card interface.

The PC card activity timer register at offset 2EH enables the PC card activity timer. The TMRES bit sets the timer resolution. When set the resolution is 1 minute and 15 seconds when cleared. Therefore, the minimum timeout is 15 seconds and maximum is 15 minutes. Setting TMO[3:0] to a non zero number enables the activity timer. Any I/O or memory access to an enabled PC card resets the timer.

Name: **PC Card Activity Timer Register**
Type **Read/Write**
Index: **2EH**

D7	D6	D5	D4	D3	D2	D1	D0
TMRES	Reserved	Reserved	Reserved	TMO3	TMO2	TMO1	TMO0

Bit	Default	Function
D7	0	0 - Timer supports from 15 to 225 sec. (15 sec. resolution). 1 - Timer supports from 1 to 15 min. (1 min. resolution).
D[6:4]	000	Reserved bits.
D[3:0]	0H	TMO[3:0] select the Activity Time-Out value. Setting the TMO{3:0] all low will disable the timer.
Note: *When Activity Time-Out interrupts are disabled and the Activity Timer expires, power to the PC Cards will automatically be removed. Subsequent activity to the PC Cards WILL NOT restore power to the Slots. In order for power to be restored, software must first write any value to the PC Card Activity Timer Register.*		

When the timer expires, an interrupt is generated or power is automatically removed from the card. When Activity timeout interrupts are enabled (through the TMOMSK bit in the PC card power control register) an interrupt is generated and it is up to the BIOS to determine if power is to be removed from the PC cards. The BIOS must restore power by writing a non-zero number into the TMO[3:0] register and setting VPCRD in the PC card power control register.

When activity timeout interrupts are disabled, power is automatically removed from the PC card. When power is automatically removed in this method, power must be re-enabled through a software routine.

Name: **BIOS Time Base Low Register**
Type **Read Only**
Index: **30H**

D7	D6	D5	D4	D3	D2	D1	D0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

Bit	Default	Function
D[7:0]	00H	Low byte of the BIOS Timer count.

Name: **BIOS Time Base High Register**
Type **Read Only**
Index: **31H**

D7	D6	D5	D4	D3	D2	D1	D0
TMR15	TMR14	TMR13	TMR12	TMR11	TMR10	TMR9	TMR8

Bit	Default	Function
D[7:0]	00H	High byte of the BIOS Timer count. The BIOS Time Base Registers are driven by a 16 bit up counter clocked form the 1.19MHz TCLK signal.

Name: **GPIO Mode Register**
Type **Read/Write**
Index: **32H**

D7	D6	D5	D4	D3	D2	D1	D0
GP3M1	GP3M0	GP2M1	GP2M0	GP1M1	GP1M0	GP0M1	GP0M0

Bit	Default	Function		
D[7:6]	00	GP3M1	GP3M0	LCDL3 Function
		0	0	General Purpose Input-GPI3.
		0	1	LCDL3.
		1	0	General Purpose Output-GPO3.
		1	1	CPU Clock Output. Due to potentially excessive skew, we do not guarantee timing relationship between this output and any other VG230 input or output. This output is intended only for observation of the CPU clock.
D[5:4]	00	GP2M1	GP3M0	LCDL2 Function
		0	0	General Purpose Input-GPI2.
		0	1	LCDL2.
		1	0	General Purpose Output-GPO2.
		1	1	SYSCLK-XT Bus Clock (Operates only during external I/O.)
D[3:2]	00	GP1M1	GP1M0	LCDL1 Function
		0	0	General Purpose Input-GPI1
		0	1	LCDL1
		1	0	General Purpose Output-GPO1
		1	1	ALE-Address Latch Enable
D[1:0]	00	GP0M1	GP0M0	LCDL0 Function
		0	0	General Purpose Input-GPI0.
		0	1	LCDL0.
		1	0	General Purpose Output-GPO0.
		1	1	*DACK0-Indicates Memory Refresh.

Name: **GPIO Control Register**
Type **Read/Write**
Index: **33H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	GPIO3	GPIO2	GPIO1	GPIO0

Bit	Default	Function
D[7:4]	0H	Reserved bits.
D3	0	**General Purpose I/O bit 3.** When programmed as GPO, this bit is read/write and appears on the LCDL3 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL3 pin. Otherwise, this bit will read back low.
D2	0	**General Purpose I/O bit 2.** When programmed as GPO, this bit is read/write and appears on the LCDL2 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL2 pin. Otherwise, this bit will read back low.
D1	0	**General Purpose I/O bit 1.** When programmed as GPO, this bit is read/write and appears on the LCDL1 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL1 pin. Otherwise, this bit will read back low.
D0	0	**General Purpose I/O bit 0** When programmed as GPO, this bit is read/write and appears on the LCDL0 pin. When programmed as GPI, this bit is read only and reflects the state of the signal driving the LCDL0 pin. Otherwise, this bit will read back low.

Name: **Top of Memory Register**
Type **Read/Write**
Index: **38H**

D7	D6	D5	D4	D3	D2	D1	D0
BUF16K	Spare	BA19	BA18	BA17	BA16	BA15	BA14

Bit	Default	Function
D7	0	0 - Display Buffer size is 32 Kbytes. 1 0 Display Buffer size is 16 Kbytes.
D6	0	Spare R/W bit.
D[5:0]	101000	Top of memory. For addresses below 640K, these bits are set to indicate the start of physical RAM reserved for the display buffer or other uses. Once set, all memory accesses to addresses equal to or greater than the value written to these bits will be inhibited except through the CGA address space (B8000H-BFFFFH), or mapping registers.

Name: **ICU Shadow Register**
Type **Read Only**
Index: **40H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	ICU_BUSY	INIT	POLL	ISR

Bit	Default	Function
D[7:4]	FH	Reserved bits read back high.
D3	0	0 - ICU not busy. 1 - ICU busy. This bit is set high while either the INIT or POLL bits are high.
D2	0	0 - ICU not being initialized. 1 - ICU is being initialized. This bit is set high when ICW1 is written to the ICU and cleared when ICW4 is written to the ICU.
D1	0	0 - ICU is not programmed into Polled Mode. 1 - ICU is programmed into Polled Mode. Writing Port 20H of the ICU will set or clear this bit. Reading Port 20H of the ICU will clear this bit.
D0	0	0 - Reading the ICU ISR/IRR register returns IRR value. 1 - Reading the ICU ISR/IRR register returns ISR value.

Real Time Clock (RTC)

The real time clock (RTC) in the VG230 is a custom design that provides a time of day clock and alarm functions. Access to the RTC registers is through the VG230 Indexed registers.

RTC Timer Registers

There are a total of 5 registers that control the RTC timer chain. These are as follows:

RTC Seconds register
RTC Minutes register
RTC Hours register
RTC Days-low register
RTC Days-high register

Each of these registers represent the time of day in a binary format. It is up to the BIOS clock routine to convert these into a BCD format required by the standard "AT" type INT 1A functions. The two RTC day registers provide a 12 bit count, providing up to a 4096 day count or over 11 years. The BIOS converts the binary day count into a BCD day of week, day, month and year format required for the INT 1A function.

Name: **RTC Seconds Register**
Type **Read/Write**
Index: **70H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0

Bit	Default	Function
D[7:6]	00	Reserved bits. Read back low.
D[5:0]	00H	Binary value representing the seconds count. Valid settings are from 00H to 3BH.

Name: **RTC Minutes Register**
Type **Read/Write**
Index: **71H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	MIN5	MIN 4	MIN 3	MIN 2	MIN 1	MIN 0

Bit	Default	Function
D[7:6]	00	Reserved bits. Read back low.
D[5:0]	00H	Binary value representing the minutes count. Valid settings are from 00H to 3BH.

Name: **RTC Hours Register**
Type **Read/Write**
Index: **72H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	HR4	HR 3	HR 2	HR 1	HR 0

Bit	Default	Function
D[7:6]	000	Reserved bits. Read back low.
D[5:0]	00H	Binary value representing the hours count of a 24-hour clock. Valid settings are from 00H to 17H.

Name: **RTC Seconds Register**
Type **Read/Write**
Index: **73H**

D7	D6	D5	D4	D3	D2	D1	D0
DAY7	DAY6	DAY5	DAY4	DAY3	DAY2	DAY1	DAY0

Bit	Default	Function
D[7:0]	00H	Binary value representing the low day count. Valid settings are from 00H to FFH.

Name: **RTC Day High Register**
Type **Read/Write**
Index: **74H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	DAY11	DAY10	DAY9	DAY8

Bit	Default	Function
D[7:4]	0H	Reserved bits. Read back low.
D[3:0]	0H	Binary value representing the high day count. Valid settings are from 00H to 0FH.

Name: **RTC Alarm Seconds Register**
Type **Read/Write**
Index: **75H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	ALRS5	ALRS4	ALRS3	ALRS2	ALRS1	ALRS0

Bit	Default	Function
D[7:6]	00	Reserved bits. Read back low.
D[5:0]	00H	Binary value representing the alarm seconds count. Valid settings are from 00H to 3BH.

Name: **RTC Alarm Minutes Register**
Type **Read/Write**
Index: **76H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	ALRM 5	ALRM 4	ALRM 3	ALRM 2	ALRM 1	ALRM 0

Bit	Default	Function
D[7:6]	00	Reserved bits. Read back low.
D[5:0]	00H	Binary value representing the alarm minutes count. Valid settings are from 00H to 3BH.

Name: **RTC Alarm Hours Register**
Type **Read/Write**
Index: **77H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ALRH 4	ALRH 3	ALRH 2	ALRH 1	ALRH 0

Bit	Default	Function
D[7:5]	00	Reserved bits. Read back low.
D[4:0]	00H	Binary value representing the alarm hours count. Valid settings are from 00H to 17H.

Name: **RTC Alarm Day Register**
Type **Read/Write**
Index: **78H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ALRD 4	ALRD 3	ALRD 2	ALRD 1	ALRD 0

Bit	Default	Function
D[7:5]	000	Reserved bits. Read back low.
D[4:0]	00H	Binary value representing the alarm day count. Valid settings are from 00H to 1FH. This value is compared with the least significant 5 bits of the RTC Low Day counter.

The alarm is enabled through the RTC MODE register at index 79H. Bit 1, the ALRMINT bit when set enables RTC interrupts. The alarm interrupt RTCINT is asserted on IRQ2. The interrupt is cleared by writing a “1” to the ALARM bit in the RTC status register (7AH).

Hardware compares this with index 73H, if equal, alarm is set for the same day.

Periodic Interrupt Feature

The RTC is also capable of generating a 1Hz periodic interrupt. This feature is enabled by setting the PERINT bit in the RTC mode register at index 79H. When the PERINT bit is set, an RTCINT will be generated every second. The BIOS can verify that the Periodic interrupt was triggered, by reading the PERIODIC bit in the RTC status register at index 7AH. The interrupt is cleared by writing a "1" to the PERIODIC bit in the RTC status register.

Setting the RTC and Power Up Considerations

The internal RTC contains a VALID bit that is reset when SNEPWRGD goes low. This bit is set via program control, and indicates that the RTC time and RAM is valid. When the BIOS or system software initializes the RTC and CMOS RAM, the VALID bit should be set. The VALID bit is contained in the RTC Status register at index 7AH. The BIOS power up routines should read the status of the VALID bit to check the validity of the RTC and the CMOS RAM.

The RTC should be initialized using the following procedure:

1. Enable RTC by clearing *RTCEN bit in RTC mode register
2. Pause RTC by setting UPDATE bit in RTC mode register
3. Initialize RTC Seconds, Minutes, Hours and Day register to proper time.
4. Clear UPDATE bit in RTC mode register.

Note: *When setting the RTC the designer must insure that the PMU does not enter a static DOZE state. If this happens when the RTC is stopped, the RTC will lose time. This can be prevented by using slow-clock DOZE or by having the RTC set routine disable the DOZE timer or trigger activity by a dummy read of an activity monitor address.*

Name: **RTC Mode Register**
Type **Read/Write**
Index: **79H**

D7	D6	D5	D4	D3	D2	D1	D0
*RTCEN	*RAMEN	UPDATE	Reserved	Reserved	Reserved	ALRMINT	PERINT

Bit	Default	Function
D7	0	0 - Enable RTC Clock Index Registers 70-78H access. 1 - Disable RTC Clock Index Registers 70-78H access.
D6	0	0 - Enable RTC CMOS RAM access. 1 - Disable RTC CMOS RAM access.
D5	0	0 - RTC Clock Running. 1 - Pause RTC Clock for setting of Time and/or Alarm values.
D[4:2]	0H	Reserved bits. Read back low.
D1	0	0 - Disable RTC Alarm interrupts. 1 - Enable RTC Alarm interrupts.
D0	0	0 - Disable 1Hz periodic interrupts. 1 - Enable 1Hz periodic interrupts.

When the contents of the alarm registers equal the values in the four corresponding clock registers and the RTC alarm interrupt bit (ALRMINT) bit is set, an alarm interrupt is generated. The BIOS can verify that the alarm interrupt was triggered, by reading the ALARM bit in the RTC status register at index 7AH. The interrupt is cleared by writing a “1” to the ALARM bit in the RTC status register.

Name: **RTC Status Register**
Type **Read/Write**
Index: **7AH**

D7	D6	D5	D4	D3	D2	D1	D0
VALID	Reserved	Reserved	Reserved	Reserved	Reserved	ALARM	PERIODIC

Bit	Default	Function
D7	0	0 - Power to RTC and CMOS RAM has been lost. Contents are not valid. 1 - RTC Clock and CMOS RAM contents valid. *System software sets the VALID bit following initialization of the RTC. VALID is cleared when power to VG230 has been removed.*
D[6:2]	0	Reserved bit. Read back low.
D1	0	0 - No RTC Clock Alarm Pending. 1 - RTC Clock Alarm Pending. *Writing this register with bit D1 set high will clear both the RTCINT signal and the ALARM status bit.*
D0	0	0 - No Periodic Interrupt Pending. 1 - Periodic Interrupt Pending. *Writing this register with bit D1 set high will clear both the RTCINT signal and the ALARM status bit.*

Name: **PMU Status Register**
Type **Read/Write**
Index: **C0H**

D7	D6	D5	D4	D3	D2	D1	D0
RESUME	WU1	WU0	NMI2	NMI1	NMI0	STATE1	STATE0

Bit	Default	Function
D7	0	Resuming from SUSPEND (warmstart)
D[6:5]	00	Wakeup code bits.
D[4:2]	000	NMI cause code bits.
D[1:0]	00	State bits.
Note: *only D0 and D1 are affected by a write.*		

The following table lists the State Codes for a Write to C0H.

State Code								Function
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	0	0	Command to ON.
X	X	X	X	X	X	0	1	Command to DOZE.
X	X	X	X	X	X	1	0	Command to SLEEP.
X	X	X	X	X	X	1	1	Command to SUSPEND.
1	1	1	1	1	X	1	1	Command to OFF.

Note*: The NMI cause, state and wakeup codes are decoded as follows for a read to C0H.*

Wakeup		NMI		State	
Code	Cause	Code	Cause	Code	State
00	None	000	None, or INMI	00	ON
01	EXT	001	EXT	01	DOZE
10	RTC	010	LB	10	SLEEP
11	RI	011	Reserved	11	SUSPEND
		100	SLEEP Timeout		
		101	SUSPEND Timeout		
		110	SLEEP to ON (Activity)		
		111	Reserved		

Name: **PMU Supply Register**
Type **Read Only**
Index: **C1H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	ACTIVITY	Reserved	LB	LOCKOUT

Bit	Default	Function
D[7:4]	0H	Reserved bits.
D3	0	System activity.
D2	0	Reserved bit.
D1	X	Low battery.
D0	1	Register write protected.
Note: *Following a hard reset or RESUME from SUSPEND or OFF modes, the PMU registers are write protected. Software must first read this register before attempting to write any PMU register.*		

Name: **PMU Control Register**
Type **Read/Write**
Index: **C2H**

D7	D6	D5	D4	D3	D2	D1	D0
FSTCLK0	RING2	RING1	RING0	STATIC	SLWREF	Reserved	Reserved

Bit	Default	Function	
D7	0	1 = Disable clock slow down in DOZE and SLEEP modes.	
D[6:4]	001	Bits	RI pulses required for turn-on.
		000	Disable RI
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	7
D3	0	Static CPU and RAM, clock stops in DOZE and SLEEP.	
D2	0	1 = Slow refresh.	
D[1:0]	00	Reserved bit.	

Name: **PMU Activity Mask Register**
Type **Read/Write**
Index: **C3H**

D7	D6	D5	D4	D3	D2	D1	D0
MSK_IORNG	MSK_VIDM	MSK_HD	MSK_FLP	MSK_SIO	MSK_RTC	MSK_KBD	MSK_PIO

Bit	Default	Function
D7	1	Mask access to I/O ports defined by IORNG{6:0].
D6	0	Mask access to video memory.
D5	0	Mask access to hard disk I/O.
D4	0	Mask access to port 3F5.
D3	0	Mask access to COM 1-2.
D2	1	Mask access to port 70H, 71H.
D1	0	Mask keyboard port 60H reads.
D0	0	Mask access to LPT 1, 2, 3.
Note: *The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.*		

Name: **PMU NMI Mask Register**
Type **Read/Write**
Index: **C4H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	MSK_NMI	MSK_SUSPEND	MSK_SLEEP	Reserved	MSK_LB	MSK_EXT	Reserved

Bit	Default	Function
D7	0	Reserved bit.
D6	1	Mask NMI input to PMU.
D5	1	Mask SUSPEND timeout.
D4	1	Mask SLEEP timeout.
D3	1	Reserved bit.
D2	1	Mask LB input.
D1	1	Mask EXT input.
D0	1	Reserved bit.
Note: *An NMI generated by the PMU is cleared by reading the NMI Mask Register.*		

Note: *The NMI vector is ALWAYS located and fetched from ROM. The VG230 will switch memory blocks to access this vector. The memory blocks are returned to their original state by reading the NMI Mask Register, Index C4H, to clear the NMI.*

Name: **PMU I/O Range (IORNG) Register**
Type **Read/Write**
Index: **C5H**

D7	D6	D5	D4	D3	D2	D1	D0
RNGSIZE	IORNG6	IORNG5	IORNG4	IORNG3	IORNG2	IORNG1	IORNG0

Bit	Default	Function
D7	0	0 = 16 byte range, 1 = 8 byte range
D6	0	Maskable I/O range base.
D5	0	Maskable I/O range base.
D4	0	Maskable I/O range base.
D3	0	Maskable I/O range base.
D2	0	Maskable I/O range base.
D1	0	Maskable I/O range base.
D0	0	Maskable I/O range base.
Note: *An NMI generated by the PMU is cleared by reading the NMI Mask Register.*		

PMU Power (PWR) Registers

Name: PMU POWER ON (PWRON) Register
Type: Read/Write
Index: C6H

Name: PMU POWER DOZE (PWRDOZE) Register
Type: Read/Write
Index: C7H

Name: PMU POWER SLEEP (PWRSLEEP) Register
Type: Read/Write
Index: C8H

Name: PMU POWER SUSPEND (PWRSUSPEND) Register
Type: Read/Write (Write 0 to ignore EXT/Write 80 to activate EXT)
Index: C9H

PWRON C6H	PWRDOZE C7H	Bit	PWRSLEEP C8H	PWRSUSPEND C9H	Description
0	1	0	0	0	VPLCD and VPBIAS control.
1	1	1	0	0	Not used.
1	1	2	1	0	VPSYS control.
1	1	3	1	0	VPCARD control.
1	1	4	0	0	Not used.
1	1	5	0	0	Not used.
1	1	6	0	0	Not used.
1	1	7	0	0	VPRAM control.

Register	Default	Index
PWRON	FEH	C6H
PWRDOZE	FFH	C7H
PWRSLEEP	0CH	C8H
PWRSUSPEND	00H	C9H

In each power management state, bits VP7, VP3, VP2 and VP0 of the appropriate PWR register correspond directly to the power control output signals of the VG230. All other bits are unused. VP0 controls the VPLCD and VPBIAS signals after being logically ANDed with the LCD timer output. VP2 controls VPSYS, VP3 controls VPCRD and VP7 controls VPRAM. All bits are logically XNORed with the POLARITY register prior to driving the output signals.

Name: **PMU Polarity Register**
Type: **Read/Write**
Index: **CAH**

This register controls the polarity of the VP outputs. If a logic low is required for a VP signal to turn an external device on, the corresponding bit in the POLARITY register must be set low. If a high is required, the bit must be set high. The polarity of VPLCD and VPBIAS are both set by bit 0 of this register. The default value is FFH.

Name: **PMU Output Register**
Type: **Read**
Index: **CBH**

This read-only register reflects the bit values of the PWR register belonging to the active power management state. For each bit (VP0, VP2, VP3 and VP7) which is ON in the appropriate PWR register, the corresponding bit in the OUPUT register will also be ON. Thus, the OUTPUT register reflects the state of the VG230 VP signals (VPLCD, VPSYS, VPCRD and VPRAM), without taking POLARITY register settings into consideration.

PMU Timer Registers

The PMU has four timers which may be set independently by means of registers. Each has its own range of allowable settings and its own default setting.

Timer Name	Timer Range	Default Setting	Register Index
DOZE	1/8 - 14 sec	4 sec	CCH
SLEEP	1 - 15 min	2 min	CDH
SUSPEND	5 - 75 min	0 (disabled)	CEH
LCD	1 - 15 min	2 min	CFH

Name: **PMU DOZE Timer Register**
Type **Read/Write**
Index: **CCH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	DOZTM3	DOZTM2	DOZTM1	DOZTM0

Bit	Default	Function			
D[7:4]	0000	Reserved bits.			
D[3:0]	1010	Bit	Time	Bit	Time
		0000	Disabled	1000	1 sec
		0001	1/8 sec	1001	2 sec.
		0010	1/4 sec.	1010	4 sec.
		0011	3/8 sec.	1011	6 sec.
		0100	1/2 sec.	1100	8 sec.
		0101	5/8 sec.	1101	10 sec.
		0110	3/4 sec.	1110	12 sec.
		0111	7/8 sec.	1111	14 sec.

Name: **PMU SLEEP Register**
Type **Read/Write**
Index: **CDH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SLPTM3	SLPTM 2	SLPTM 1	SLPTM 0

Bit	Default	Function			
D[7:4]	0000	Reserved bits.			
D[3:0]	1010	**Bit**	**Time**	**Bit**	**Time**
		0000	Disabled	1000	8 min.
		0001	1 min.	1001	9 min.
		0010	2 min.	1010	10 min.
		0011	3 min.	1011	11 min.
		0100	4 min.	1100	12 min.
		0101	5 min.	1101	13 min.
		0110	6 min.	1110	14 min.
		0111	7 min.	1111	15 min.

Name: **PMU SUSPEND Timer Register**
Type **Read/Write**
Index: **CEH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SUSTM3	SUSTM 2	SUSTM 1	SUSTM 0

Bit	Default	Function			
D[7:4]	0000	Reserved bits.			
D[3:0]	1010	**Bit**	**Time**	**Bit**	**Time**
		0000	Disabled	1000	40 min.
		0001	1 min.	1001	45 min.
		0010	2 min.	1010	50 min.
		0011	3 min.	1011	55 min.
		0100	4 min.	1100	60 min.
		0101	5 min.	1101	65 min.
		0110	6 min.	1110	70 min.
		0111	7 min.	1111	75 min.

Name: **PMU LCD Timer Register**
Type **Read/Write**
Index: **CFH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	LCDTM3	LCDTM 2	LCDTM 1	LCDTM 0

Bit	Default	Function			
D[7:4]	0000	Reserved bits.			
D[3:0]	1010	**Bit**	**Time**	**Bit**	**Time**
		0000	Disabled	1000	8 min.
		0001	1 min.	1001	9 min.
		0010	2 min.	1010	10 min.
		0011	3 min.	1011	11 min.
		0100	4 min.	1100	12 min.
		0101	5 min.	1101	13 min.
		0110	6 min.	1110	14 min.
		0111	7 min.	1111	15 min.

Name: **PMU LCD Sequence Register**
Type **Read/Write**
Index: **D4H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	SEQEN	N/U	N/U	Reserved	Reserved

Bit	Default	Function
D[7:5]	---	Reserved bits.
D4	0	Automatic sequencing enable. When SEQEN bit is set, the VG230 performs the LCD power up/down sequencing.
D[3:2]	---	Not used.
D[1:0]	---	Reserved bits.

Name: **PMU Resume Status Register**
Type **Read/Write**
Index: **DAH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PMUREF	CLKSPD

Bit	Default	Function
D[7:2]	00H	Reserved bits.
D1	0	Read only bit polled by software to determine the end of the Resume Operation. PMUREF should be 0 after resume. 1 - PMU Refreshing.
D0	0	CPU Clock speed divider during DOZE or SLEEP mode. 0 - divided by 4; 1 = divided by 8.

Note: *PMUREF should be 0 after RESUME.*

Name: **PMU Activity Status Register**
Type **Read/Write**
Index: **DBH**

The status of the activity monitor can be checked via the ACTIVITY bit in the PMU Supply register. If this bit is set, activity has occurred since the last read of this register. If the ACTIVITY bit is set, the source of the activity can be determined by reading the PMU activity register at index DBH. All bits in the PMU activity register are cleared after being read.

D7	D6	D5	D4	D3	D2	D1	D0
IORNGACT	VIDACT	HDACT	FLPACT	COMACT	RTCACT	KBDACT	PIOACT

Bit	Default	Function
D7	0	Activity to programmable I/O range.
D6	0	Video memory activity.
D5	0	Hard disk I/O activity.
D4	0	Floppy I/O activity.
D3	0	COM1/COM2 activity.
D2	0	I/O Address 70-71H activity.
D1	0	Keyboard I/O activity.
D0	0	LPT1/LPT2/LPT3 I/O activity.
Note: *The activity status register is cleared following deassertion of the SNEPWRGD signal, or after being read by the CPU.*		

The following registers are implemented in the VG230 Single-Chip PC Platform to assure IBM CGA compatibility. These registers are accessed through an index and a data register. The index register is at 3D4 and the data register is at 3D5. Both registers are read/write and are shadowed at 3D0/3D1, 3D2/3D3 and 3D6/3D7 respectively. The address is decoded using A0-9 and AEN=0 (the PC/XT uses only A0-9). The 6845 registers R1-R9 are used to program the display characteristics for a CRT. They have no meaning for an LCD and are therefore not implemented here.

Name: **CGA Index Register**
Type: **Read/Write**
Address: **3D4H**

Note: *The Index register is shadowed at 3D0, 3D2 and 3D6*

Name: **CGA Data Register**
Type: **Read/Write**
Address: **3D5H**

Note: *The Index register is shadowed at 3D1, 3D3 and 3D7*

Name: **Mode Select Register A**
Type: **Read/Write**
Address: **3D8H**

Name: **Status Register**
Type: **Read**
Address: **3DAH**

Name: **Mode Select Register** B
Type: **Read/Write**
Address: **3DEH**

CGA LCD Indexed Register Summary

Register Indices

The following register indices select among the CGA LCD indexed registers:

REGISTER	INDEX
Cursor Start Raster Register	0AH
Cursor End Raster Register	0BH
Display Start Address MSB Register	0CH
Display Start Address LSB Register	0DH
Cursor Location Address MSB Register	0EH
Cursor Location Address LSB Register	0FH

The following registers control VG230 extended LCD features: *windowing, LCD type, timeout delays, LCD resolution and the ink plane.*

Window Start MSB Register	C0H
Window Start LSB Register	C1H
LCD Display Control Register	C2H
LCD Panel Resolution Register	CAH
LCD Mode Register	CCH
Ink Plane Register	CDH

Name: **Cursor Start Raster Register**
Type **Read/Write**
Index: **0AH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	*CURON	SC4	SC3	SC2	SC1	SC0

Bit	Default	Function
D[7:6]	00	Not used.
D5	0	0 - Cursor displayed. 1 - Cursor not displayed.
D[4:0]	00H	Select raster to start cursor. 00 = line 0, 01 = line 1, 02 = line 2, etc.

Name: **Cursor End Raster Register**
Type **Read/Write**
Index: **0BH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	EC4	EC3	EC2	EC1	EC0

Bit	Default	Function
D[7:5]	000	Not used.
D[4:0]	0H	Select raster to end cursor. 00 = line 0, 01 = line 1, 02 = line 2, etc.

Name: **Display Start Address MSB Register**
Type **Read/Write**
Index: **0CH**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D[7:6]	Not used.
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8
Note: *Holds the upper byte of address for the character at the upper left corner of a normal CGA display. See Window Start MSB Register.*	

Name: **Display Start Address LSB Register**
Type **Read/Write**
Index: **0DH**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0
Note: *Holds the lower byte of address for the character at the upper left corner of a normal CGA display. See Window Start LSB Register.*	

Name: **Cursor Location Address MSB Register**
Type **Read/Write**
Index: **0EH**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D[7:6]	Not used.
D5	13
D4	12
D3	11
D2	10
D1	9
D0	8
Note: *Holds the upper byte of the cursor location address.*	

Name: **Cursor Location Address LSB Register**
Type **Read/Write**
Index: **0FH**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0
Note: *Holds the lower byte of the cursor location address.*	

VG230-Specific CGA LCD Controller Registers

The following registers are specific to the VG230 CGA LCD Controller. They are accessed via the same Index and Data addresses as the previously described CGA-compatible registers. These registers are used to configure the VG230 LCD controller. They control windowing, LCD type and resolution, set time-out delays, and control related PMU functions.

The standard Display Start Address MSB and LSB Registers address a display area of 640 x 200. The VG230 provides the additional Window Start MSB and LSB Registers to address smaller displays. When the VG230 LCD Controller is configured for a display that is smaller than 640 x 200, software writes and reads intended for the Display Start Address MSB and LSB registers are redirected by the BIOS to the Window Start MSB and LSB Registers. This redirection is totally transparent to the software and user.

Name: **Window Start MSB Register**
Type **Read/Write**
Index: **C0H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D[7:5]	Not used.
D4	12
D3	11
D2	10
D1	9
D0	8
Note: *The Window Start registers contain the memory address for the upper left corner of the LCD panel. Writes to index 0CH are automatically copied to this register.*	

Name: **Window Start LSB Register**
Type **Read/Write**
Index: **C1H**

D7	D6	D5	D4	D3	D2	D1	D0

Bit	Function
D7	7
D6	6
D5	5
D4	4
D3	3
D2	2
D1	1
D0	0
Note: *Writes to index 0DH are automatically copied to this register.*	

Name: **LCD display Control Register**
Type **Read/Write**
Index: **C2H**

D7	D6	D5	D4	D3	D2	D1	D0
ATTBLK1	ATTBLK0	CURBLK1	CURBLK0	Reserved	Reserved	Reserved	RVVD

Bit	Default	Function		
D[7:6]	00	Controls blink rate for character blink attribute.		
		Bit 7	Bit 6	
		0 0 1 1	0 1 0 1	Steady 1/64 frame 1/32 frame 1/16 frame
D[5:4]	00	Controls blink rate for the cursor in conjunction with bit 5 of the Cursor Start Scan Line Register.		
		Bit 5	Bit 4	
		0 0 1 1	0 1 0 1	Steady 1/64 frame 1/32 frame 1/16 frame
D[3:1]	000	Reserved bits.		
D0	0	Reverse video for entire LCD. 0 = Normal polarity. 1 = LCD in reverse video.		

ATTBLK[1:0] control the rate at which a character blinks. The value written to these bits determines whether a character remains steady or blinks at various rates.

CURBLK[1:0] along with bit 5 of the Cursor Start Raster Register determine the blink rate of the cursor.

RVVD controls the polarity of the LCD display. The default value is for normal polarity. Setting this bit high reverses the video of the entire display.

Name: **LCD Panel Resolution Register**
Type **Read/Write**
Index: **CAH**

D7	D6	D5	D4	D3	D2	D1	D0
LCDW1	LCDW0	LCDR5	LCDR4	LCDR3	LCDR2	LCDR1	LCDR0

Bit	Default	Function	
D[7:6]	00	LCD data bus width. 00-4, 01=2 bit, 10=1 bit, 11=not used	
D[5:0]	000000	LCDR[5:0]	Panel Resolution
		000000	640x400
		000000	640x200
		000010	640x100
		001001	480x128
		010011	240x64
		011001	128x128
		011011	128x64
		100000	320x200
		100101	320x240

LCDW[1:0] are used to select the proper LCD data bus width required for the LCD panel. Large panels usually require a 4 bit data bus. Smaller panels may require a 2 bit or 1 bit data bus. Table 2.5-2 gives the data pin names for 4 bit, 2 bit, and 1 bit wide LCD data bus requirements.

Name: **Gray Scale Register**
Type **Read/Write**
Index: **CBH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	OPT2401	OPT2400	Reserved	Reserved

Bit	Default	Function	
D[7:4]	0H	Reserved bits.	
D[3:2]	00	320 x 240 panel image control options.	
		OPT240[1:0]	Option
		00	Display the 200 CGA lines in the top 200 lines of the panel. Remaining 40 lines are fetched form subsequent memory.
		01	As above, but remaining 40 lines are blanked.
		10	Reserved.
		11	Center the 200 CGA lines in the 240 panel lines. Remaining 40 lines (20 above and 20 below image) are blanked.
D[1:0]	00	Reserved.	

Name: **LCD Mode Register**
Type **Read/Write**
Index: **CCH**

D7	D6	D5	D4	D3	D2	D1	D0
SEL60HZ	Reserved	DLY2	DLY1	DLY0	400LINE	Toshiba	Sharp

Bit	Default	Function
D7	0	Frame Rate for LCD Widths

SEL60HZ Value	Clock MHz	640;320 Hz	480;240 Hz	128 Hz
0	14.3	69	72	67
0	16	72	75	70
1	14.3	60	62	58
1	16	59	62	57

Bit	Default	Function
D6	0	Reserved bit.
D[5:3]	000	LCD Sequencing Delay Setting

DLY2	DLY1	DLY0	Sequencing Delay
0	0	0	7.5ms
0	0	1	15ms
0	1	0	30ms
0	1	1	60ms
1	0	0	120ms
1	0	1	240ms
1	1	X	Reserved

Bit	Default	Function
D2	0	400 line select. 0 - LCD is 640x200 resolution or lower. 1 - LCD is 640x400 lines.
D1	0	1 - Toshiba LOADCLK Timing.
D0	0	1 - Sharp LOADCLK Timing.
Note: *For physical 400-line panels, the lower 4 data bits to the panel (LCDL[3:0]) must be explicitly enabled using the GPIO Mode Register (index 32H).*		

SEL60HZ (bit D7) is used to select the frame rate frequency. The FRAME output is measured in Hz and is based on the CPUCLK. The value written to SEL60HZ selects the proper frame rate for the different panel widths supported. The actual frame rate is dependent upon the CPUCLK frequency and the setting of SEL60HZ.

LCD panels have different power sequencing requirements. The DLY[2:0] bits control the delay interposed between power sequencing events to meet the requirements of the specific panel in the system.

400LINE (bit D2) in conjunction with the LCD Panel Resolution Register are used to configure the VG230 LCD controller for the various supported panel resolutions. For panels of 64, 128, and 200 lines, the 400LINE bit must be set low. Setting 400LINE high normally is used for 400 line panels.

The Toshiba (bit D1) and Sharp (bit D0) register bits are used to provide the proper LOADCLK timing. Toshiba and Sharp panels require specific LOADCLK timings. When a Toshiba or Sharp LCD panel is used, setting the appropriate bit high enables the correct LOADCLK timing for that panel. When both these bits are low, the generic LOADCLK timing is selected. The generic LOADCLK timing is valid for most LCD panels other than Toshiba or Sharp.

Name: **Ink Plane Register**
Type **Read/Write**
Index: **CDH**

D7	D6	D5	D4	D3	D2	D1	D0
INKEN	Reserved	Reserved	Reserved	Reserved	Reserved	IMOD1	IMOD0

Bit	Default	Function
D[7:4]	0	0 - Disable Ink Plane. 1 - Enable Ink Plane. When this bit is set and the VG230 is programmed into 400 line mode, the lower half screen data will be logically superimposed on the upper half screen data to drive the LCDU[3:0] outputs.
D[6:2]	0	Reserved bits.
D[1:0]	00	Selects method of combining upper half screed data and lower half screen data.

IMOD1	IMOD0	
0	0	Modulate
0	1	OR
1	0	XOR
1	1	Reserved

The following registers are implemented in the VG230 Single-Chip PC Platform to assure IBM CGA compatibility. These registers are accessed through an index and a data register. The index register is at 3D4 and the data register is at 3D5. Both registers are read/write and are shadowed at 3D0/3D1, 3D2/3D3 and 3D6/3D7 respectively. The address is decoded using A0-9 and AEN=0 (the PC/XT uses only A0-9). The 6845 registers R1-R9 are used to program the display characteristics for a CRT. They have no meaning for an LCD and are therefore not implemented here.

Name: **CGA Index Register**
Type: **Read/Write**
Address: **3D4H**

Note: *The Index register is shadowed at 3D0, 3D2 and 3D6*

Name: **CGA Data Register**
Type: **Read/Write**
Address: **3D5H**

Note: *The Index register is shadowed at 3D1, 3D3 and 3D7*

Name: **Mode Select Register A**
Type **Read/Write**
Index: **3D8H**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	BLINK	GRES0	VIDE	Reserved	GRAPH	CRES

Bit	Default	Function
D[7:6]	00	Reserved bits.
D5	0	0 - MSB of Attribute Byte is intensity. 1 - MSB of Attribute Byte is blink.
D4	0	0 - 320x200 APA 1 - 640x200 APA or 640x400 APA
D3	0	0 - Video disabled. 1 - Video enabled. ***Note:*** *Used by power management logic only, does not actually control video.*
D2	0	Reserved bit.
D1	0	0 - Character mode. 1 - Graphics mode.
D0	0	0 - 40x25 Alpha. 1 - 80x25 Alpha.

In text mode, the BLINK bit (D5) is used to identify the function of the most significant bit of the character Attribute Byte. When this bit is reset low, the Attribute Byte MSB controls the intensity of the character. When this bit is set high the MSB of the character Attribute Byte controls the character blink.

GRES0 (bit D4), GRAPH (bit D1), and CRES (bit D0) are used in conjunction with GRES1 (bit D0) of the Mode Select Register B, to control the AT&T mode of display. VIDE (bit D3) is used by the VG230 PMU to determine whether the LCD panel should be turned on or off.

Name: **Status Register**
Type **Read/Write**
Index: **3DAH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	VSYNC	Reserved	Reserved	HSYNC

Bit	Default	Function
D[7:4]	FH	Reserved bits.
D3	0	Simulated vertical retrace time.
D2	1	Reserved bit.
D1	0	Reserved bit.
D0	0	Simulated horizontal retrace time.

Name: **Mode Select Register B**
Type **Read/Write**
Index: **3DEH**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	UNDRLN	Reserved	PAGSEL	VSYNC	Reserved	Reserved	GRES1

Bit	Default	Function
D7	0	Reserved bit.
D6	0	0 - Underline disabled, grayscaling enabled. 1 - Underline enabled, grayscaling disabled.
D[5:4]	00	Reserved bits.
D3	0	0 - Select low page for display. 1 - Select high page for display.
D[2:1]	00	Reserved bits.
D0	0	0 - 640x200 APA, two 16K alpha pages. 1 - 640x400 APA, one 32K alpha page.

GRAPH, CRES and GRES[1:0] are used to select the ATT mode.

GRAPH	CRES	GRES1	GRES0	Mode
0	0	X	X	40x25 Alpha
0	1	X	X	80x25 Alpha
1	X	X	0	320x200 APA
1	X	0	1	640x200 APA
1	X	1	1	640x400 APA

NOTES

SPECIFICATIONS
AND
CHARACTERISTICS

NOTES

SPECIFICATIONS

This chapter details the device specifications and characteristics of the VG230 Single-Chip PC Platform.

Processor

Type	V30HL	
Max Input Clock Frequency	32.215905 MHz	
Input Clock Frequencies Supported	32.215905 MHz	28.63636 MHz
(Maximum)	16.0 MHz (÷ 2)	14.3 MHz (÷ 2)
	10.7 MHz (÷ 3)	9.54 MHz (÷ 3)
CPU Clock Frequencies	8.00 MHz (÷ 4)	7.12 MHz (÷ 4)
	5.33 MHz (÷ 6)	4.77 MHz (÷ 6)
(Minimum)	4.00 MHz (÷ 8)	3.58 MHz (÷ 8)

I/O

Serial Port	8250 Based. Programmable as COM1 or COM2.
Interrupts	8259 Based. 2 channels available on bus (programmable).
DMA	8237 Based. 1 channel available on bus (programmable).
Timer	8254 Based. Provides Speaker I/F.
RTC	Includes 64 bytes of CMOS RAM.
Expansion	Supported though Single Bus. I/O channel is user-programmable to operate at CPU frequency or 1/2, 1/3, or 1/4 CPU frequency.

Configurable I/O

	Configuration 1	Configuration 2
Keyboard I/F*	Built-in keyboard scanner supporting 8x12 key matrix with 5 dedicated shift keys (101 keys total).	PC/XT compatible two line serial keyboard I/F.
Parallel Port	None.	PC/XT Compatible. (Requires external parallel data latch).
PC Card I/F	One PCMCIA 2.1 Memory or I/O Card Slot supported.	Two PCMCIA 2.1 Memory or I/O Card Slots supported.

**Keyboard I/F itself may be disabled to allow implementation of separate keyboard controller.*

Power Management

CPU Clock Control	Divide by 4, 8, or Stop Clock
Power Control Pins (VP Pins)	2 for LCD 1 for PC Cards 1 for RAM 1 for System On/Off
Modes	On, Doze, Sleep, Suspend, and Off
Battery Monitoring	1 level (LB)
Suspend/Resume Control	Via EXT switch, RTC Alarm, Ring Indicator

LCD Controller

Supported Modes	AT&T 400 line Graphics, Double-Scan Text and Graphics, CGA Text and Graphics
Displays Supported	640x400, 640x200, 640x100, 480x128, 320x200, 240x128, 240x64, 128x128, 128x64 and 320x240

VG230 Memory Cycle Behaviors

	Memory Type: SRAM		Memory Type: PSRAM		Memory Type: DRAM	
	x8	x16	x8	x16	x8	x16
Cycle Type: Fast	3 cycles: *CS - 2 / 1 *OE - 1.5	4 cycles: *CS - 3 / 1 *OE - 2.5	3 cycles: *CE - 2 / 1 *OE - 1.5	4 cycles: *CE - 3 / 1 *OE - 2.5	3 cycles: *RAS - 2 / 1 *CAS - 1	4 cycles: *RAS - 2 / 2 *CAS - 1
Cycle Type: Normal	4 cycles: *CS - 2 / 2 *OE - 1.5	5 cycles: *CS - 3 / 2 *OE - 2.5	4 cycles: *CE - 2 / 2 *OE - 1.5	5 cycles: *CE - 3 / 2 *OE - 2.5	4 cycles: *RAS - 2 / 2 *CAS - 1	5 cycles: *RAS - 3 / 2 *CAS - 2
Cycle Type: Slow	5 cycles: *CS - 3 / 2 *OE - 2.5	6 cycles: *CS - 4 / 2 *OE - 3.5	5 cycles: *CE - 3 / 2 *OE - 2.5	6 cycles: *CE - 4 / 2 *OE - 3.5	5 cycles: *RAS - 3 / 2 *CAS - 2	6 cycles: *RAS - 3 / 3 *CAS - 2

Remark:
"3 cycles" ***means 3 VID_TCYC or CPU_TCYC clock periods, whichever determ ines the maximum allowable memory access time.***
"*CS - 2 /1" ***means *CS signal is active for 2 clock periods and inactive for 1 clock period.***
"*OE - 1.5" ***means *OE signal is active for 1.5 clock period.***

Cycle type is set by writing D[6:5] bits of LCD Configuration Control Register, 07h. Display memory in VG230 is embedded in the main memory. Display cycle demands the highest memory performance if high resolution display panel is employed, ie 640x200 or 640x400. Normally, it sets the memory speed requirement for the whole system . By choosing these bits appropriately, memory performance, power and memory cost can be optimized for a given display panel size and X1 input frequency.

A.C. Test Conditions

Output Load I(load) = ± 200 µA (5V and 3.3V)
C(load) = 50pF (5V and 3.3V)

Input Rise and Fall Times 5 ns. maximum (5V) 3ns. maximum (3.3V)

Timing Measurement Reference level Inputs: 0.8V and 2.0V (5V and 3.3V)
Outputs: 0.45V and 2.4V (5V and 3.3V

Mechanical Specifications

Package 160 pin QFP

5V

5V Electrical Characteristics

Supply Voltage 5V +/- 5%

DC Characteristics

Parameter	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	-	0.8	volt.
Input High Voltage	V_{IH}	2.1	-	volt.
Output Low Voltage (TTL & CMOS)	V_{OL}	0	0.45	volt.
Output High Voltage (TTL)	V_{OHT}	2.4	-	volt.
Output High Voltage (CMOS)	V_{OHT}	3.5	-	volt.
Input Low Current	I_{IL}	-	-20	µA
Input High Current Vin = 2.4v, Vcc = 5.5v	I_{IH1}	-	20	µA
Input High Current Vin = 5.5v, Vcc = 5.5v	I_{IH2}	-	200	µA
Output Short Circuit Current Vo = Ov	I_{OS}	-	-100	mA
Input Clamp Voltage II = 020mA, Vcc = 4.5v	V_{IC}	-	-1.5	volt.
Output Leakage Current (Hi-Z)	I_{OLZ1}	-20	20	µA
Output Leakage Current (Bi-Dir)	I_{OLZ2}	-20	20	µA
NOTE: *Entire device max = 1mA*				

5V

Absolute Maximum Ratings

Case Temperature Under Bias	-25 to + 100 C
Case Storage Temperature	-40 to +125 C
DC Supply Voltage	0 to 7.0V
Voltage to any pin with respect to ground	-0.5V to Vcc +0.5V

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage (5 volt)	4.75	5.25	V
Freq	Operating Frequency	-	32.216	MHz
Ta	Ambient Temperature	0	70	C

Capacitance DC Specifications

Symbol	Parameter	Min.	Max.	Unit	Note
Cin	Input Capacitance	-	10	pF	1
Cout	Output Capacitance	-	10	pF	1

ICC Specifications

Symbol	Parameter	Typ.	Unit	Note
ICC_1	Supply Current @ 8 MHz	60	mA	2
ICC_2	Supply Current @ 16 MHz	90	mA	2
ICC_3	Supply Current under SUSPEND	80	μA	3

Electrostatic Discharge Characteristics

Symbol	Parameter	Value	Test Condition
Vzap	E.S.D. Tolerance	>1500V	Mil-STD 883 Meth. 3015

Notes: 1. @ 1MHz
2. ON Mode

5V

VG230 5V TIMING TABLE

- **CPU_TCYC = (X1 period) ÷ (value set by D[7:5] of Index Reg. [01h]) min. period = 62.1ns (max freq. = 16.1MHz)**
- **SYS_TCYC = CPU_TCYC ÷ (value set by D[1:0] of Index Reg. [01h]) min. period = 124.2ns (max. freq. = MHz)**
- **VID_TCYC = (X1 period) ÷ 2min. period = 62.1ns (max freq. = 16.1mhz)**

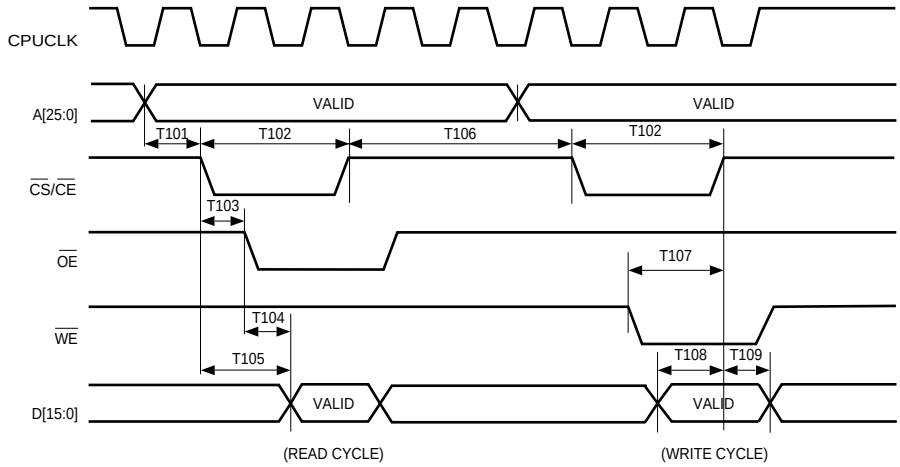
Memory Cycle Timing

Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	Memory Cycle Timing (Wait State = 0)			
T101	ADDR setup time to *CS/*CE/*RAS↓	-	0.5*CPU_TCYC	-
T102	*CS/*CE/*RAS pulse width	2*CPU_TCYC - 10ns	-	-
T103	*OE↓ delay from *CS/*CE/*RAS↓	-	0.5*CPU_TCYC	-
T104	DATA valid from *OE↓ (read)	-	-	1.5*CPU_TCYC - 20ns
T105	DATA valid from *CS/*CE↓ (read)	-	-	2*CPU_TCYC - 20ns
T106	*CS/*CE/*RAS precharge time	2*CPU_TCYC - 10ns	-	-
T107	*WE↓ setup time to *CS/*CE↑ (write)	1.5*CPU_TCYC	-	-
T108	DATA setup time to *CS/*CE↑ (write)	-	1.5*CPU_TCYC	-
T109	DATA hold time from *CS/*CE↑ (write)	-	0.5*CPU_TCYC	-
T110	ADDR hold time from *RAS↓	-	0.5*CPU_TCYC	-
T111	ADDR setup time to *CAS↓	-	0.5*CPU_TCYC	-
T112	*CAS↓ delay from *RAS↓	-	-	1*CPU_TCYC
T113	*CAS pulse width	1*CPU_TCYC - 10ns	-	-
T114	DATA valid from *RAS↓ (read)	-	-	2*CPU_TCYC - 20ns
T115	DATA valid from *CAS↓ (read)	-	-	1*CPU_TCYC - 20ns
T116	DATA setup time to *CAS↓ (write)	-	0.5*CPU_TCYC	-
T117	DATA hold time from *CAS↓ (write)	-	0.5*CPU_TCYC	-
T118	*WE↓ setup time to *CAS↓	-	0.5*CPU_TCYC	-

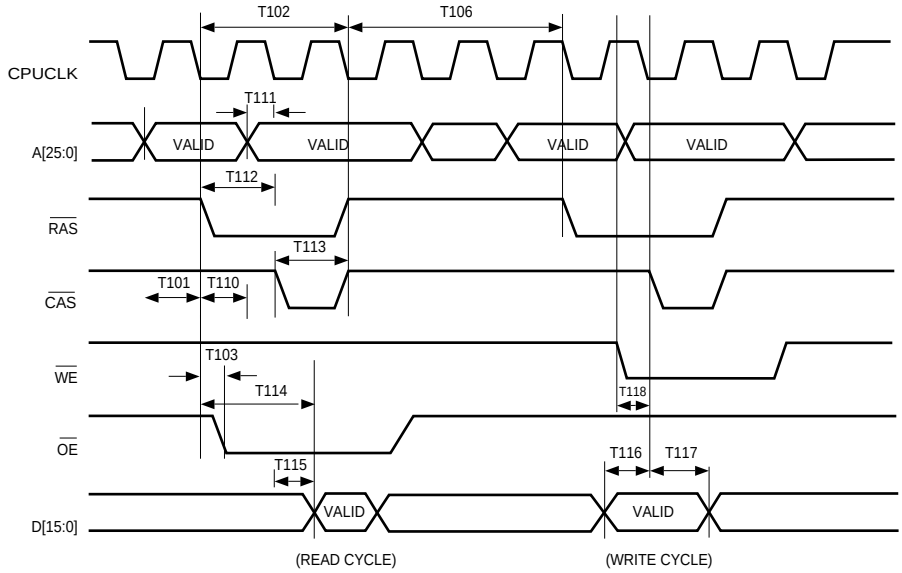
5V

MEMORY CYCLE TIMING

SRAM/PSRAM



DRAM Timing

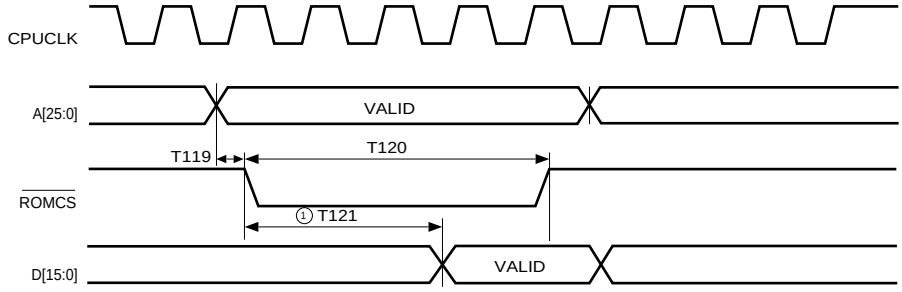


5V

MEMORY CYCLE TIMING (continued)

T119	ADDR setup time to *ROMCE[1:0]↓	-	0.5*CPU_TCYC	-
T120	*ROMCE[1:0] pulse width	2*CPU_TCYC - 10ns	-	-
T121	DATA valid from *ROMCE[1:0]↓	-	-	2*CPU_TCYC - 20ns

ROM Timing



① **Note:**

T121: Parameter shown in table, wait state = 0.

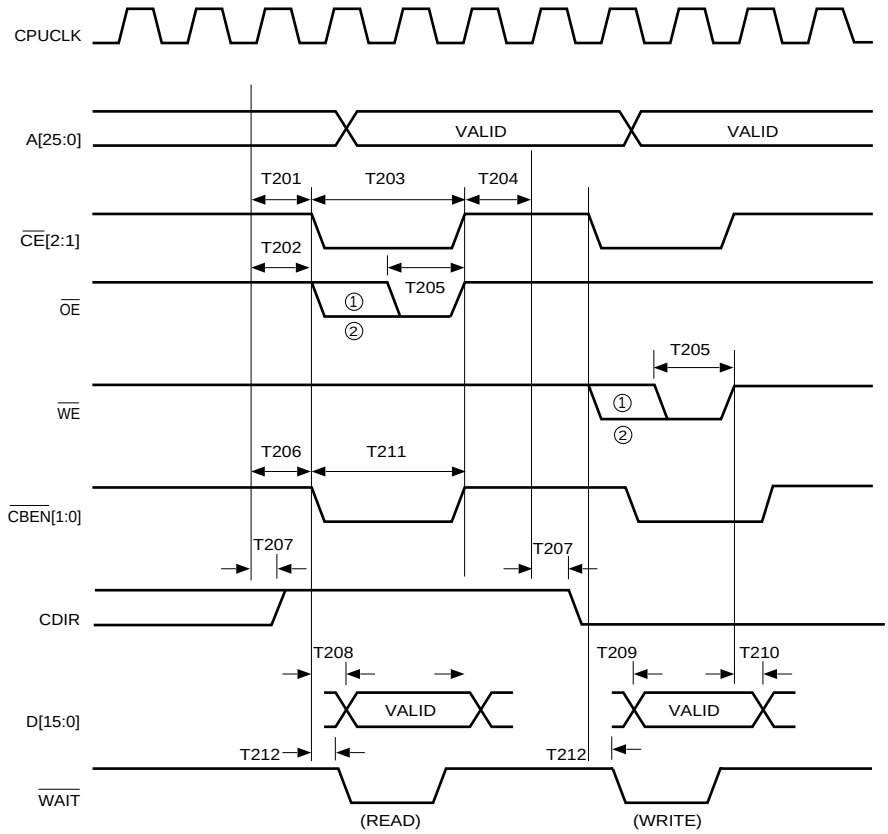
5V

PC CARD MEMORY CYCLE TIMING

Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	PCCARD Memory Cycle Timing (Wait State = 0)			
T201	ADDR delay from *CE[2:1]↓	-	-	0.5*CPU_TCYC
T202	*OE/*WE↓ delay from *CE[2:1]↓	-	1*CPU_TCYC	-
T203	*CE[2:1] pulse width	2.5*CPU_TCYC - 10ns	-	-
T204	ADDR hold time from *CE[2:1]↑	-	0.5*CPU_TCYC	-
T205	*OE/*WE pulse width	2*CPU_TCYC - 10ns	-	-
T206	ADDR delay from *CBEN[1:0]↓	-	-	0.5*CPU_TCYC
T207	CDIR setup time to *CE[2:1]/*CBEN[1:0]↓	-	1*CPU_TCYC	-
T208	DATA valid from *OE↓ (read)	-	-	2*CPU_TCYC - 20ns
T209	DATA setup time from *CE[2:1]/*WE↑ (write)	-	1*CPU_TCYC	-
T210	DATA hold time from *CE[2:1]/*WE↑ (write)	-	0.5*CPU_TCYC	-
T211	*CBEN[1:0] pulse width	2.5*CPU_TCYC - 10ns	-	-
T212	*WAIT delay from *OE/*WE↓	-	-	1*CPU_TCYC - 10ns

5V

PC Card Memory Timing



Notes:

① OE/WE may be delayed 0, 1, 2, or 3 clocks from the falling edge of CE under software control.

② When enabling OE/WE command delay, an additional number of wait states are added to the PC Card Memory cycle to match the OE/WE delay value.

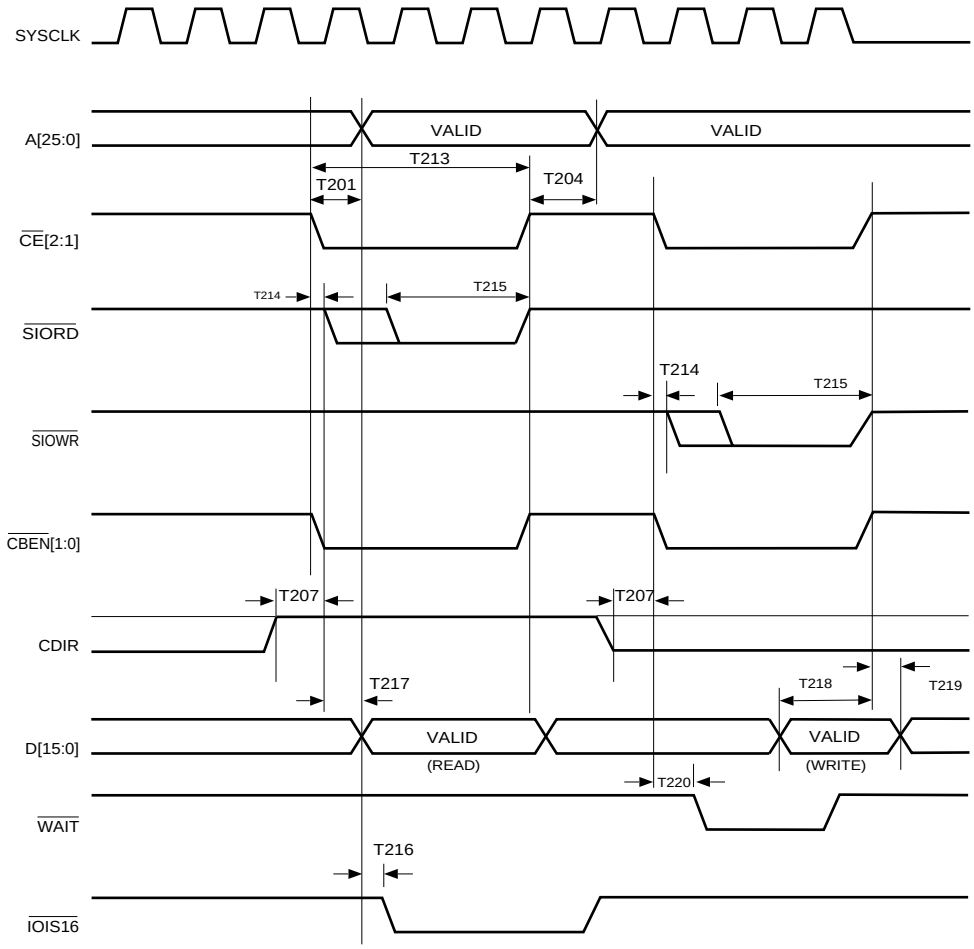
5V

PC CARD I/O CYCLE TIMING

Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	PCCARD I/O Cycle Timing (Wait State = 0)			
T201	ADDR delay from *CE[2:1]⇓	-	-	0.5*CPU_TCYC
T204	ADDR hold time from *CE[2:1]⇑	-	0.5*CPU_TCYC	-
T207	CDIR setup time to *CE[2:1]/*CBEN[1:0]⇓	-	1*CPU_TCYC	-
T213	*CE[2:1] pulse width	3*SYS_TCYC - 10ns	-	-
T214	*SIORD/*SIOWR⇓ delay from *CE[2:1]⇓	-	0.5*SYS_TCYC	-
T215	*SIORD/*SIOWR pulse width	2*SYS_TCYC - 10ns	-	-
T216	ADDR setup time to *IOIS16A⇓		-	1*SYS_TCYC - 10ns
T217	DATA valid from *SIORD⇓ (read)	-	-	2*SYS_TCYC - 20ns
T218	DATA setup time from *SIOWR/*CE[2:1]⇑ (write)	1*SYS_TCYC	-	-
T219	DATA hold time from *SIOWR/*CE[2:1]⇑ (write)	-	0.5*SYS_TCYC	-
T220	*WAIT⇓ delay from *CE[2:1]⇓	-	-	0.5*SYS_TCYC - 20ns

5V

PC Card I/O Timing



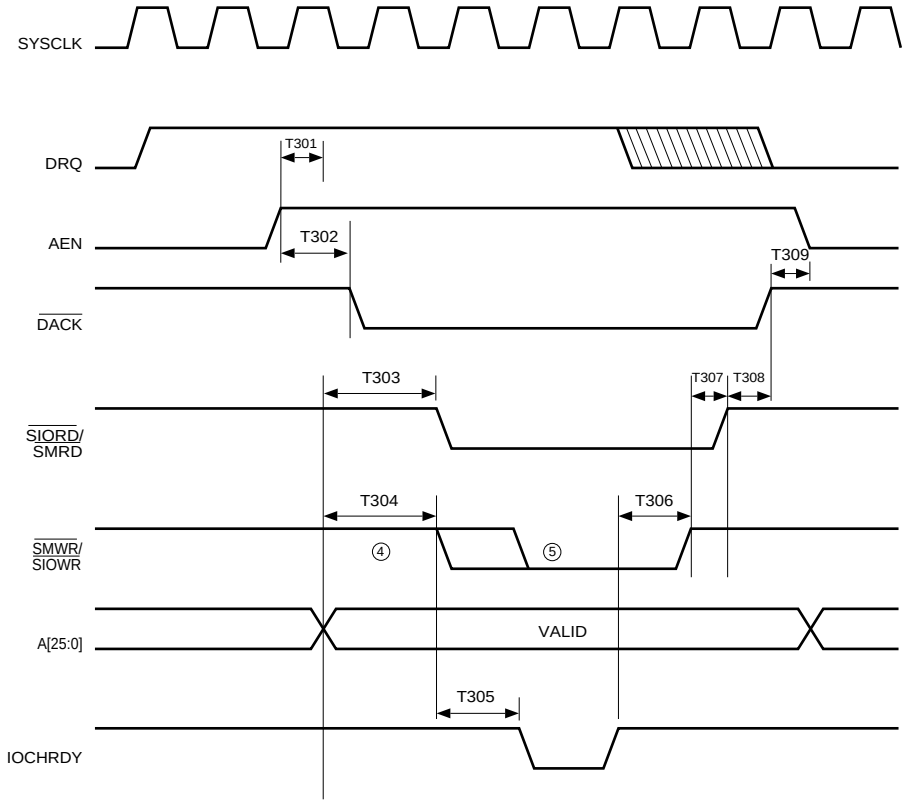
5V

DMA CYCLE TIMING

Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	DMA Cycle Timing			
T301	AEN↑ to ADDR valid	-	0.5*SYS_TCYC	-
T302	*DACK↓ delay from AEN↑	-	0.5*CPU_TCYC	-
T303	ADDR setup time to *SMRD/*SIORD↓	-	0.5*SYS_TCYC	-
T304	ADDR setup time to *SMWR/*SIOWR↓	-	1.5*SYS_TCYC	-
T305	IOCHRDY↓ delay from *SMRD/*SIORD↓	-	-	1*SYS_TCYC - 10ns
T306	*SMRD/*SIORD↑ delay from IOCHRDY release	-	1*SYS_TCYC	-
T307	*SMRD/*SIORD↑ delay from *SIOWR/*SMWR↑	-	1*SYS_TCYC	-
T308	*DACK↑ delay from *SMRD /*SIORD↑	-	0.5*SYS_TCYC	-
T309	AEN↓ delay from *DACK↑	-	0.5*CPU_TCYC	-

5V

DMA Timing



Notes:

T304: ④ SIOWR/SMWR leading edge may be delayed 0, 1, 2, or 3 clocks after the leading edge of SIORD/SMRD.

⑤ For all DMA cycles, SIOWR/SMWR is active for at least 3 clock cycles.

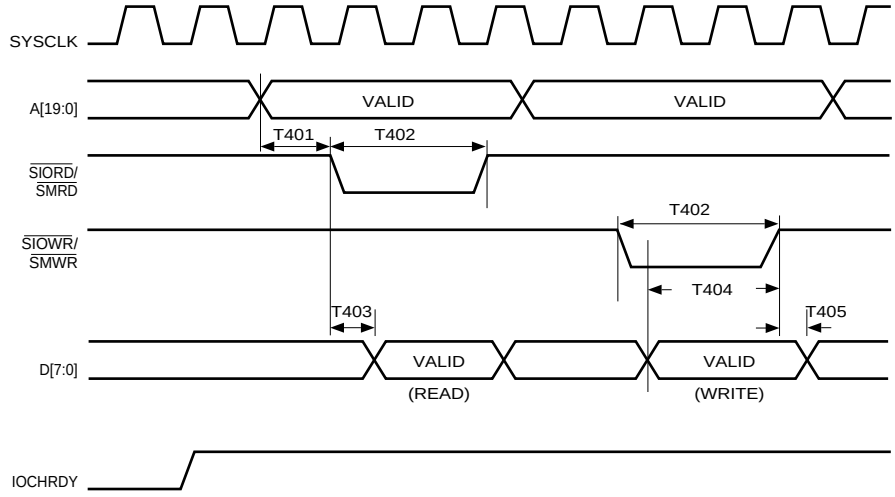
5V

EXTERNAL BUS TIMING

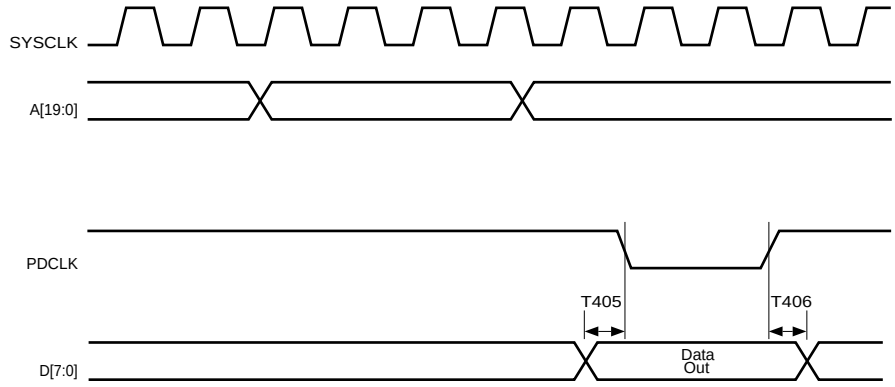
Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	External Bus Timing			
T401	ADDR setup time to *SMRD/*SMWR/*SIORD/*SIOWR↓	-	0.5*SYS_TCYC	-
T402	*SMRD/*SMWR/*SIORD/*SIOWR pulse width	2*SYS_TCYC - 10ns	-	-
T403	DATA valid from *SMRD/*SIORD↓	-	-	2*SYS_TCYC - 20ns
T404	DATA setup time from *SMWR/*SIOWR↑ (write)	-	0.5*SYS_TCYC	-
T405	DATA hold time from *SMWR/*SIOWR↑ (write)	-	0.5*SYS_TCYC	-
T406	DATA hold time from *SMWR/*SIOWR↑ (write)	-	0.5*SYS_TCYC	-

5V

XT Bus Timing



PIO Timing

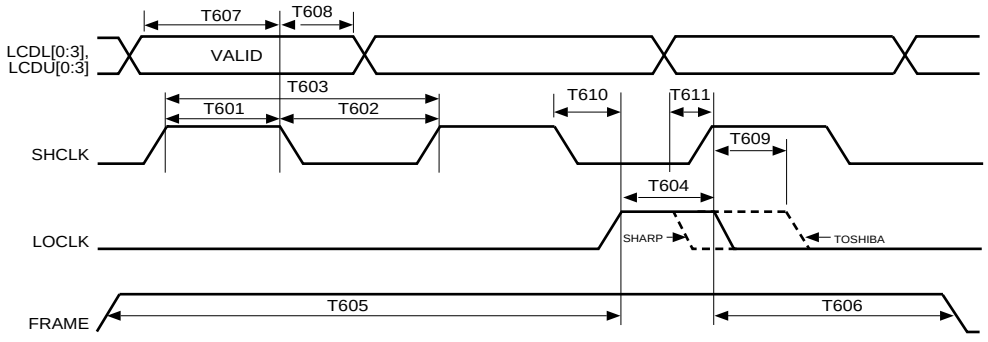


5V

LCD TIMING

Items	*Descriptions*	*5V Datasheet*		
		min.	*typ.*	*max.*
	LCD Timing			
T601	SHCLK high time	3*VID_ TCYC- 10ns	-	-
T602	SHCLK low time	3.5*VID_ TCYC- 10ns	-	-
T603	SHCLK cycle time	6.5*VID_ TCYC- 10ns	-	-
T604	LOCLK width, generic timing	3*VID_ TCYC- 10ns	-	-
	LOCLK width, SHARP timing	2.5*VID_ TCYC- 10ns	-	-
	LOCLK width, TOSHIBA timing	5*VID_ TCYC- 10ns	-	-
T605	FRAME setup time to LOCLK↑	800 ns	-	-
T606	FRAME↓ delay from LOCLK↓	800 ns	-	-
T607	Pixel Data setup time to SHCLK↓	4.5*VID_ TCYC - 10ns	-	-
T608	Pixel Data hold time to SHCLK↓	2*VID_ TCYC - 10ns	-	-
T609	LOCLK↓ (TOSHIBA) delay from SHCLK↑	2*VID_ TCYC - 10ns	-	-
T610	LOCLK↑ delay from SHCLK↓	0.5*VID_ TCYC - 10ns	-	-
T611	LOCLK↓ (SHARP) setup time to SHCLK↑	0.5*VID_ TCYC - 10ns	-	-

LCD Timing



NOTES ✎

3.3V

3.3V Electrical Characteristics

Supply Voltage 3.3V +/- 5%

DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}	-	0.6	volt.
Input High Voltage	V_{IH}	2.4	-	volt.
Output Low Voltage	V_{OL}	0	0.4	volt.
Output High Voltage	V_{OHT}	2.4	-	volt.
Input Low Current	I_{IL}	-	-10	µA
Input High Current Vin = 2.4v, Vcc = 3.6v	I_{IH1}	-	10	µA
Input High Current Vin = 3.6v, Vcc = 3.6v	I_{IH2}	-	20	µA
Output Short Cicuit Current Vo = Ov	I_{OS}	-	-100	µA
Output Leakage Current (Hi-Z)	I_{OLZ1}	-10	10	µA
Output Leakage Current (Bi-Dir)	I_{OLZ2}	-10	10	µA

3.3V

Absolute Maximum Ratings

Case Temperature Under Bias	-25 to + 100 C
Case Storage Temperature	-40 to +125 C
DC Supply Voltage	0 to 7.0V
Voltage to any pin with respect to ground	-0.5V to Vcc +0.5V

Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage (3.3 volt)	3.15	3.45	V
Freq	Operating Frequency	-	32.216	MHz
Ta	Ambient Temperature	0	70	C

Capacitance DC Specifications

Symbol	Parameter	Min.	Max.	Unit	Note
Cin	Input Capacitance	-	10	pF	1
Cout	Output Capacitance	-	10	pF	1
$C_{I/0}$	Bi-directional Capacitance	-	20	pF	1

ICC Specifications

Symbol	Parameter	Typ.	Max.	Unit	Note
ICC_1	Supply Current	40	90	mA	2
ICC_3	Supply Current under SUSPEND	30	90	μA	

Electrostatic Discharge Characteristics

Symbol	Parameter	Value	Test Condition
Vzap	E.S.D. Tolerance	>1500V	Mil-STD 883 Meth. 3015

Notes: 1. @ 1MHz
2. ON Mode; CPU operating @ MHz

3.3V

VG230 3.3V TIMING TABLE

- **CPU_TCYC = (X1 period) ÷ (value set by D[7:5] of Index Reg. [01h]) min. period = 124.2ns (max freq. = MHz)**
- **SYS_TCYC = CPU_TCYC ÷ (value set by D[1:0] of Index Reg. [01h]) min. period = 124.2ns (max. freq. = MHz)**
- **VID_TCYC = (X1 period) ÷ 2 min. period = 62.1ns max freq. = 16.1mhz)**

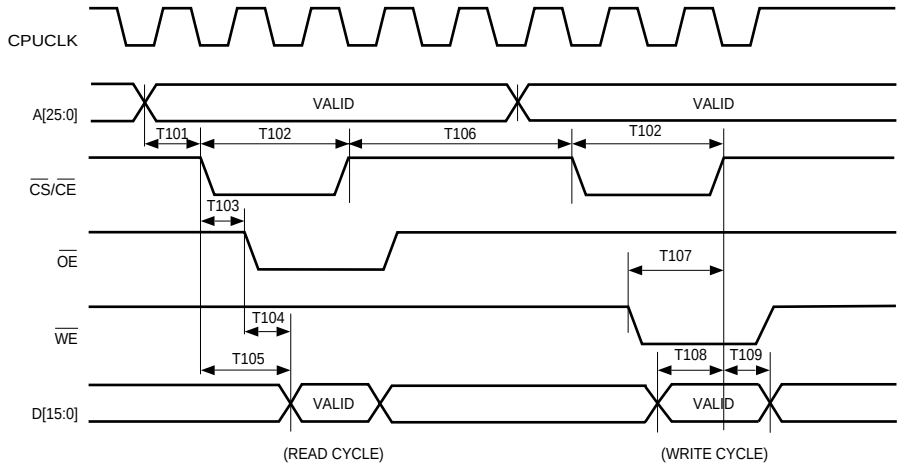
MEMORY CYCLE TIMING

Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	Memory Cycle Timing (Wait State = 0)			
T101	ADDR setup time to *CS/*CE/*RAS↓	-	0.5*CPU_TCYC	-
T102	*OE↓ delay from *CS/*CE/*RAS↓	-	0.5*CPU_TCYC	-
T103	*CS/*CE/*RAS pulse width	2*CPU_TCYC - 20ns	-	-
T104	DATA valid from *OE↓ (read)	-	-	1.5*CPU_TCYC - 40ns
T105	DATA valid from *CS/*CE↓ (read)	-	-	2*CPU_TCYC - 40ns
T106	*CS/*CE/*RAS precharge time	2*CPU_TCYC - 20ns	-	-
T107	*WE↓ setup time to *CS/*CE↑ (write)	1.5*CPU_TCYC	-	-
T108	DATA setup time to *CS/*CE↑ (write)	-	1.5*CPU_TCYC	-
T109	DATA hold time from *CS/*CE↑ (write)	-	0.5*CPU_TCYC	-
T110	ADDR hold time from *RAS↓		0.5*CPU_TCYC	-
T111	ADDR setup time to *CAS↓		0.5*CPU_TCYC	-
T112	*CAS↓ delay from *RAS↓	-	-	1*CPU_TCYC
T113	*CAS pulse width	1*CPU_TCYC - 20ns	-	-
T114	DATA valid from *RAS↓ (read)	-	-	2*CPU_TCYC - 40ns
T115	DATA valid from *CAS↓ (read)	-	-	1*CPU_TCYC - 40ns
T116	DATA setup time to *CAS↓ (write)	-	0.5*CPU_TCYC	-
T117	DATA hold time from *CAS↓ (write)	-	0.5*CPU_TCYC	-
T118	*WE↓ setup time to *CAS↓	-	0.5*CPU_TCYC	-

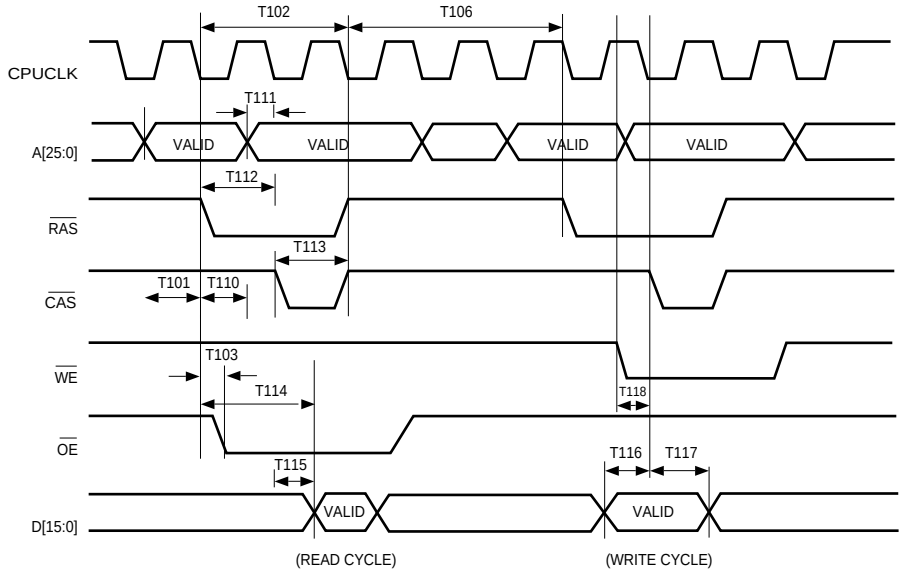
3.3V

MEMORY CYCLE TIMING

SRAM/PSRAM



DRAM Timing

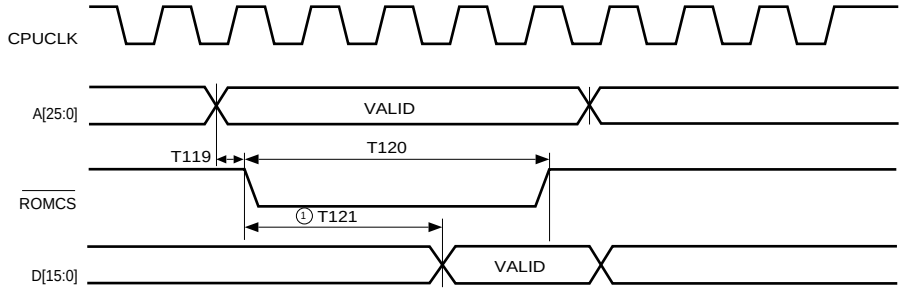


3.3V

MEMORY CYCLE TIMING (continued)

T119	ADDR setup time to *ROMCE[1:0]↓	-	0.5*CPU_TCYC	-
T120	*ROMCE[1:0] pulse width	2*CPU_TCYC - 20ns	-	-
T121	DATA valid from *ROMCE[1:0]↓	-	-	2*CPU_TCYC - 40ns

ROM Timing



① **Note:**

T121: Parameter shown in table, wait state = 0.

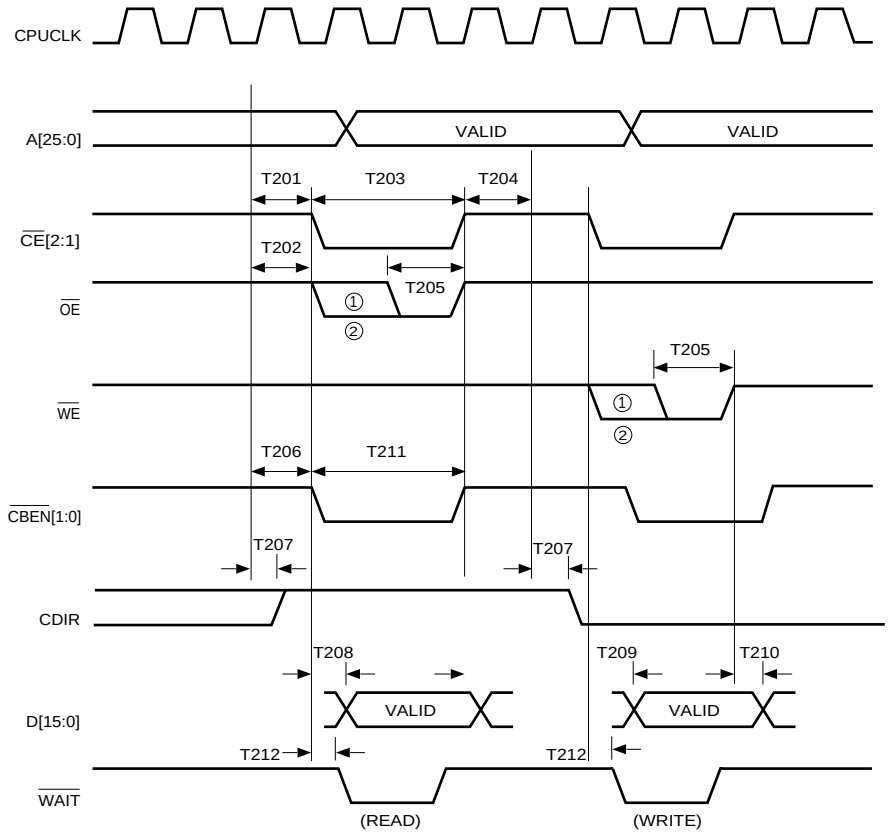
3.3V

PC CARD MEMORY CYCLE TIMING

Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	PCCARD Memory Cycle Timing (Wait State = 0)			
T201	ADDR delay from *CE[2:1]⇓	-	-	0.5*CPU_TCYC
T202	*OE/*WE↓ delay from *CE[2:1]⇓	-	1*CPU_TCYC	-
T203	*CE[2:1] pulse width	2.5*CPU_TCYC - 20ns	-	-
T204	ADDR hold time from *CE[2:1]⇑	-	0.5*CPU_TCYC	-
T205	*OE/*WE pulse width	2*CPU_TCYC - 20ns	-	-
T206	ADDR delay from *CBEN[1:0]⇓	-	-	0.5*CPU_TCYC
T207	CDIR setup time to *CE[2:1]/*CBEN[1:0]⇓	-	1*CPU_TCYC	-
T208	DATA valid from *OE⇓ (read)	-	-	2*CPU_TCYC - 40ns
T209	DATA setup time from *CE[2:1]/*WE⇑ (write)	-	1*CPU_TCYC	-
T210	DATA hold time from *CE[2:1]/*WE⇑ (write)	-	0.5*CPU_TCYC	-
T211	*CBEN[1:0] pulse width	2.5*CPU_TCYC - 20ns	-	-
T212	*WAIT delay from *OE/*WE⇓	-	-	1*CPU_TCYC - 10ns

3.3V

PC Card Memory Timing



Notes:

① OE/WE may be delayed 0, 1, 2, or 3 clocks from the falling edge of CE under software control.

② When enabling OE/WE command delay, an additional number of wait states are added to the PC Card Memory cycle to match the OE/WE delay value.

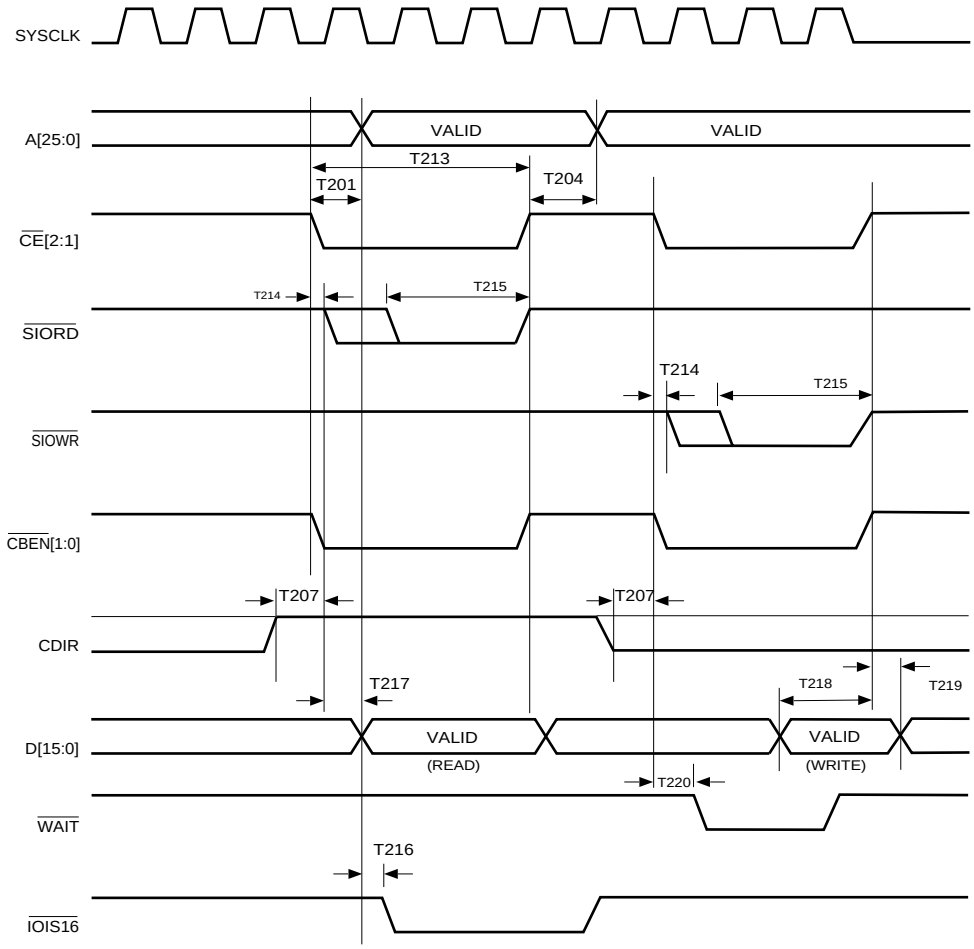
3.3V

PC CARD I/O CYCLE TIMING

Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	PCCARD I/O Cycle Timing (Wait State = 0)			
T213	*CE[2:1] pulse width	3*SYS_TCYC 20ns	-	-
T214	*SIORD/*SIOWR↓ delay from *CE[2:1] ↓	-	0.5*SYS_TCYC	-
T215	*SIORD/*SIOWR pulse width	2*SYS_TCYC 20ns	-	
T216	ADDR setup time to *IOIS16A↓	-	-	1.5*SYS_TCYC-20ns
T217	DATA valid from *SIORD↓ (read)	-	-	2*SYS_TCYC - 40ns
T218	DATA setup time from *SIOWSR/*CE[2:1]↑ (write)	1*SYS_TCYC	-	-
T219	DATA hold time from *SIOWSR/*CE[2:1]↑ (write)	-	0.5*SYS_TCYC	-
T220	*WAIT↓ delay from *CE[2:1]↓	-	-	0.5*SYS_TCYC-20ns

3.3V

PC Card I/O Timing



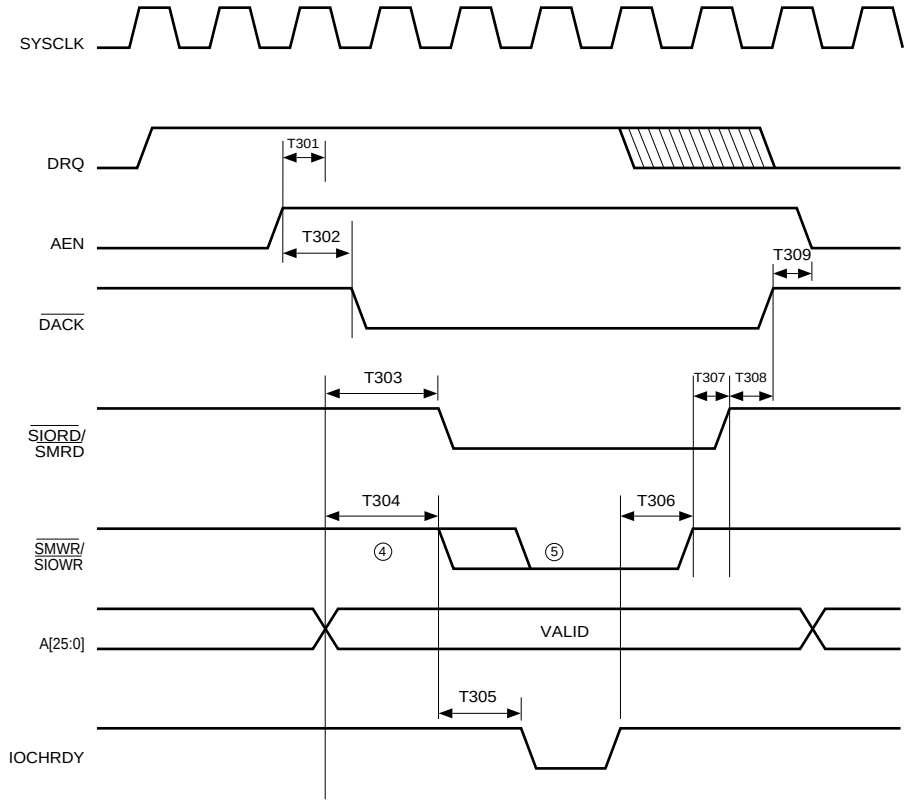
3.3V

DMA CYCLE TIMING

Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	DMA Cycle Timing			
T301	AEN↑ to ADDR valid	-	0.5*SYS_TCYC	-
T302	*DACK↓ delay from AEN↑	-	0.5*CPU_TCYC	-
T303	ADDR setup time to *SMRD/*SIORD↓	-	0.5*SYS_TCYC	-
T304	ADDR setup time to *SMWR/*SIOWR↓	-	1.5*SYS_TCYC	-
T305	IOCHRDY↓ delay from *SMRD/*SIORD↓	-	-	1*SYS_TCYC - 20ns
T306	*SMRD/*SIORD↑ delay from IOCHRDY release	-	1*SYS_TCYC	-
T307	*SMRD/*SIORD↑ delay from *SIOWR/*SMWR↑	-	1*SYS_TCYC	-
T308	*DACK↑ delay from *SMRD /*SIORD↑	-	0.5*SYS_TCYC	-
T309	AEN↓ delay from *DACK↑	-	0.5*CPU_TCYC	-

3.3V

DMA Timing



Notes:

T304: ④ SIOWR/SMWR leading edge may be delayed 0, 1, 2, or 3 clocks after the leading edge of SIORD/SMRD.

⑤ For all DMA cycles, SIOWR/SMWR is active for at least 3 clock cycles.

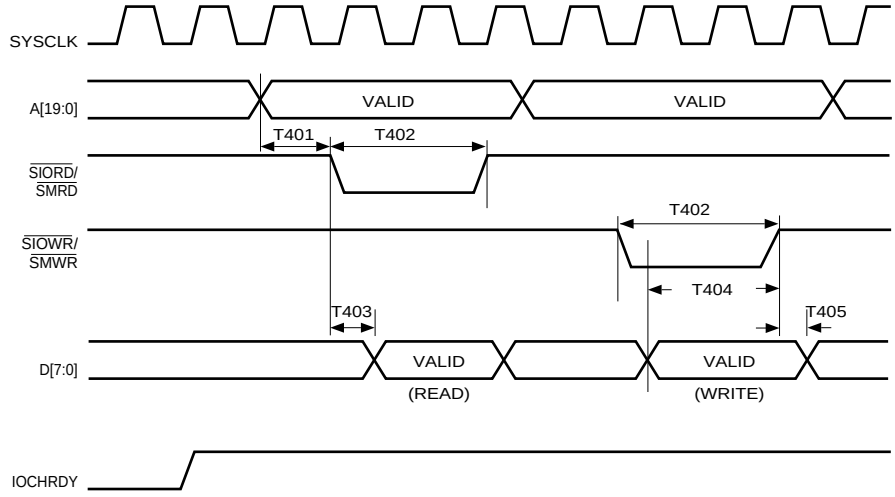
3.3V

EXTERNAL BUS TIMING

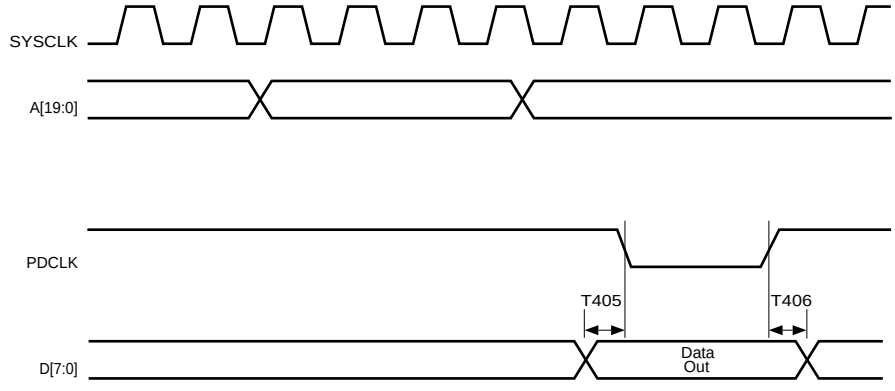
Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	External Bus Timing			
T401	*SMRD/*SMWR/*SIORD/*SIOWR pulse width	2*SYS_TCYC - 20ns	-	-
T403	DATA valid from *SMRD/*SIORD↓ (read)	-	-	2*SYS_TCYC - 40ns
T405	DATA setup time from *SMWR/*SIOWR↑ (write)	-	0.5*SYS_TCYC	-
T406	DATA hold time from *SMWR/*SIOWR↑ (write)	-	0.5*SYS_TCYC	-

3.3V

XT Bus Timing



PIO Timing

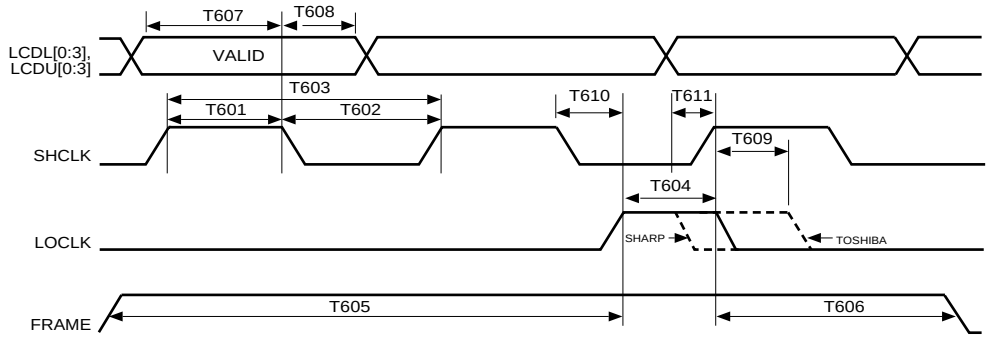


3.3V

LCD TIMING

Items	*Descriptions*	*3.3V Datasheet*		
		min.	*typ.*	*max.*
	LCD Timing			
T601	SHCLK high time	3*VID_TCYC - 20ns	-	-
T602	SHCLK low time	3.5*VID_ TCYC - 20ns	-	-
T603	SHCLK cycle time	6.5*VID_ TCYC - 20ns	-	-
T604	LOCLK width, generic timing	3*VID_ TCYC - 20ns	-	-
	LOCLK width, SHARP timing	2.5*VID_ TCYC - 20ns	-	-
	LOCLK width, TOSHIBA timing	5*VID_ TCYC - 20ns	-	-
T605	FRAME setup time to LOCLK↑	800 ns	-	-
T606	FRAME↓ delay from LOCLK↓	800 ns	-	-
T607	Pixel Data setup time to SHCLK↓	4.5*VID_ TCYC - 20ns	-	-
T608	Pixel Data hold time to SHCLK↓	2*VID_ TCYC - 20ns	-	-
T609	LOCLK↓ (TOSHIBA) delay from SHCLK↑	2*VID_ TCYC - 20ns	-	-
T610	LOCLK↑ delay from SHCLK↓	0.5*VID_TCYC - 20ns	-	-
T611	LOCLK↓ (SHARP) setup time to SHCLK↑	0.5*VID_TCYC - 20ns	-	-

LCD Timing



ADDENDUM

NOTES

V3.1 is Backwards compatible with V2.3. This is achieved by the addition of three (3) Enhancement Registers at addresses E0h, E1h and E2h. After every power on or hardware reset until specific bits are set within these registers, the VG230 will be in revision V2.3 mode. Enhancements may be independently enabled by use of the extended register set.

This document is in 2 sections. The 1st section describes fixes in V3.1 to the known V2.3 anomalies. Section 2 describes enhancements to V2.3.

The VG230 revision level is shown on the package body as:

Revision Code	VG230 Revision
A100	V2.2
A101	V2.3
A211	V3.1

V3.1 of the VG230 fixes known anomalies as detailed on the following pages. These anomalies are broken into two groups, depending on whether they have Enhanced Register Bit requirements, and for completeness we have included a third group.

CONTENTS

SECTION 1

Anomaly Group 1:

The following two anomalies identified in V2.3 have been fixed in V3.1. They have no repercussions on V2.3 designs and so have no Enhancement Register bits. They are always enabled.

- **Internal UART 2400 Baud 8 bit STOP detect. (Anomaly #3 in V2.3, fixed in V3.1)**
  At 2400 Baud, 8 Bits, if a modem generated a short STOP bit between two characters, the VG230 did not detect the STOP bit and so did not resync on the start bit of the second character correctly. Setting other Baud rates or 7 Bits were a work around for this problem. No other work around was available so this fix does not have an Enhancement Register Bit.

- **Internal UART 9600 Baud loopback testing. (Anomaly #7 in V2.3, fixed in V3.1)**
  The UART failed the loopback test at 9600. There was no work around available so this fix does not have an Enhancement Register Bit.

Anomaly Group 2:

These anomalies in V2.3 have been fixed in V3.1. To maintain Backwards compatability the use of Enhancement Registers E0h-E2h allow the enabling/disabling of these upgrades and enhancements.

- **DRAM (256K x 16) correct SUSPEND mode added. (Anomaly #2 in V2.3, fixed in V3.1)**
  The 256Kx16 DRAM SUSPEND was not fully supported. ALL other DRAM configurations are supported correctly. This has been corrected in V3.1. When D0 of the Enhanced 1 Register is set to '1' the VG230 will correctly support the 256K x 16 DRAM SUSPEND mode.

- **Software RESET of the arbitration logic (Anomaly #4 in V2.3, fixed in V3.1).**
  Previous versions of the VG230 prevent the system RESUME'ing from OFF mode reliably when OFF mode is entered due to an unexpected deassertion of the SYSPWRGD input. The RESUME failure is caused when SYSPWRGD goes low while the DMA controller or LCD controller has control of the local CPU bus. In this case, the OFF mode forces a CPU RESET but does not RESET the arbitration logic. This causes the arbitration logic and the CPU to lose synchronization when the system is RESUME'd.

To correct this problem, the VG230 V3.1 silicon supports a software RESET of the arbitration logic. This allows software to force the arbitration logic back into synchronization with the CPU and successfully complete a RESUME from OFF mode. Software may reset the arbitration logic by first setting bit D4 of the VG230 Enhance 3 register to '1' and then resetting this bit back to '0'.

Due to the nature of the failure, the internal V30HL only has control of the bus while the DMA controller is requesting service (HRQ asserted). Therefore when resetting the arbitration logic the following sequence should be observed:

Following a hard reset, the BIOS checks if a RESUME from OFF has occurred. If RESUME'ing from OFF, the BIOS next checks if refresh is running by polling the refresh address counter in the 8237 macro. If refresh is not running, the BIOS sets bit D4 of the VG230 Enhance 3 register to '1' to force the arbitration logic into RESET. Next the BIOS must disable pending DMA cycles by masking all DMA channels. After this has been done, the BIOS may reset bit D4 of the VG230 Enhance 3 register to '0' to bring the arbitration logic out of RESET. Finally, DMA may be re-enabled.

- **PCMCIA Card detect slot 1 updated for when power is off. (Anomaly #5in V2.3, fixed in V3.1)**

  When the power to the PCMCIA slots was off the Card Presence for slot 1 was not reported until the power to the slot had been sequenced. This has been fixed in V3.1 as described in more detail below. When D1 of the Enhanced 1 Register is set to '1' the VG230 will report the real time status of the PC Card insertion.

- **Multiple banks of PSRAM now supported correctly. (Anomaly #6 in V2.3, fixed in V3.1)**

  For designs that used multiple banks of PSRAM there was a potential for data corruption in all but the highest numbered PSRAM bank. Most designs use only one bank of PSRAM but there is a BIOS work around for this with V2.3. When D5 of the Enhanced 1 Register is set to '1' the V3.1 VG230 will correct this problem.

- **8 Bit PSRAM SUSPEND refresh for odd numbered banks supported. (Anomaly #8 in V2.3, fixed in V3.1)**

  When using 8 Bit PSRAMs the odd numbered banks were not refreshed correctly during SUSPEND. Most designs use 16 Bit PSRAMs but an external work around was available for V2.3. When D3 of the Enhanced 1 Register is set to '1' the V3.1 VG230 will correct this problem.

Anomaly Group 3:

The following two anomalies identified in V2.3 and associated with V3.1 are considered to have no impact to system designers.

- **Anomaly #1 in V2.3 - ROM OE control.**
  The VG230 is designed to provide OE for both the BIOS ROM and the option ROM via MC[9:6] depending on the RAM type selected. In some configurations of ROM and RAM, ROM OE does not function correctly.

  This is considered to be of little or no impact to system designers. The 2 modes supported correctly are the most commonly used. Alternatively it is possible to use external logic to force the ROMOE low until the RAM type and density have been initialized by Software.

- **Anomaly #9 in V2.3 - Parallel Port Power Consumption.**
  Applications that enable the Parallel Port Interrupt noted a slight increase in current due to an internal pulldown resister. This is minimized by the BIOS during SUSPEND by disabling the parallel port interrupt prior to S USPEND and restoring the state upon Resuming.

SECTION 2

System Enhancements:

These upgrades/enhancements have been added to V3.1. To maintain Backwards compatibility the use of Enhancement Registers E0h-E2h allow the enabling/disabling of these upgrades and enhancements.

Note that any changes to current VG230 register definitions are represented by *Italic* text.

- **SUSPEND current improvement for all clock speeds. (Anomaly in V2.3, fixed in V3.1)**

  When the VG230 internal CPU was operating at some frequency less than 16Mhz and 3.3v, there was a potential for the SUSPEND current to be high (2 to 10mA). V2.3 fixed this for frequencies down to 8Mhz. V3.1 fixes this for all clock frequencies. When D6 of the Enhanced 1 Register is set to '1' the VG230 will correctly SUSPEND for all CPUCLK frequencies.

- **PCMCIA attribute and common memory control Enhanced.**

  V2.3 of the VG230 supported PC Card attribute/common memory selection on a socket basis through the *REG bits of the PC Card Slot 0 and PC Card Slot 1 Control Registers. V3.1 of the VG230 has been modified to allow PC Card attribute/common memory selection on a window basis.

  To enable this functionality, bit D2 of the VG230 Enhance 1 register must be set to '1'. Once this functionality has been enabled, selection of the PC Card attribute/common memory space is accomplished through the memory mapping registers as follows:

Name Map High Byte Data Register
Type Read/Write
Address 06FH

D7	D6	D5	D4	D3	D2	D1	D0
PEN	DTYP2	DTYP1	DTYP0	MAP25	MAP24	MAP23	MAP22

Bit	Default	Function
D7	0	0 - Disable mapping for this page 1 - Enable mapping for this page
D[6:4]	000	DTYP2 DTYP1 DTYP0 Page Memory Device Type 0 0 0 None (external bus cycle) 0 0 1 RAM (as specified by MTYP[3:0] bits) 0 1 0 ROM #0 0 1 1 ROM #1 1 0 0 PC Card A (Common Memory) 1 0 1 PC Card B (Common Memory) *1 1 0 PC Card A (Attribute Memory)* *1 1 1 PC Card B (Attribute Memory)*
D[3:0]	0H	most significant nibble of memory map address

When window addressable attribute/common memory space is enabled, the *REG bits of the PC Card Slot 0 and PC Card Slot 1 Control Registers will be redefined as spare R/W bits.

- **PCMCIA 8 bit memory card Enhancement.**
  V2.3 of the VG230 supported only 16 bit PCMCIA memory cards. V3.1 of the VG230 has been modified to support either 8 bit or 16 bit PCMCIA memory cards on a socket basis.

  To enable this functionality, bit D4 of the VG230 Enhance 1 register must be set to '1'. Once enabled, the socket may be set to 8 bit or 16 bit operation through the PC Card Controller Mode Register as follows:

Name PC Card Controller Mode Register
Type Read/Write
Index 20H

D7	D6	D5	D4	D3	D2	D1	D0
*SLOT0EN	*SLOT1EN	IRSTS1	IRSTS0	S0PGMEN	*SLOT0_MEM8*	S1PGMEN	*SLOT1_MEM8*

Bit	Default	Function		
D7	0	0 - Enable PC Card Slot 0		
D6	1	0 - Enable PC Card Slot 1 Note: In order to enable PC Card Slot 1, the Keyboard Scan function must be disabled.		
D[5:4]	11	IRSTS1	IRSTS0	Controller Status Interrupt Selects
		0	0	NMI
		0	1	IRQ2
		1	0	IRQ6
		1	1	IRQ7
D3	0	1 - Enable Slot 0 Programming Voltage (VPPENA)		
D2	*0*	*0 - Slot 0 supports 16 bit PCMCIA Cards. Common & Attribute memory cycles will use both bytes of the data bus, D[15:8] and D[7:0].* *1 -Slot 0 supports 8 bit PCMCIA Cards. Common & Attribute memory cycles will use only the low byte of the data bus, D[7:0].*		
D1	0	1 - Enable Slot 1 Programming Voltage (VPPENB)		
D0	*0*	*0 - Slot 1 supports 16 bit PCMCIA Cards. Common & Attribute memory cycles will use both bytes of the data bus, D[15:8] and D[7:0].* *1 -Slot 1 supports 8 bit PCMCIA Cards. Common & Attribute memory cycles will use only the low byte of the data bus, D[7:0].*		

The *SLOT0_MEM8* and *SLOT1_MEM8* bits described above only define the memory data bus width of an installed PCMCIA card. The I/O data bus width is programmed through the IO8BIT bits of the PC Card Slot 0 PC Card Slot 1 Control Registers. When the 8 bit PCMCIA memory card enhancement is disabled, the *SLOT0_MEM8* and *SLOT0_MEM8* bits described above are defined as Reserved.

The table below indicates the operation of the VG230 revision V3.1 while accessing slots configured for 8 bit and 16 bit PCMCIA memory cards.

Slot Definition	Access Type	A0	*CE2	*CE1	*CBEN1	*CBEN0
8 Bit	Even Byte	0	1	0	1	0
	Odd Byte	1	1	0	1	0
	Word (note 1)	0	1	0	1	0
		1	1	0	1	0
16 Bit	Even Byte	0	1	0	1	0
	Odd Byte	1	0	1	0	1
	Word	0	0	0	0	0

Note 1: 16 bit access to sockets defined as 8 bits will be split into consecutive 8 bit even and 8 bit odd accesses by the VG230.

- **PCMCIA card change enhancements for real time card detect signals.**
  Four changes have been implemented to enhance the Card Change logic of the V3.1 VG230. These enhancements are enabled by bits D3 and D1 of the VG230 Enhance 1 Register.

  1. Real time status reporting of the card detect signals.

  Earlier revisions of the VG230 delay assertion of the *PRESENT bits of the PC Card Slot 0 and PC Card Slot 1 Status Registers following a card insertion event until the PC Card interface has been power sequenced. V3.1 of the VG230 has been modified to reflect the real time status of the card detect pins for their respective sockets.

  This feature is enabled by setting bit D1 of the VG230 Enhance 1 Register to '1'. Once enabled, the *PRESENT bits of each slot status register will be reset to '0' immediately after a PC Card insertion.

  *Note: This enhancement will not disable power sequencing of the PC Card interface. Socket Services will be required to monitor the RDY/*BSY bit of the PC Card Slotx Status Register to determine when power sequencing has been completed and the PC Card may be accessed. Refer to the next section for details.*

  2. Power sequence status reporting.

  In order to support real time card presence status reporting, the V3.1 VG230 silicon redirects power sequencing status onto the RDY/*BSY bits of the PC Card Slot 0 and PC Card Slot 1 Status Registers. When real time card presence status reporting is enabled, Socket Services

must monitor the RDY/*BSY status bit following a PC Card insertion event or the cycling of power to the PC Card slot. The RDY/*BSY bit will be driven to '0', indicating that the PC Card is busy, until the power sequencing has been completed and the PC Card interface signals are activated. Socket Services must not attempt to access the PC Card until the RDY/*BSY bit is set to '1'.

Previous revisions of the VG230 report the actual status of the PC Card RDY/*BSY pin on the RDY/*BSY register bit. The *PRESENT bit for each socket is delayed until the PC Card power sequencing has completed.

3. Card insertion events.

To provide support for insertion interrupts, V3.1 of the VG230 allows S/W to generate a Card Changed status interrupt. This is functionally enabled by setting bit D3 of the VG230 Enhance 1 Register to '1'. Once enabled, S/W Card Changed status interrupts may be generated by writing to the PC Card Slot 0 or PC Card Slot 1 Interrupt Mask Registers.

Name PC Card Slot 0 Interrupt Mask Register
Type Read/Write
Index 23H

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	*SWCHGINT*	CHGMSK	Reserved	Reserved	PULSED

Bit	Default	Function
D7	1	0 - Enable Slot 0 PC I/O Card Interrupts
D6	0	0 - Enable Slot 0 Low Battery Warning Interrupts (Memory Mode) or disable PC Card Audio output (I/O Mode). When this bit is reset low in I/O mode, the PC Card Audio signal is disabled and the will read back high in the PC Card Slot 0 Status register.
D5	0	0 - Enable Slot 0 Battery Fail Alarm Interrupts (Memory Mode) or Status Changed Interrupts (I/O Mode)
D4	*0*	*Writing this bit to '1' will trigger a Card Changed interrupt for Slot 0. Writing this bit to '0' has no effect.*
D3	0	0 - Enable Slot 0 Card Changed Interrupts
D[2:1]	00	Reserved bits
D0	00	0 - Controller Supports Level Mode Interrupts from PC I/O Cards 1 - Controller Supports Pulsed Mode Interrupts from PC I/O Cards

Name PC Card Slot 1 Interrupt Mask Register
Type Read/Write
Index 29H

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	*SWCHGINT*	CHGMSK	Reserved	Reserved	PULSED

Bit	Default	Function
D7	1	0 - Enable Slot 1 PC I/O Card Interrupts
D6	0	0 - Enable Slot 1 Low Battery Warning Interrupts (Memory Mode) or disable PC Card Audio output (I/O Mode). When this bit is reset low in I/O mode, the PC Card Audio signal is disabled and the will read back high in the PC Card Slot 1 Status register.
D5	0	0 - Enable Slot 1 Battery Fail Alarm Interrupts (Memory Mode) or Status Changed Interrupts (I/O Mode)
D4	*0*	*Writing this bit to '1' will trigger a Card Changed interrupt for Slot 1. Writing this bit to '0' has no effect.*
D3	0	0 - Enable Slot 1 Card Changed Interrupts
D[2:1]	00	Reserved bits
D0	00	0 - Controller Supports Level Mode Interrupts from PC I/O Cards 1 - Controller Supports Pulsed Mode Interrupts from PC I/O Cards

To use the S/W Card Changed feature, Socket Services must be modified to differentiate between card insertion and card removal events through the state of the *PRESENT bit of the PC Card Slotx Status Registers. When a Card Changed interrupt is received and the *PRESENT bit is '1', a card removal event occurred. If the *PRESENT bit is '0', a card insertion event occurred.

4. Card change status.

V3.1 of the VG230 allows software to clear card changed status at any time. This capability is enabled by setting bit D3 of the VG230 Enhance 1 Register to '1'. Previous revisions of the VG230 required a PC Card to be installed before a card removal interrupt could be cleared.

Note: Care must be exercised by the software when clearing card changed status. The card detect inputs are not debounced by the VG230. It is possible during card insertions or card removals, that multiple card changed interrupts may be generated. When the enhanced card change capability is enabled, S/W is responsible for debouncing the card changed status latch.

*Card insertion is generated by software, so it is possible for software to debounce by polling until RDY/*BSY indicates that the PC Card I/F has been power sequenced. Card removal can be debounced by disabling card removal interrupts until after a card is inserted. Debouncing in this manner will not require an in-line delay in the interrupt routine.*

- **PCMCIA status change interrupt global on/off enhancement.**
  V3.1 of the VG230 provides global I/O window enable/disable and status changed interrupt mask bits. This capability is enabled by setting bit D0 of the VG230 Enhance 2 Register to '1'. Once enabled, the global interrupt control will be provided by the PC Card Slot 0 and PC Card Slot 1 Interrupt Mask Registers as shown below:

Name PC Card Slot 0 Interrupt Mask Register
Type Read/Write
Index 23H

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	Reserved	CHGMSK	Reserved	*SIRQMSK*	PULSED

Bit	Default	Function
D7	1	0 - Enable Slot 0 PC I/O Card Interrupts
D6	0	0 - Enable Slot 0 Low Battery Warning Interrupts (Memory Mode) or disable PC Card Audio output (I/O Mode). When this bit is reset low in I/O mode, the PC Card Audio signal is disabled and the will read back high in the PC Card Slot 0 Status register.
D5	0	0 - Enable Slot 0 Battery Fail Alarm Interrupts (Memory Mode) or Status Changed Interrupts (I/O Mode)
D4	0	Reserved bit
D3	0	0 - Enable Slot 0 Card Changed Interrupts
D2	0	Reserved bit
D1	*0*	*0 - Enable all Slot 0 status interrupt sources.* *1 - Disable all Slot 0 status interrupt sources.*
D0	00	0 - Controller Supports Level Mode Interrupts from PC I/O Cards 1 - Controller Supports Pulsed Mode Interrupts from PC I/O Cards

Name PC Card Slot 1 Interrupt Mask Register
Type Read/Write
Index 29H

D7	D6	D5	D4	D3	D2	D1	D0
IREQMSK	LBMSK	LLBMSK	Reserved	CHGMSK	Reserved	*SIRQMSK*	PULSED

Bit	Default	Function
D7	1	0 - Enable Slot 1 PC I/O Card Interrupts
D6	0	0 - Enable Slot 1 Low Battery Warning Interrupts (Memory Mode) or disable PC Card Audio output (I/O Mode). When this bit is reset low in I/O mode, the PC Card Audio signal is disabled and the will read back high in the PC Card Slot 1 Status register.
D5	0	0 - Enable Slot 1 Battery Fail Alarm Interrupts (Memory Mode) or Status Changed Interrupts (I/O Mode)
D4	0	Reserved bit
D3	0	0 - Enable Slot 1 Card Changed Interrupts
D2	0	Reserved bit
D1	*0*	*0 - Enable all Slot 1 status interrupt sources.* *1 - Disable all Slot 1 status interrupt sources.*
D0	0	0 - Controller Supports Level Mode Interrupts from PC I/O Cards 1 - Controller Supports Pulsed Mode Interrupts from PC I/O Cards

Note that when interrupt sources for a particular slot are globally masked, pending or new interrupts will not be lost. Any pending or new interrupts will be asserted if the global mask bit is reset to ’0’ and the interrupting sources specific mask bit is unmasked.

The global I/O window enable is provided by the PC Card Slot 0 and PC Card Slot 1 Address Range Registers as shown below:

Name PC Card Slot 0 I/O Address Range Register
Type Read/Write
Index 26H

D7	D6	D5	D4	D3	D2	D1	D0
MSK7	MSK6	MSK5	MSK4	MSK3	Reserved	*IOEN*	*INPMSK

Bit	Default	Function
D[7:3]	00	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked form the address comparison as follows: A[7:3]MSK — I/O Range 0 0 0 0 0 — 8 bytes 0 0 0 0 1 — 16 bytes 0 0 0 1 1 — 32 bytes 0 0 1 1 1 — 64 bytes 0 1 1 1 1 — 128 bytes 1 1 1 1 1 — 256 bytes
D2	0	Reserved bit
D1	*0*	*0 - Disable Slot 0 I/O window.* *1 - Enable Slot 0 I/O window.*
D0	0	Card A input acknowledge mask bit. 0 - Ignore PC I/O Card *INPACK signal. PC Card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC Card data buffers enabled only when chip select is asserted and *INPACK is returned from the PC I/O Card..

Name PC Card Slot 1 I/O Address Range Register
Type Read/Write
Index 2CH

D7	D6	D5	D4	D3	D2	D1	D0
MSK7	MSK6	MSK5	MSK4	MSK3	Reserved	*IOEN*	*INPMSK

Bit	Default	Function
D[7:3]	00	Mask bits for lower address bits. Each bit allows its corresponding address bit to be masked form the address comparison as follows: A[7:3]MSK — I/O Range 0 0 0 0 0 — 8 bytes 0 0 0 0 1 — 16 bytes 0 0 0 1 1 — 32 bytes 0 0 1 1 1 — 64 bytes 0 1 1 1 1 — 128 bytes 1 1 1 1 1 — 256 bytes
D2	0	Reserved bit
D1	*0*	*0 - Disable Slot 1 I/O window.* *1 - Enable Slot 1 I/O window.*
D0	0	Card B input acknowledge mask bit. 0 - Ignore PC I/O Card *INPACK signal. PC Card data buffers enabled whenever chip select is asserted. 1 - Enable PC I/O Card *INPACK signal. PC Card data buffers enabled only when chip select is asserted and *INPACK is returned from the PC I/O Card.

- **PCMCIA IOIS16 sampling enhanced for slower ATA cards.**
  Earlier revisions of the VG230 required that PC I/O cards drive the IOIS16 signal valid within 70 nS of address valid. The PCMCIA specification defines the maximum delay for PC I/O cards from address valid to IOIS16 as 35 nS. However, some PCMCIA ATA drives qualify IOIS16 with chip select therefore delaying IOIS16 beyond the minimum 70 nS requirement of the VG230.

  V3.1 of the VG230 relaxes the IOIS16 valid requirement considerably. This capability is enabled by setting bit D1 of the VG230 Enhance 2 Register to '1'. Once enabled, IOIS16 from PC I/O cards will be sampled and must be valid 55 nS after chip select to the PC Card goes active.

- **ROM Chip Select control by power management enhancement.**
  The VG230 provides the ability to stop the processor clock upon entry to the DOZE or SLEEP power management modes. This operation is referred to as Static DOZE. In some instances, such as when an APM driver is executing out of ROM, Static DOZE operation may not be possible due to the mechanism which halts the processor clock. This mechanism may cause the processor clock to stop while the ROM chip enable (*ROMCE0 or *ROMCE1) is asserted. This has the potential of resulting in increased total system power consumption.

  V3.1 of the VG230 provides the capability of assuring that the ROM chip enable signals are not asserted when the Static DOZE mode is entered. This capability is enabled by setting bit D2 of the VG230 Enhance 2 Register to ’1’.

- **Output BAUDOUT signal from internal UART on GPIO3 pin (HP SIR requirement).**
  The VG230 V3.1 silicon supports a mode where the internal 16450 BAUDOUT signal may be output on the GPIO3 pin. This feature is enabled by setting bit D5, SIR_EN, of the VG230 Enhance 3 register to ’1’. When enabled, BAUDOUT is output on the GPIO3 pin regardless of the setting of the GPIO Mode register. It should be noted that the GPIO3 pin will be driven tri-state during SUSPEND and OFF modes even when configured to output BAUDOUT.

- **Software power sequencing of the LCD interface (Fast SUSPEND support).**
  Option 1 -
  The VG230 V3.1 silicon supports software power sequencing of the LCD panel. This capability is provided to enable the BIOS to execute a Fast SUSPEND. Software power sequencing is enabled by setting bit D3 of the VG230 Enhancement 3 register to ’1’. Once software power sequencing enabled, the LCD logic power, LCD interface signals, and LCD bias power are enabled or disabled by bits D2 - D0 respectively of the VG230 Enhancement 3 register.

  Option 2 -
  This option permits software to immediately power down the LCD panel when SUSPENDing. On RESUMEing, the power up is controlled by the hardware power sequencing logic of the LCD controller. This mode is enabled by setting Bit D6 to ‘1’ and Bits D3 to ‘0’ of the VG230 Enhancement 3 register. The fast power down of the LCD panel is then accomplished by setting the DLY[2:0] BITS OF THE LCD Mode Register to ‘111’. The system will power off the LCD and then SUSPEND. When RESUMEing, the DLY[2:0] bits are written with the desired power up sequencing delay value and the LCD controller powers up the LCD panel.

5. Enabling VG230 Enhanced Features.

The enhanced features of the revision V3.1 VG230 will be disabled following a hard reset. This means that the revision V3.1 VG230 will power-up into a VG230 revision V2.3 compatible mode. Each feature or set of features are selectively enabled via a register bit in one of the Enhancement Registers.

Name VG230 Enhancement 1 Register
Type Read/Write
Index E0H

D7	D6	D5	D4	D3	D2	D1	D0
ENHENA	ONPMU	ONDSPRQ	ON8BIT	ONCCHG	ONATTR	ONCDPRS	ONBY16

Bit	Default	Function
D7	0	0 - Globally disable all VG230 enhanced features. 1 - Enable selected VG230 features as specified by bits D[6:0] of this register and bits D[7:0] of the Enhance 2 Register.
D6	0	0 - Normal SUSPEND. 1 - Delay start of SUSPEND.
D5	0	0 - Normal LCD cycles. 1 - Delay end of LCD cycle.
D4	0	0 - Disable 8 bit PCMCIA card support. 1 - Enable 8 bit PCMCIA card support.
D3	0	0 - Disable PC Card change enhancements. 1 - Enable PC Card change enhancements.
D2	0	0 - Disable PC Card Common/Attribute memory enhancement. 1 - Enable PC Card Common/Attribute memory enhancement.
D1	0	0 - Disable PC Card PRESENT status enhancement. 1 - Enable PC Card PRESENT status enhancement.
D0	0	0 - Disable 256Kx16 DRAM SUSPEND fix. 1 - Enable 256Kx16 DRAM SUSPEND fix.

Name VG230 Enhancement 2 Register
Type Read/Write
Index E1H

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ONDINH	ON8PSR	ONRMCE	ONATA	ONGMSK

Bit	Default	Function
D[7:5]	0	Reserved bits. These bits must always be written to zero.
D4	0	0 - Disable D[15:0] input gating during Static DOZE. 1 - Enable D[15:0] input gating during Static DOZE.
D3	0	0 - Disable 8 bit PSRAM OE SUSPEND fix. 1 - Enable 8 bit PSRAM OE SUSPEND fix.
D2	0	0 - Disable ROMCE output control during Static DOZE mode. 1 - Enable ROMCE output control during Static DOZE mode.
D1	0	0 - Disable PC Card ATA interface enhancement. 1 - Enable PC Card ATA interface enhancement.
D0	0	0 - Disable Global PC Card Controller status interrupt mask bit and I/O window enable/disable bit. 1 - Enable Global PC Card Controller status interrupt mask bit and I/O window enable/disable bit.

Bit D7 of the VG230 Enhancement 1 Register is the global enable bit for all revision V3.1 errata and enhancements. Bit D7 must be set to '1' before any of the other Enhancement 1, Enhancement 2 or Enhancement 3 Register bits will enable their respective fixes and/or enhancements.

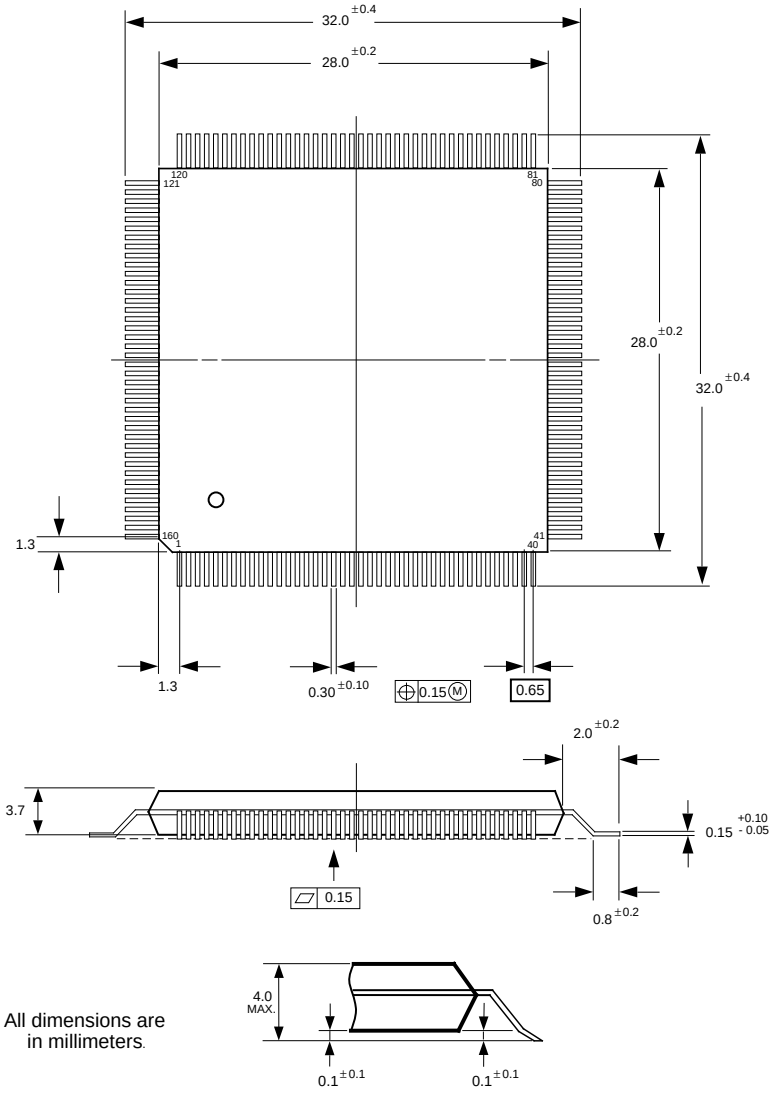
Name VG230 Enhancement 3 Register
Type Read/Write
Index E2H

D7	D6	D5	D4	D3	D2	D1	D0
ENH30ENA	FASTSUSP	SIR_EN	RST_ARB	SW_SEQEN	SW_VPLCD	SW_ VPSIG	SW_ VPBIAS

Bit	Default	Function
D7	0	0 - Globally disable all VG230 version 3.1 enhanced features. 1 - Enable selected VG230 version 3.1 features as specified by bits D[6:0] of this register.
D6	0	0 - Disable Fast LCD Power Down option of LCD Mode register. 1 - Enable Fast LCD Power Down option of LCD Mode register.
D5	0	0 - GPIO pin mappings enabled for default operation. 1 - BAUDOUT signal from internal 16450 output on GPIO3 pin.
D4	0	0 - Do not RESET arbitration logic. 1 - RESET arbitration logic..
D3	0	0 - Disable software power sequencing of the LCD. 1 - Enable software power sequencing of the LCD. When this bit is set to '1', VPLCD signal is enabled and controlled by setting SW_VPLCD Register bit, LCD interface signals are enabled and controlled by setting SW_VPSIG register bit, VPBIAS signal is enabled and controlled by setting SW_VPBIAS register bit.
D2	0	0 - LCD logic power OFF (VPLCD driven Hi-Z). 1 - LCD logic power ON.
D1	0	0 - LCD interface is disabled (driven low). 1 - LCD interface is enabled.
D0	0	0 - LCD bias power OFF (VPBIAS driven Hi-Z). 1 - LCD bias power ON.

VG230 OUTLINE DIAGRAM (QFP)

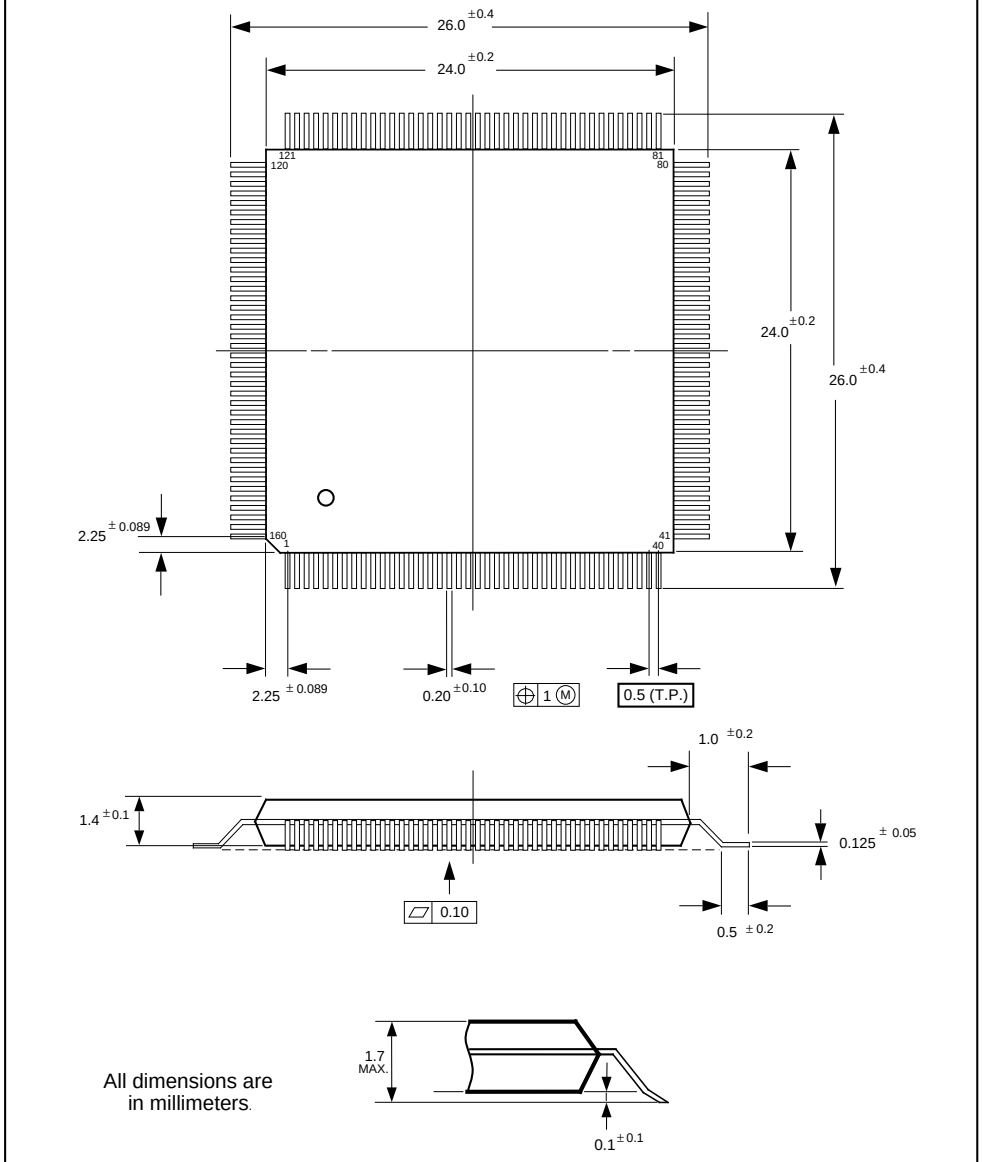
VG-230 160 PIN QFP



All dimensions are in millimeters.

VG230 OUTLINE DIAGRAM (TQFP)

VG-230S 160 PIN TQFP



NOTES

NOTES

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V A D E M

VADEM VG230

SINGLE-CHIP PLATFORM

DATA MANUAL

February 1996

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VG230
SINGLE-CHIP PLATFORM
Data Manual
DATA MANUAL REV. 1.1

V A D E M

1960 Zanker Road San Jose, CA 95112 Tel: 408.467.2100 Fax: 408.467.2199

V3.1 is Backwards compatible with V2.3. This is achieved by the addition of three (3) Enhancement Registers at addresses E0h, E1h and E2h. After every power on or hardware reset until specific bits are set within these registers, the VG230 will be in revision V2.3 mode. Enhancements may be independently enabled by use of the extended register set.

The VG230 revision level is shown on the package body as:

Revision Code	VG230 Revision
A100	V2.2
A101	V2.3
A211	V3.1

V3.1 of the VG230 fixes known anomalies as detailed on the following pages. These anomalies are broken into two groups, depending on whether they have Enhanced Register Bit requirements, and for completeness we have included a third group.

Note: Changes specific to V3.1 are shown in the Addendum.

VG230 REVISION UPDATE

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
16	Connection and Pin Descriptions	Test Mode. ~~(See VG230 Technical Reference Manual)~~
21	Functional Description	The V30HL is designed to operated over a range including +3V (reduces maximum clock rate to 8 MHz) and +5V.
22	Functional Description	*For Register description, see Index 02H ~~Pg. 77 in this manual~~.*
23	Functional Description	Selection of the desired DMA channel is made through bits DRQS[1.0] ~~in the DMA channel is made through bits DRQS[1.0]~~ in the DMA mode register located at index OEH.
24	Functional Description	~~For Register Descriptions, see Pg. 113~~.
25	Functional Description	Levels (IRQ)
25	Functional Description	The Internal Interrupt Configuration Figure illustrates the sources of the internal and external interrupts ~~sources~~.
27	Functional Description	~~The DTYP[2:0] bits specify which type of memory is selected. RAM, ROMCS0, ROMCS1, PCMCIA A, PCMCIA B or external memory are the available selections.~~
27	Functional Description	~~Also included in this register is a mapping enable bit called PEN. When this bit is cleared, mapping for the selected mapping register is disabled.~~
27	Functional Description	For Register Descriptions, see ~~Pg. 82~~ Index 08H.
27	Functional Description	For Register Descriptions, see Index C0H ~~Pg. 140.~~
29	Functional Description	*Change table.*

VG230 REVISION UPDATE
Document: M151013-06 / M151013-07
Old Revision: 1.0 / New Revision: 1.1

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
29	Functional Description	~~*For Register Descriptions, see Pg. 79*~~.
31	Functional Description	*Change table. Add table.*
32	Functional Description	Power also can be removed from the Cards when the Power Management Unit (see pg. 36 ~~Table 2-2~~) incicates SLEEP mode.
32	Functional Description	*For Register Description, see Pg. 9*9~~8~~*.*
35	Functional Description	*For Register Description, see Pg. Index C4H ~~123~~.*
37	Functional Description	Add to table: PWRON, PWRDOZE, PWRSLEEP, PWRSUSPEND
37	Functional Description	*For Register Description, see Index C6H-C9H. ~~Pg. 128~~*
37	Functional Description	~~*For Register Description, see Pg. 126*~~.
38	Functional Description	The RAM is valid as long as the VALID bit is set at index 7AH. The RTC RAM contains a write protect feature that is enabled via the *RAMEN bit located in the RTC Mode Register at index 79H.
38	Functional Description	The alarm is enabled through the Real Time Clock configuration registers at indeces 75H-79H. ~~Serial Port.~~
38	Functional Description	For example, power managing peripheral devices might require shutdown . ~~shutting them down.~~
38	Functional Description	In this case, the SMU would intervene in I/O situations, invoking a firmware routine shich would emulate the device's standard ~~standard device's~~ behavior in software.

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
39	Functional Description	System Power Management Modes Table CPU CLOCK DOZE 4 or 8 ~~8 or 16~~ SLEEP 4 or 8 ~~8 or 16~~
40	Functional Description	The following text has been added to the SLEEP State section: The SLEEP state reduces the operating frequency of the internal V30HL CPU. This reduction is controlled by The SLEEP divider value specified in the PMU Resume Status Register located at index DAH. Any write to this register also enables the EXT NMI.
41	Functional Description	~~*For Register Description, see Pg. 130.*~~
41	Functional Description	Power control devices activated by VP pins will be turned off according to the PWRSUSPEND register (C9H).
41	Functional Description	After the NMI is received, the STATUS register (C0H) should be read to determine the NMI source.
42	Functional Description	The CPU should wait until the SAKEUP CODE is present in the PMU Status Register an dPMUREF is low in the PMU Resume ~~Reserve~~ Status Register (DAH).
42	Functional Description	~~*For Register Description, see Pg. 131*~~.
42	Functional Description	The RESUME source identification will be stored in the WU[1:0] status located in the STATUS register (C0H).
42	Functional Description	~~For Register Description, see Pg. 133~~.
49	Functional Description	Serial Port Power Management Modes Table: Serial OSC SLEEP with oscillator disabled~~enabled~~

VG230 REVISION UPDATE
Document: M151013-06 / M151013-07
Old Revision: 1.0 / New Revision: 1.1

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
50	Functional Description	When the programmable time-out expires (Index CFH),
50	Functional Description	~~*For Register Description, see Pg. 140.*~~
50	Functional Description	The PMU ~~in~~ provided automatic power sequencing.
50	Functional Description	Sources for programmable PC card ~~card programming~~ voltage generators include Maxim and Linear Technology.
56	Functional Description	DRAM cannot be mixed with FLASH ~~EPROM~~.
56	Functional Description	For example, if a system has two banks of PSRAM, FlASH can be located in banks 3 and above. The BANK bits must be programmed...
56	Functional Description	Replace table.
57	Functional Description	Remove 128x16 Flash ROM Interface Figure.
60	Register Description	VG230 I/O Map Table: Add: XT PPIG Keyboard Data Register 060H
70	Register Description	(Depending on setting of PPSEL bits of PIO Register, Index 18H & KBDMODE bit of Keyboard Mode Register, Index 08H)
70	Register Description	Bit D[7:0]: In bi-directional mode, the BIDIR bit of the PIO mode register (18H) is...
71	Register Description	(Depending on setting of PPSEL bits of PIO Register, Index 18H & KBDMODE bit of Keyboard Mode Register, Index 08H)

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
72	Register Description	(Depending on setting of PPSEL bits of PIO Register, Index 18H & KBDMODE bit of Keyboard Mode Register, Index 08H)
72	Register Description	Bit D5: Parallel Port direction control. When the BIDIR bit of the PIO (18H) Mode register is set high...
73	Register Description	Index: 2F8H, 2FFH, 3F8H, or 3FFH *(Depending on setting of SPSEL bit of SIO mode Register (10H))*
76	Register Description	Add: ***Notes:*** *LTCHADR should be set to 0 if not using upper address to save power. SDIV[1:0] changes the speed of I/O processing.*
80	Register Description	Bit D4: 0 - Normal Refresh Rate DRAM. *(Only applies during SUSPEND)* 1 - Slow Refresh Rate DRAM. *(Only applies during SUSPEND)*
82	Register Description	Bit D[1:0]: SCLK1 SCLK0~~1~~ NMI Scan Rate
86	Register Description	Add: ***Notes****: KNMIEN must drive scan lines low (Index 09H) befor writing 1. By writing 0 to D4, D3, D2 also clears D7, D6, D5.*
93	Register Description	Add: ***Notes****: To trap a port: Index 1B 0 26 16* *Write 80 0 27 80* *Index 1C 0 26 1C* *Trap port 6C 0 27 6C*
101	Register Description	Add: ***Notes****: Bits D2 and D3=0 after SUSPEND/RESUME.*
106	Register Description	Add: ***Notes****: (Bit D7) Wait until =1 from RESUME*
113	Register Description	Bit D[5:4]: SYSCLK-XT Bus Clock (operates only during external I/O.)

VG230 REVISION UPDATE

Document: M151013-06 / M151013-07

Old Revision: 1.0 / New Revision: 1.1

Rev. 1.0 Page #	Section	Revision 1.0 Revision Marks
119	Register Description	The interrupt is cleared by writing a "1" to the ALARM bit in the RTC status register (7AH). Add: ***Note**: Hardware compares this with index 73H, if equal, alarm is set for the same day.*
123	Register Description	Fix state code table.
127	Register Description	Replace table.
128	Register Description	Name: PMU POWER SUSPEND Register Type: Read/Write Write 0 to ignore EXT/Write 80 to activate EXT)
128	Register Description	Add Table.
133	Register Description	Add: ***Note:** PMUREF should be 0 after resume.*
150	Specifications and Characteristics	Delete Memory Table
153	Specifications and Characteristics	DC Characteristics: Input Low Current - Max -20 ~~–200~~ Output Leakage Curent (Hi-Z) - Min -20~~100~~, Mas 20~~100~~ Output Leakage Curent (**B**i-Dir) - Min -20 ~~-200~~, Mas 20~~200~~
146	Register Description	Add description to IMOD[1:0].
153	Specifications and Characteristics	Add: ***Note**: Entire device max = 1mA*
167-168	Specifications and Characteristics	Pages moved to 159.

169	Specifications and Characteristics	DC Characteristics: Input Low Current - Max 10~~-20~~ Input High Current Vin=2.4v, Vcc=3.6v - Max 10~~20~~ Output Lea kage Current (Hi-Z) - Min -10~~-5~~ Max - 10~~5~~