VADEM

VG330

Single-Chip Platform

Data Manual

Preliminary

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Data Manual
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1 Introduction

1.1 General Description

The VG330 is the next generation of the popular Vadem Single-Chip Platform for portable computing devices. It is targeted specifically towards systems requiring good processing power but which also provide longer battery life than that allowed by conventional CPUs.

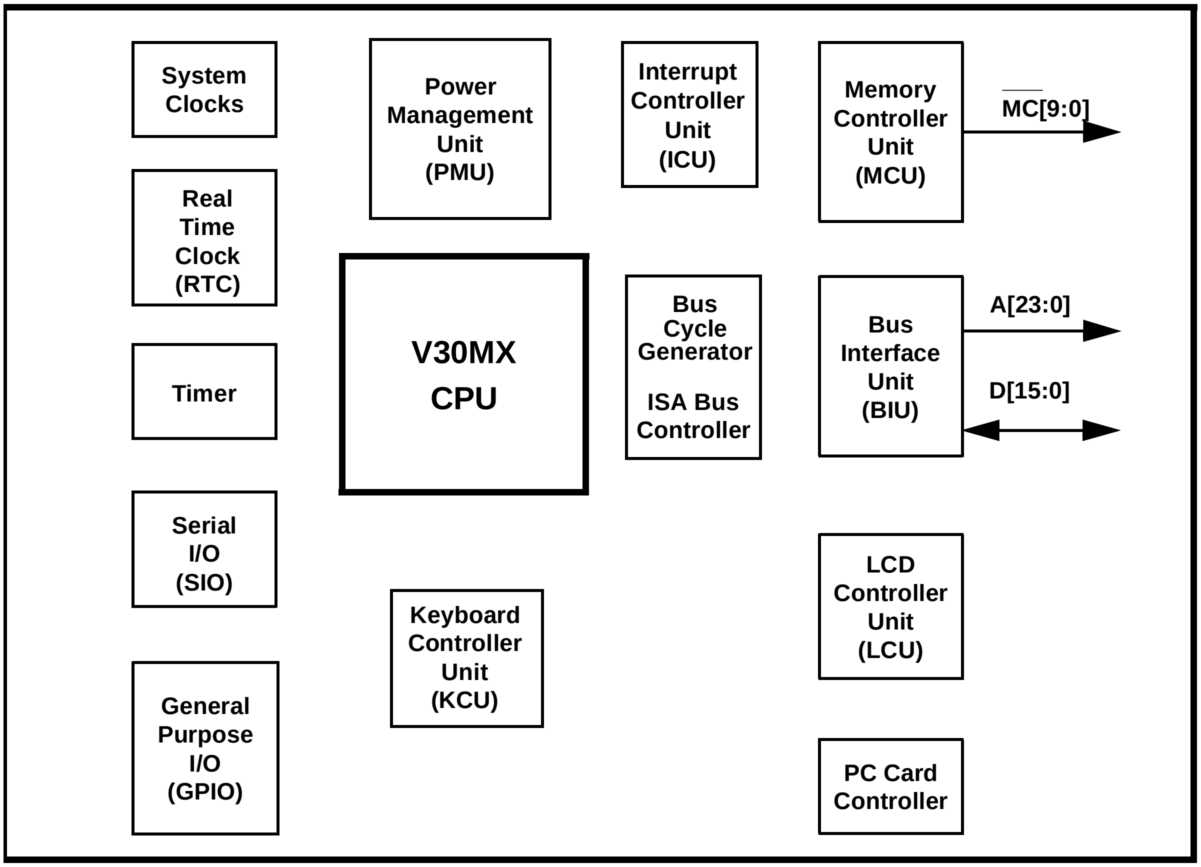
Leveraging on the proven VG230 architecture, the VG330 provides enhanced power management for extended battery operation, along with improved PC CARD capabilities and increased CPU and memory performance. The VG330 also offers increased flexibility with the addition of 24 general purpose input/output (GPIO) pins. The VG330 is packaged in a 160 pin Thin Quad Flat Pack (TQFP).

1.1.1 Processor Capabilities

The VG330 system design integrates system components with the NEC V30MX microprocessor, a high performance 32 MHz CPU core that is Intel 80186 binary code compatible but which provides increased performance over the 80186.

The VG330 operating at 3.3 V and 32 MHz clock rate provides a 2x performance improvement over Vadem's VG230.

The main functional blocks in the VG330 are shown in Figure 1-1.


System Clocks
Power Management Unit (PMU)
Interrupt Controller Unit (ICU)
Memory Controller Unit (MCU)
MC[9:0]
Real Time Clock (RTC)
V30MX CPU
Bus Cycle Generator
ISA Bus Controller
Bus Interface Unit (BIU)
A[23:0]
D[15:0]
Timer
Serial I/O (SIO)
Keyboard Controller Unit (KCU)
LCD Controller Unit (LCU)
General Purpose I/O (GPIO)
PC Card Controller

330D0101

Figure 1-1 VG330 Block Diagram

1.2 Key Features

The VG330 is intended to support cost sensitive 3.3 V applications requiring high performance at low power consumption.

CPU

- NEC V30MX core offers a 2x performance improvement over a 5 V VG230 and a 4x improvement over a 3.3 V VG230.
- The V30MX can be operated at the maximum target CPU clock rate for highest performance
- Under power management control,VG330 can run with a slow clock and even supports a stopped clock.
- Programmable 32, 16, 11 or 8 MHz operating frequencies; full-speed clock rate may optionally be reduced under software control to conserve additional power for non compute-intensive applications.
- CPU supports a low-power Halt state

System Features

- Extensive power management support including DOZE, SLEEP and SMART-CLOCK, Low Battery Resume Inhibit, and Resume Abort.
- 8 and 16 bit Expansion Bus supporting most I/O and Memory ISA cycles, allowing easy connection of ISA devices.
- Real-time clock, dual programmable interrupt controllers and counter/timer.

Memory Support

- High performance integrated memory controller supporting:
  - Fast page-mode DRAM operation.
  - BIOS shadow option.
  - Supports SRAM, PSRAM, DRAM, SRDRAM 16 bit memory configurations. Also supports new high density x8 and x16 DRAM.
  - Extensive support for memory saving “execute-in-place” ROM applications.
  - Flash EPROM support.

LCD Support

- Integrated LCD controller supports a wide variety of LCD panel resolutions. Supports 640x200, 640x400, and 640x480 monochrome graphics modes.

I/O

- Integrated 16450 compatible serial port with HP Infra-Red interface option.
- Integrated PC CARD 2.1/ExCA/JEIDA 4.2 controller providing Intel 82365SL B-step register compatibility.
- 24 general purpose input/output (GPIO) pins provide configuration flexibility for maximizing utilization of all chip functions.

Packaging

- 160 pin Thin Quad Flat Pack (TQFP) package reduces footprint by nearly 25% compared to standard 160 pin QFP devices.

1.3 Architectural Overview

1.3.1 Single-Bus Architecture

The VG330 utilizes a Single-Bus Architecture. All external memory and I/O devices share a common address bus and data bus. A unique set of control signals are provided for each logical subbus such as main memory, Expansion, and PC CARD.

The VG330 is manufactured using a 0.5 micron 3 Volt process. All output pins are 3.3 V and driven to CMOS levels. Selected input pins are 5 V tolerant allowing 5 V devices to connect to the VG330 address and control buses. Any 5 V components connected to the VG330 must support TTL level inputs.

The address bus, A[23:0], and data bus, D[15:0], are dynamically reconfigured on each bus cycle to match the address range and format, data width, and cycle timing of the target I/O or memory device.

1.3.2 Main Modules

The main functional modules in the VG330 are shown in Figure 1-1 and listed in Table 1-1. They are discussed in detail in later chapters.

Table 1-1. VG330 Main Function Modules

ID	Name	Main Functions
CPU	Central Processing Unit	NEC V30MX microprocessor
MCU	Memory Control Unit	Integrated memory controller providing all memory controller functions for system memory; no glue logic required.
BCG / ISA	Bus Cycle Generator	Internal controller for system memory and I/O transactions; provides all required internal system timing
BIU	Bus Interface Unit	Controller for activities on external ISA bus; controls internal address and data path handling
GPIO	General Purpose I/O	I/O pin programmable function matrix
PMU	Power Management Unit	Programmable automatic power control management of functional areas on and off the chip
KCU	Keyboard Controller Unit	XT-compatible standard serial keyboard interface (routed through GPIO pins), and matrix keyboard scanner capability.
ICU	Interrupt Controller Unit	Dual AT-compatible interrupt controller (Intel 8259 compatible) providing 15 interrupt sources.
Timer	Timer	XT-compatible timer (Intel 8254 compatible)
PC Card Ctlr	PC Card Controller	PCMCIA card controller/interface
RTC	Real Time Clock	Vadem-designed real time clock
SIO	Serial I/O	Serial I/O UART and Infrared device I/O
LCU	LCD Controller Unit	Controller and interface to LCD panel

1.3.3 Programmer’s Model

All PC-XT compatible functional elements in the VG330 are programmable using the standard means for programming a PC-XT.

Vadem enhancements to the architecture are programmed using Vadem-specific indexed registers. These registers are described in the chapters covering the functional blocks, and in Chapter 16.

2 Pins and Signals

2.1 Introduction

This section describes VG330 pins and signals.

2.1.1 Capabilities

- The VG330 is manufactured using a 0.5 micron 3 Volt process.
- All output pins are 3.3 V and driven to CMOS levels.
- Selected input pins are 5 V-tolerant, permitting direct-connection to 5 V peripherals.

2.2 Pinout Diagram

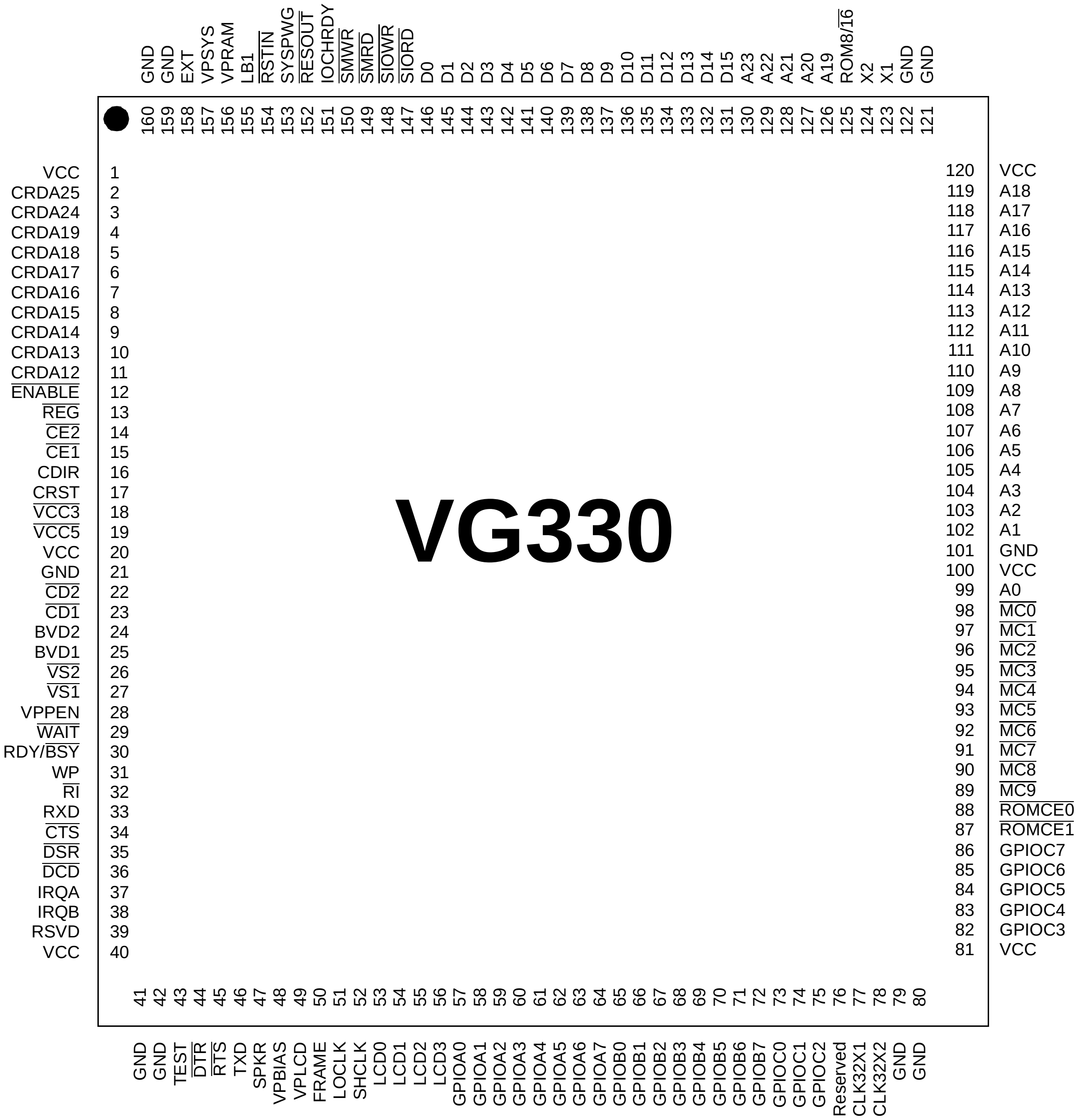


Figure 2-1 VG330 Pinout Diagram

2.3 Pin Assignments - Summary as Alphabetical Listing

Table 2-1. Pins - Alphabetical List

Symbol	Type	Pin No.	Vcc	Characteristics	Iol/Ioh	State During SUSPEND	State during Reset
A[23:0]	O	130:126, 119:102, 99	3.3 V	CMOS three-state	6 mA	Low	A0- Low A[23:2]- Indeterminent
BVD2	I	24	5 V tolerant	CMOS Schmitt	-	High-Z	High-Z
BVD1	I	25	5 V tolerant	CMOS Schmitt	-	High-Z	High-Z
$\overline{\text{CD2}}$	I	22	5 V tolerant	CMOS Schmitt	-	High-Z	High-Z
$\overline{\text{CD1}}$	I	23	5 V tolerant	CMOS Schmitt	-	High-Z	High-Z
CDIR	O	16	3.3 V	CMOS three-state	3 mA	Low	Low
$\overline{\text{CE2}}$	O	14	3.3 V	CMOS three-state	6 mA	High-Z: see note A	High-Z
$\overline{\text{CE1}}$	O	15	3.3 V	CMOS three-state	6 mA	High-Z: see note A	High-Z
CLK32X2	XTL	78	-	Crystal (RTC)	-	Running	Running
CLK32X1	XTL	77	-	Crystal (RTC)	-	Running	Running
CRDA[25:24]	O	2, 3	3.3 V	CMOS three-state	6 mA	Low: see note A	Low
CRDA[19:12]	O	4:11	3.3 V	CMOS three-state	6 mA	Low: see note A	Low
CRST	O	17	3.3 V	CMOS three-state	6 mA	High-Z	High-Z
$\overline{\text{CTS}}$	I	34	3.3 V	CMOS	-	Active	High-Z
D[15:0]	I/O	131:146	3.3 V	CMOS	6 mA	Low	
$\overline{\text{DCD}}$	I	36	3.3 V tolerant	CMOS	-	Active	Indeterminent
$\overline{\text{DSR}}$	I	35	3.3 V	CMOS	-	Active	High-Z
$\overline{\text{DTR}}$	O	44	3.3 V	CMOS three-state	3 mA	Active	High
$\overline{\text{ENABLE}}$	O	12	3.3 V	CMOS three-state	3 mA	High: see note A	High
EXT	I	158	3.3 V	CMOS Schmitt	-	Active	High-Z
FRAME	O	50	3.3 V	CMOS	6 mA	Low	Low

Table 2-1. Pins - Alphabetical List

Symbol	Type	Pin No.	Vcc	Characteristics	Iol/Ioh	State During SUSPEND	State during Reset
GND	GND	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	Ground connections				
GPIOA[7:0]	I/O	64:57	I = 5 V tolerant O = 3.3 V	CMOS Schmitt CMOS	6 mA	Low	Indeterminent
GPIOB[7:0]	I/O	72:65	I = 5 V tolerant O = 3.3 V	CMOS Schmitt CMOS	6 mA	Low	Indeterminent
GPIOC[7:0]	I/O	75:73, 86:82	I = 5 V tolerant O = 3.3 V	CMOS Schmitt CMOS	6 mA	Low	Indeterminent
IOCHRDY	I	151	5 V tolerant	CMOS		Low	Indeterminent
IRQA	I	37	5 V tolerant	CMOS Schmitt		Low	High-Z
IRQB	I	38	5 V tolerant	CMOS Schmitt		Low	High-Z
LB1	I	155	3.3 V	CMOS Schmitt		Active	High-Z
LCD[3:0]	O	56:53	3.3 V	CMOS	6 mA	Low	Low
LOCLK	O	51	3.3 V	CMOS	6 mA	Low	Low
$\overline{\text{MC}}$[9:0]	O	89:98	3.3 V	CMOS three-state	6 mA	Active	Indeterminent
RDY/ $\overline{\text{BSY}}$	I	30	5 V tolerant	CMOS Schmitt		High-Z	High-Z
$\overline{\text{REG}}$	O	13	3.3 V	CMOS three-state	6 mA	High-Z	High-Z
RESERVED	I	76	3.3 V	Pull this pin low through 4.7 KOhm resistor		-	
RESERVED	I	39	3.3 V	Pull this pin low through 4.7 KOhm resistor		-	
$\overline{\text{RESOUT}}$	O	152	3.3 V	CMOS	6 mA	Low	Low
$\overline{\text{RI}}$	I	32	3.3 V	CMOS Schmitt		Active	High-Z
ROM8/ $\overline{\text{16}}$	I	125	3.3 V	CMOS		Active	High-Z
$\overline{\text{ROMCE1}}$	O	87	3.3 V	CMOS three-state	3 mA	Low	Indeterminent
$\overline{\text{ROMCE0}}$	O	88	3.3 V	CMOS three-state	3 mA	Low	Indeterminent
$\overline{\text{RSTIN}}$	I	154	3.3 V	CMOS Schmitt		Active	Low

Table 2-1. Pins - Alphabetical List

Symbol	Type	Pin No.	Vcc	Characteristics	Iol/Ioh	State During SUSPEND	State during Reset
$\overline{\text{RTS}}$	O	45	3.3 V	CMOS three-state	3 mA	Active	High
RXD	I	33	3.3 V	CMOS		Active	High-Z
SHCLK	O	52	3.3 V	CMOS three-state	6 mA	Low	Low
$\overline{\text{SIORD}}$	O	147	3.3 V	CMOS three-state	3 mA	Low	Indeterminent
$\overline{\text{SIOWR}}$	O	148	3.3 V	CMOS three-state	3 mA	Low	Indeterminent
$\overline{\text{SMRD}}$	O	149	3.3 V	CMOS three-state	3 mA	Low	indeterminent
$\overline{\text{SMWR}}$	O	150	3.3 V	CMOS three-state	3 mA	Low	Indeterminent
SPKR	O	47	3.3 V	CMOS three-state	3 mA	Low	Low
SYSPWG	I	153	3.3 V	CMOS Schmitt		Active	Low
TEST	I	43	3.3 V	CMOS Schmitt		Low	Low
TXD	O	46	3.3 V	CMOS three-state	3 mA	Active	Indeterminent
VCC	PWR	1, 20, 40, 81, 100, 120	3.3 V				
$\overline{\text{VCC3}}$	O	18	3.3 V	CMOS	3 mA	High: see note A	High
$\overline{\text{VCC5}}$	O	19	3.3 V	CMOS	3 mA	High: see note A	High
VPBIAS	O	48	3.3 V	CMOS three-state	3 mA	Active- set to Off	High-Z
VPLCD	O	49	3.3 V	CMOS three-state	3 mA	Off	High-Z
VPPEN	O	28	3.3 V	CMOS	3 mA	Low	Low
VPRAM	O	156	3.3 V	CMOS	3 mA	High	High
VPSYS	O	157	3.3 V	CMOS	3 mA	ON -High	High
$\overline{\text{VS2}}$	I	26	3.3 V	CMOS		High-Z	High-Z
$\overline{\text{VS1}}$	I	27	3.3 V	CMOS		High-Z	High-Z
$\overline{\text{WAIT}}$	I	29	5 V tolerant	CMOS		High-Z	High-Z
WP	I	31	5 V tolerant	CMOS		High-Z	High-Z
X2	XTL	124		Crystal (main clock)		Low	Running
X1	XTL	123		Crystal (main clock)		High-Z	Running

Note A. PCMCIA interface is controlled by bit D7, OE, of the PC Card Controller Power and RESET-

DRV Control Register, Index 02H in the PC Card Register set.

2.4 Pin Descriptions

Table 2-2. Pin Descriptions

Symbol	Type	Pin No.	Description
A[23:0]	O	130:126, 119:102,99	Address Bus. All external memory and I/O devices attach to this common address bus. The function of this bus is dynamically set according to the device type being addressed in any cycle: DRAM, SRAM, PC Card, ROM, I/O, or Expansion memory.
BVD2	I	24	Battery voltage status input for PC Card memory cards. Redefined for PC Card I/O cards as $\overline{\text{SPKR}}$.
BVD1	I	25	Battery voltage status input for PC Card memory cards. Redefined for PC Card I/O cards as $\overline{\text{STSCHG}}$.
CDIR	O	16	Direction control for PC Card Odd and Even Byte data buffers. 0 = transfer from VG330 to PC Card (write to card) 1 = transfer from PC Card to VG330
$\overline{\text{CD2}}$	I	22	Card detect status input from PC Card slot.
$\overline{\text{CD1}}$	I	23	Card detect status input from PC Card slot.
$\overline{\text{CE2}}$	O	14	Odd byte chip select signal to PC Card memory and I/O cards.
$\overline{\text{CE1}}$	O	15	Even byte chip select signal to PC Card memory and I/O cards.
CLK32X2	XTL	78	32.768 KHz crystal connection.
CLK32X1	XTL	77	32.768 KHz crystal connection; external clock input to VG330.
CRDA[25:24]	O	2,3	PC card address bits. These bits may be directly connected to the PC card socket.
CRDA[19:12]	O	4:11	PC card address bits. These bits may be directly connected to the PC card socket.
CRST	O	17	Reset signal for PC Card memory and I/O cards.
$\overline{\text{CTS}}$	I	34	Serial Port clear to send.
D[15:0]	I/O	131:146	Bi-directional System Data Bus. All external memory and I/O devices attach to this common data bus. 8-bit devices must reside on the D[7:0] half of the system data bus.
$\overline{\text{DCD}}$	I	36	Serial Port data carrier detect.
$\overline{\text{DSR}}$	I	35	Serial Port data set ready.
$\overline{\text{DTR}}$	O	44	Serial Port data transmit ready.
$\overline{\text{ENABLE}}$	O	12	Enable for PC Card address/control buffers.

Table 2-2. Pin Descriptions

Symbol	Type	Pin No.	Description
EXT	I	158	External switch input. Active high. Used to command SUSPEND/RESUME from outside the VG330. See also description of PMU NMI Mask Register bit D1, MSK_EXT. (Register Index C4H.)
FRAME	O	50	Frame clock to LCD.
GND	GND	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	Ground connections.
GPIOA[7:0]	I/O	64:57	General Purpose I/O Pin Group A. See GPIO pin mapping section in Chapter 10 for programming options.
GPIOB[7:0]	I/O	72:65	General Purpose I/O Pin Group B. See GPIO pin mapping section in Chapter 10 for programming options.
GPIOC[7:0]	I/O	75:73, 86:82	General Purpose I/O Pin Group C. See GPIO pin mapping section in Chapter 10 for programming options.
IOCHRDY	I	151	I/O Channel Ready input, OR'ed with internal ready sources to insert CPU wait states.
IRQA	I	37	System interrupt request input to internal 8259. It is user programmable to be any one of IRQ[7:1], using ICU Mode Register.
IRQB	I	38	System interrupt request input to internal 8259. It is user programmable to be any one of IRQ[7:1], using ICU Mode Register.
LB1	I	155	Low Battery Critical warning input. Active high. Use this in a system design as a critical warning signal that the battery is at exhaustion. If not used in a design, pull this pin low. See also LB2 signal description in Table 2-3.
LCD [3:0]	O	56:53	Display data out to LCD.
LOCLK	O	51	Load clock out to LCD.
$\overline{\text{MC}}$[9:0]	O	89:98	System RAM control signals from MCU. Functions of the pins vary depending on definition of type of system RAM. See Table 8-2, Memory Controller Pin Functions, in Chapter 8, *Memory Controller Unit*.
RDY/ $\overline{\text{BSY}}$	I	30	Ready / $\overline{\text{Busy}}$ status input from PC Card memory card. May be redefined as $\overline{\text{IREQ}}$ for PC Card I/O cards.
$\overline{\text{REG}}$	O	13	Register select signal for PC Card memory and I/O cards.
$\overline{\text{RESOUT}}$	O	152	Active low system RESET output.
$\overline{\text{RI}}$	I	32	Serial Port ring indicator.
ROM8/ $\overline{\text{16}}$	I	125	This is a strap pin option allowing definition of BIOS ROM width. 0 = System design uses a ROM0, a BIOS ROM, that is 16 bits wide. 1= System design uses an eight-bit BIOS ROM.

Table 2-2. Pin Descriptions

Symbol	Type	Pin No.	Description
$\overline{\text{ROMCE}}$[1:0]	O	87,88	ROM chip enable outputs. $\overline{\text{ROMCE0}}$ is asserted for memory read accesses to the BIOS ROM (address range F000:0 - FFFF:F) when the BIOS is not shadowed by RAM. Assertion of ROM chip enable outputs [1:0] for other address ranges may be specified using the VG330 EMS addressing.
$\overline{\text{RSTIN}}$	I	154	VG330 power good input. A system design should provide a means for driving this pin low when power to the VG330 falls below the recommended operating thresholds. $\overline{\text{RSTIN}}$ is used to initialize the internal registers, peripherals, RTC, and microprocessor of the VG330. It will also generate a system reset on the $\overline{\text{RESOUT}}$ output.
$\overline{\text{RTS}}$	O	45	Serial Port request to send.
RXD	I	33	Serial Port receive data.
SHCLK	O	52	Shift clock out to LCD.
$\overline{\text{SIORD}}$	O	147	System I/O Read strobe. This output tells external I/O devices to put their data onto the D[15:0] bus. The VG330 may be programmed to inhibit this output during I/O read cycles to VG330 internal devices.
$\overline{\text{SIOWR}}$	O	148	System I/O Write strobe. This output tells external I/O devices that data is available on the D[15:0] bus. The VG330 may be programmed to inhibit this output during I/O write cycles to VG330 internal devices.
$\overline{\text{SMRD}}$	O	149	System Memory Read strobe. This output tells external memory devices to put their data on the D[15:0] bus. $\overline{\text{SMRD}}$ is not asserted during reads from system RAM, but may be configured to drive the $\overline{\text{OE}}$ pins of ROM0 or ROM1.
$\overline{\text{SMWR}}$	O	150	System Memory Write strobe. This output is used to inform expansion memory devices that data is available on the D[15:0] bus. $\overline{\text{SMWR}}$ is not asserted during writes to system RAM or ROM.
SPKR	O	47	Speaker data output. This output should be buffered and then input to a low pass filter. The output of the filter connects to a speaker.
SYSPWG	I	153	System Power Good input. A system design should provide a means for driving this pin low when the system VCC falls below the recommended operating thresholds. SYSPWG is used to initialize the external system peripherals, via the $\overline{\text{RESOUT}}$ signal, and re-start the internal VG330 clocks. See discussion in Chapter 14.
TEST	I	43	Test Mode / ICE Mode Enable. 0 = normal operation (strap low for normal systems) 1 = test mode (pull high for ICE usage)
TXD	O	46	Serial Port transmit data.
VPBIAS	O	48	BIAS power gate for LCD panel.

Table 2-2. Pin Descriptions

Symbol	Type	Pin No.	Description
$\overline{\text{VCC3}}$	O	18	VCC power gate for PC Cards. Use $\overline{\text{VCC3}}$ to enable the 3.3 V supply. 0 = 3 V supply ON 1 = 3 V Supply OFF
$\overline{\text{VCC5}}$	O	19	VCC power gate for PC Cards. Use $\overline{\text{VCC5}}$ to enable the 5 V supply. 0 = 5 V supply ON 1 = 5 V supply OFF
VPLCD	O	49	VCC power gate for LCD panel.
VPPEN	O	28	Program voltage enable for PC Cards. 0 = Programming supply OFF 1 = Programming supply ON
VPRAM	O	156	VCC power gate for RAM array. 0 = RAM supply OFF 1 = RAM supply ON
VPSYS	O	157	Main System power gate for system power supply. 0 = System supply OFF 1 = System supply ON
$\overline{\text{VS2}}$	I	26	PC card voltage sense input. (See PC Card Interface Register 1FH.)
$\overline{\text{VS1}}$	I	27	PC card voltage sense input. (See PC Card Interface Register 1FH.)
$\overline{\text{WAIT}}$	I	29	Extend bus cycle for PC Card cards.
WP	I	31	Write protect input from PC Card memory cards. May be redefined as $\overline{\text{IOIS16}}$ for PC Card I/O cards.
X2	XTL	124	Main clock crystal input. X2 is the inverted output of X1. If a crystal is used, connect X2 to the crystal circuit. If an external oscillator is used, X2 must be left unconnected.
X1	XTL	123	Main clock crystal input. X1 is an input for a passive crystal circuit, or packaged oscillator providing a 32 MHz signal.
Reserved	I	76	Pull this pin low through 4.7 KOhm resistor.
Reserved	I	39	Pull this pin low through 4.7 KOhm resistor.
VCC	PWR	1, 20, 40, 81, 100, 120	Power.

2.5 Additional Signals

In addition to signals for which there are dedicated pins, the VG330 also supports a number of signals that are available for use in a system design only if they are specifically routed out through a GPIO pin. Table 2-3 shows these signals. For more information, refer to Table 12-1 in Chapter 12 which discusses GPIO functions.

Table 2-3. Signals Routable Through GPIO

Signal Name	Type	Signal Description
$\overline{\text{BHE}}$	O	ISA signal. This is the ISA Byte high enable.
$\overline{\text{CRDMOE}}$	O	PC Card signal: Card Memory Output Enable.
$\overline{\text{CRDMWE}}$	O	PC Card signal: Card Memory Write Enable.
CA22	O	PC Card signal: Card Address bit 22.
CA21	O	PC Card signal: Card Address bit 21.
CA20	O	PC Card signal: Card Address bit 20.
CRD_ALE	O	PC Card signal: Card Address Latch Enable.
GP_RXD	I	Data signal to SIO block. This internal signal may be routed from the GPIO block as either a standard serial RXD signal or as an HP-IR conditioned signal. See Chapter 11, *Serial I/O* , and Chapter 12, *GPIO*. Routing can be allocated by certain GPIO Group registers in the range of index 52H to 5BH, and conditioning is controlled by bit D5, HPIREN, of the SIO Mode Register at index 10H.
GP_TXD	O	Signal from SIO block. This internal signal may be treated as either a standard serial TXD signal or as an HP-IR conditioned signal depending on programmatic control. See Chapter 11, *Serial I/O*, and Chapter 12, *GPIO*. Routing can be allocated by certain GPIO Group registers in the range of index 52H to 5BH. Signal conditioning is controlled by bit D5, HPIREN, of the SIO Mode Register at index 10H.
GPI	I	General purpose input signals which can be mapped to GPIO pins.
GPO	O	General purpose output signals which can be mapped to GPIO pins.
IRQ15/ IRQ7	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
IRQ14/ IRQ6	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
IRQ13/ IRQ5	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
IRQ12/ IRQ4	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
IRQ11/ IRQ3	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
IRQ10	I	Interrupt request line. Input which can be configured to connect to the interrupt controller.

Table 2-3. Signals Routable Through GPIO

Signal Name	Type	Signal Description
IRQ9/ IRQ1	I	Interrupt request lines. Inputs which can be configured to connect to the interrupt controller.
$\overline{\text{IOCS16}}$	I	ISA signal. The I/O chip select 16 signal line is driven low by an I/O resource if it can support data transfers on the upper byte of the data bus, D[15:8].
KBCLK	I	Keyboard Clock from serial keyboard to Keyboard Controller Unit
KBDAT	I	Keyboard Data from serial keyboard to Keyboard Controller Unit
LB2	I	Signal to PMU. Active high. Use LB2 in a design as the Low Battery Caution signal that informs the PMU that the battery is getting low, but is not yet critically low.
LCD M	O	Output signal providing LCD M. (alternate BIAS select for panel)
$\overline{\text{MEMCS16}}$	I	ISA signal. The Memory Chip Select 16 signal line is driven low by an ISA bus memory resource to signal that it can support data transfers on the upper byte of the data bus, D[15:8].
PCS0	O	Output signal providing Programmable Chip Select 0.
PCS1	O	Output signal providing Programmable Chip Select 1.
PCS2	O	Output signal providing Programmable Chip Select 2.
RET (multiple lines)	I	Return lines for matrix keyboard scanning. See discussion in Chapter 10, *Keyboard Controller Unit*.
SCAN (multiple lines)	O	Output: Scan lines for matrix keyboard control. See discussion in Chapter 10, *Keyboard Controller Unit*.
SYSCLK	O	ISA signal. This is the ISA 8 MHz output clock.

3 Electrical Specifications

3.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	-0.5 to +4.6	V
Operating Ambient Temperature	Ta	0 to +85	^oC
Storage Temperature	Tstg	-65 to +150	^oC

3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	3.0	3.3	3.6	V
Operating Ambient Temperature	Ta	0	-	+70	^oC

3.3 Thermal Characteristics

Package	θ_{ja} (0m/s)	θ_{ja} (1m/s)	θ_{jc}
160LQFP	44	38	2.1

3.4 Power

The following table shows the supply current for VG330 measured on evalution board under typical condition.

Parameter	On	Doze	Suspend w/ DRAM (1MB)	Suspend w/ SRAM (1MB)	Suspend w/ PSRAM(1MB)
Current	70mA	10mA	110µA	10.5µA	10.5µA

3.5 DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit
Input low Voltage	V_{IL}	-	0.8	Volt.
Input High Voltage	V_{IH}	2.4		Volt
Output Low Voltage	V_{OL}	0	0.4	Volt
Output High Voltage	V_{OH}	2.4	-	Volt
Input Low current	I_{IL}	-10	10	µA
Input High Current V_{in} = 3.6v,V_{cc}=3.6v	I_{IH}	-20	20	µA
Output Short Circuit Current V_0=0v	I_{OS}	-	100	µA
Output Leakage Current (Hi-Z)	I_{OLZ1}	-10	10	µA
Output Leakage Current (Bi-Dir)	I_{OLZ2}	-10	10	µA
Input Capacitance	C_{IN}	-	10	pF
Output Capacitance	C_{OUT}	-	10	pF
Bi-directional Capacitance	$C_{I/O}$	-	20	pF

3.6 Timing

3.6.1 Clock Timing

Timing for VG330 clocks is shown in Figure 3-1:

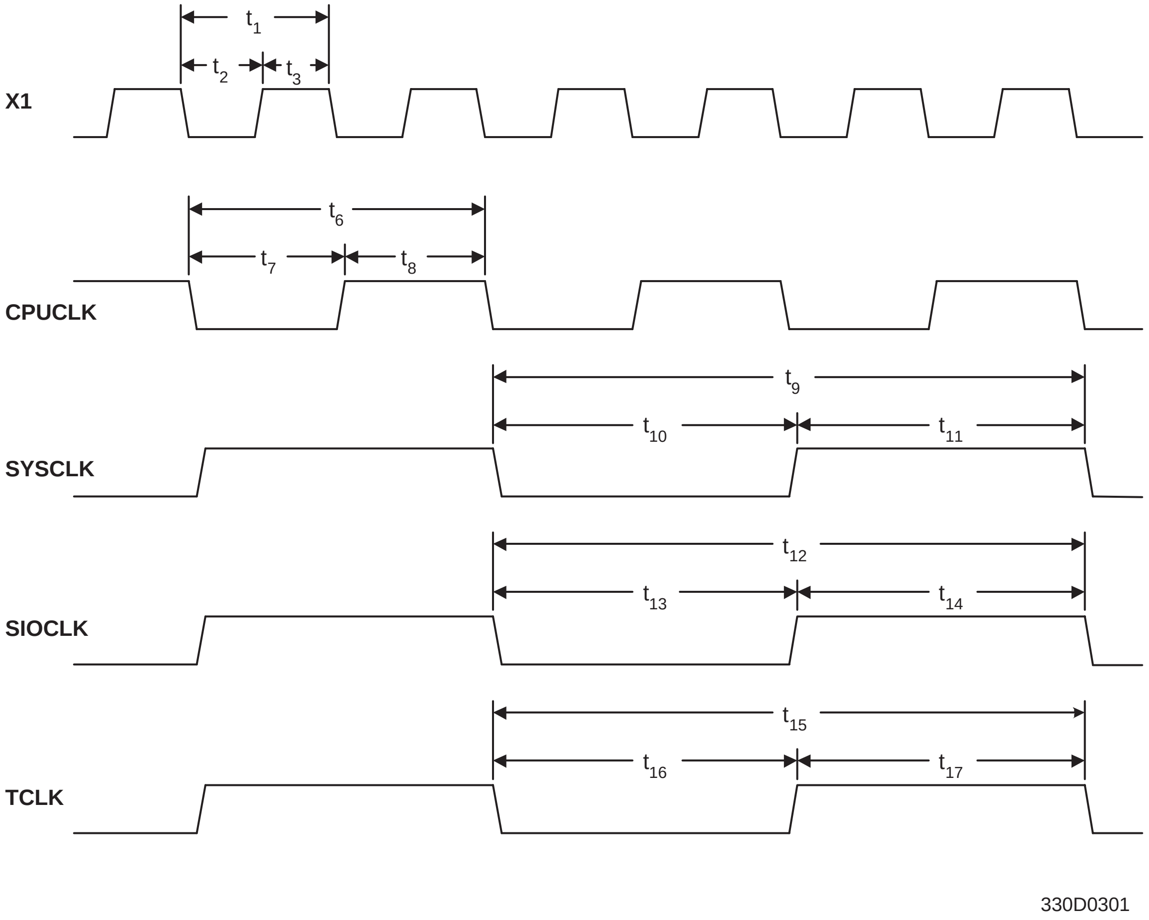


Figure 3-1 VG330 Clocks Timing

Table 3-1. Clock Timing Parameters

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_1	X1 period	31.25 ns			
t_2	X1 low time	15.63 ns			
t_3	X1 high time	15.63 ns			
t_4	X1 rise time				
t_5	X1 fall time				
t_6	CPUCLK period	t_1		$4t_1$	a
t_7	CPUCLK low time	t_2		$2t_1$	
t_8	CPUCLK high time	t_3		$2t_1$	
t_9	SYSCLK period	$2t_6$		$4t_6$	b
t_{10}	SYSCLK low time	t_6		$2t_6$	
t_{11}	SYSCLK high time	t_6		$2t_6$	
t_{12}	SIOCLK period		$t_{13} + t_{14}$		
t_{13}	SIOCLK low time		*(SLCNT+1)*t_1		c
t_{14}	SIOCLK high time		*(SHCNT+1)*t_1		
t_{15}	TCLK period		$t_{16} + t_{17}$		d
t_{16}	TCLK low time		*(LC)* t_1		
t_{17}	TCLK high time		*(HC)*t_1		

a. CPUCLK is the internal processor clock source. Its frequency is programmable through the BCG mode register at Index 01H. Parameters t_6, t_7, and t_8 are calculated based on the CDIV[1:0] bits of this register as follows:

CDIV1	CDIV0	CPUCLK Frequency	t_6	t_7	t_8
0	0	X1	t_1	t_2	t_3
0	1	X1/ 2	$2t_1$	t_1	t_1
1	0	X1/ 3	$3t_1$	$2t_1$	t_1
1	1	X1/ 4	$4t_1$	$2t_1$	$2t_1$

b. SYSCLK is the internal ISA bus clock source. Its frequency is programmable through the BCG mode register at index 01H. Parameters t_9, t_{10}, and t_{11} are calculated based on the SDIV[1:0] bits of this register as follows:

SDIV1	SDIV0	SYSCLK Frequency	t_9	t_{10}	t_{11}
0	0	CPUCLK/4	$4t_6$	$2t_6$	$2t_6$
0	1	CPUCLK/3	$3t_6$	$2t_6$	t_6
1	0	CPUCLK/2	$2t_6$	t_6	t_6
1	1	Illegal	---	---	---

c. SIOCLK is the internal 16450 UART clock source and is programmable through the SIO Clock Control register at index 0FH.

Parameter t_{13} is calculated from the SLCNT[3:0] bits of this register as (SLCNT[3:0] + 1) x t_1.

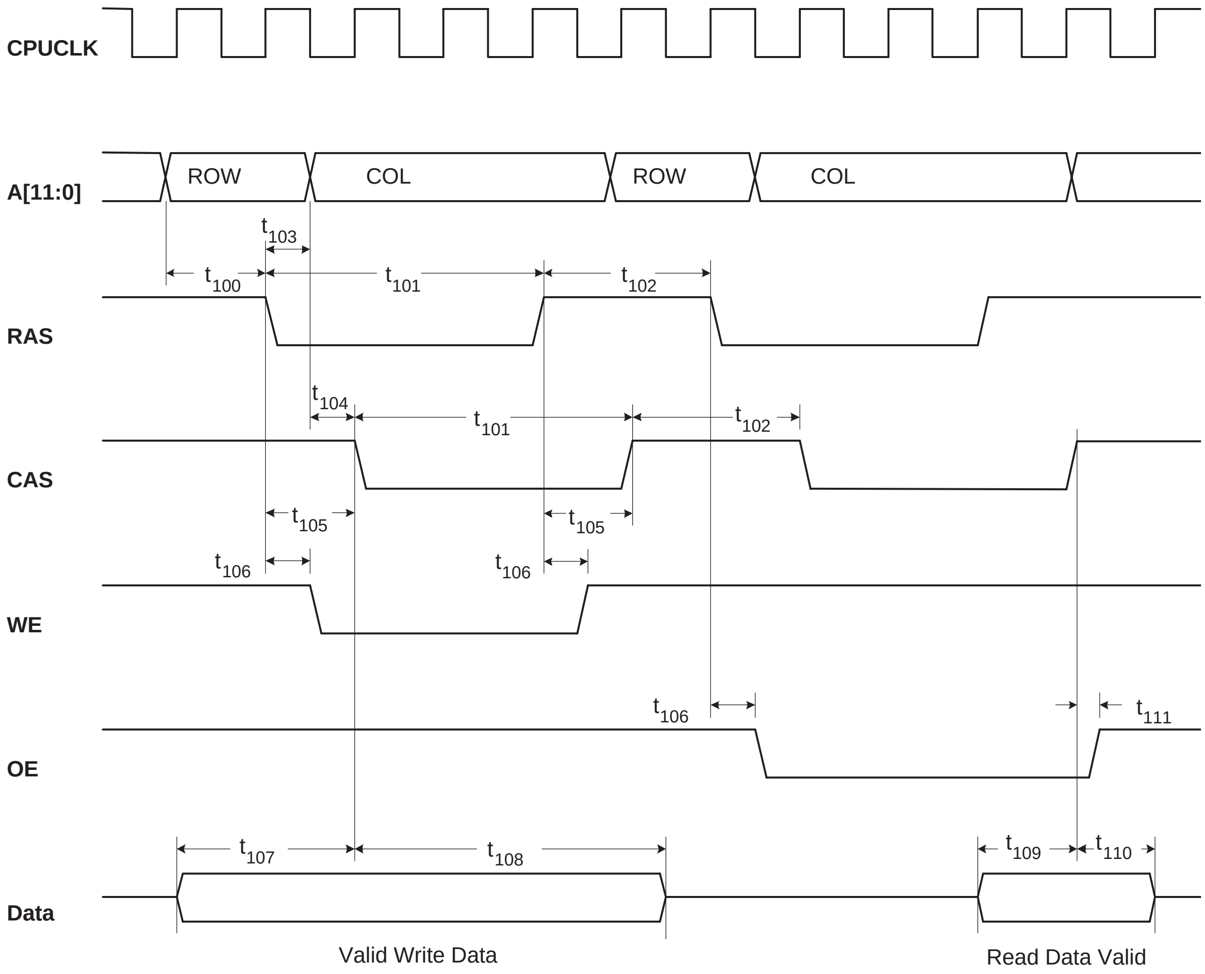
Parameter t_{14} is calculated from the SHCNT[3:0] bits of this register as (SHCNT[3:0] + 1) x t_1.

d. TCLK is the internal 8254 Timer/Counter clock source and is programmable through the Timer Clock Control 1 and Timer Clock Control 2 registers at indices 12H and 13H.

Parameter t_{16} is typically calculated from the TLCNT[3:0] bits of the Timer Clock Control 1 register as (TLCNT[3:0] + 1) x t_1. During a single timer clock cycle, when the alternate timer count specified by the TCNT[3:0] bits of the Timer Clock Control 2 register has been reached, parameter t_{16} will be calculated from the ALTLCNT[3:0] bits of the Timer Clock Control 2 register as (ALTLCNT[3:0] + 1) x t_1.

Parameter t_{17} is calculated from the THCNT[3:0] bits of the Timer Clock Control 1 register as (THCNT[3:0] + 1) x t_1.

3.6.2 DRAM Read/Write Timing



Note: CPUCLK is a VG330 internal signal and is shown for reference only 330D0302

Figure 3-2 DRAM Read/Write Timing

Table 3-2. DRAM Timing for Read/Write Cycles

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{100}	Address setup to RAS	$t_6 + t_7 - 28$			[a]
t_{101}	RAS/CAS pulse width		$(3+W)t_6$		[b]
t_{102}	RAS/CAS precharge	$2t_6$			
t_{103}	Address hold from RAS	$t_8 - 5$			
t_{104}	Address setup to CAS	$t_7 - 13$			
t_{105}	RAS to CAS delay		t_6		
t_{106}	RAS to OE/WE delay		t_8		
t_{107}	Write data setup to CAS	$t_6 - 8$			
t_{108}	Write data hold from CAS	$t_{101} + 1$			
t_{109}	Read data valid to CAS			20	
t_{110}	Read data hold from CAS	0			
t_{111}	CAS to OE delay	0			

[a] Address setup may be increased to 2 t_6 by setting the LODLY bit of the RAM Wait State Register to ‘1’.

[b] *W* is the number of wait states programmed for RAM cycles in the RAM Wait State Register. When bit D7 of RAM Wait State control register at index 07Dh is set to 1, this equation changes to $(1+ W)t_6$.

3.6.3 DRAM Refresh Timing

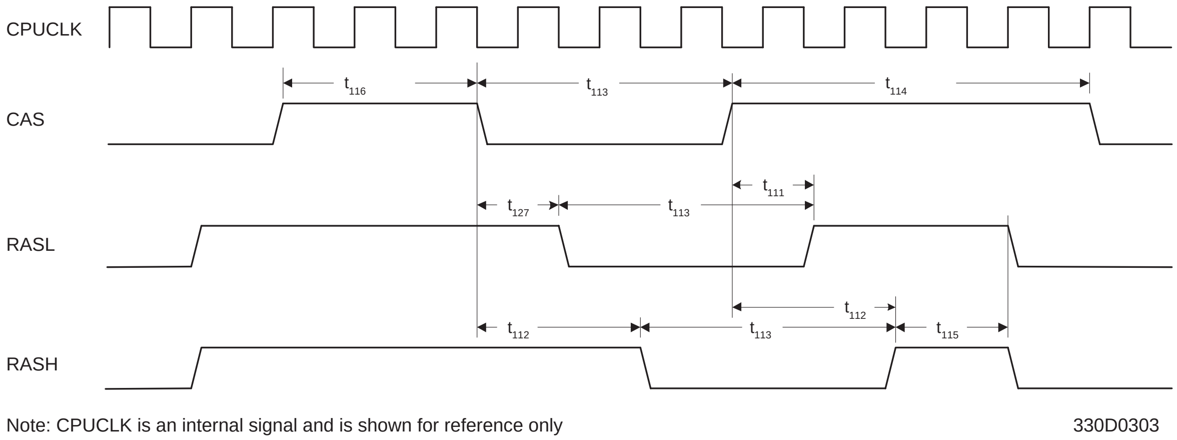

CPUCLK
CAS
RASL
RASH
t116
t113
t114
t127
t113
t111
t112
t113
t112
t115
Note: CPUCLK is an internal signal and is shown for reference only
330D0303

Figure 3-3 DRAM Refresh Timing

Table 3-3. DRAM Timing for Refresh Cycles

Parameter	Description	Min.	Typ.	Max.	Notes
t_{127}	CAS to RASL delay		t_6		
t_{112}	CAS to RASH delay		$2t_6$		
t_{113}	CAS/RASL/RASH pulse width		$3t_6+t_7$		
t_{114}	CAS precharge	$6t_6$			
t_{115}	RASH precharge	$7t_6$			
t_{116}	RAS/CAS cycle to CBR cycle delay	$9t_6$			

3.6.4 DRAM Video Page Mode Read Timing

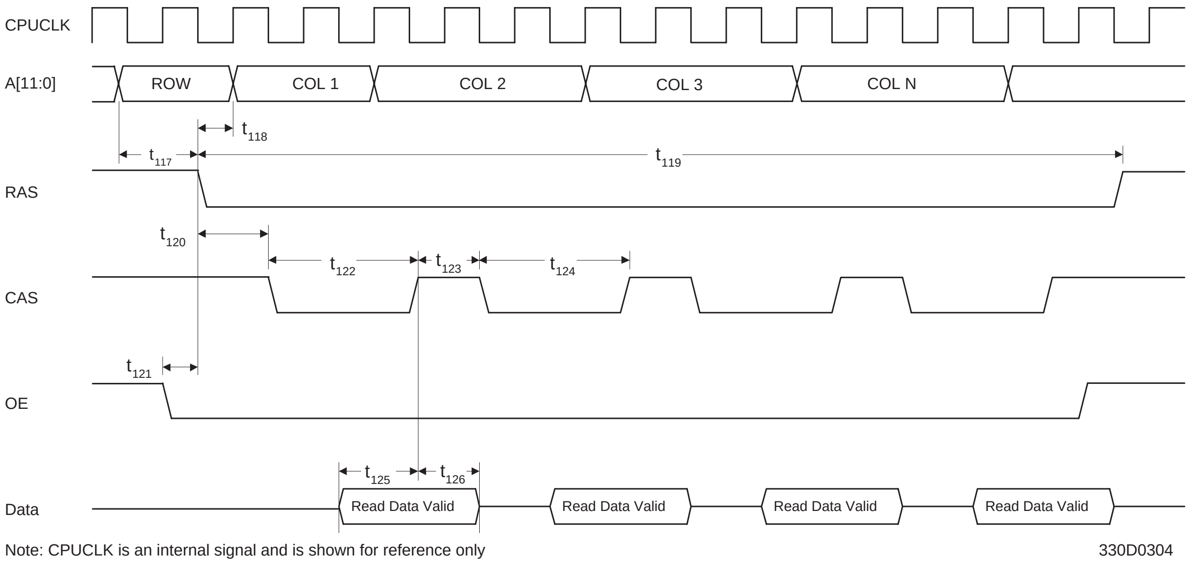


Figure 3-4 DRAM Video Page Mode Read Timing

Table 3-4. DRAM Video Page Mode Read Timing

Parameter	Description	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{117}	Address setup to RAS	t_6 - 25			
t_{118}	Address hold from RAS	t_7 - 5			
t_{119}	RAS pulse width			64 t_6	a
t_{120}	RAS to CAS delay		t_6		
t_{121}	OE to RAS delay		t_8		
t_{122}	CAS pulse width 1st cycle		$2t_6$+t_7		b
t_{123}	CAS precharge		t_8		
t_{124}	CAS pulse width page mode access		$t_{6+}t_7$		b
t_{125}	Read data valid to CAS			20	
t_{126}	Read data hold from CAS	0			

a. RAS pulse width is determined by LCD horizontal resolution. RAS will be generated to fetch one half the pixels of 1 line.

b. CAS pulse width is programmable through the VIDSPD[6:5] bits of the LCD Configuration Control register.

3.6.5 PSRAM /SRAM CPU Read/Write Timing

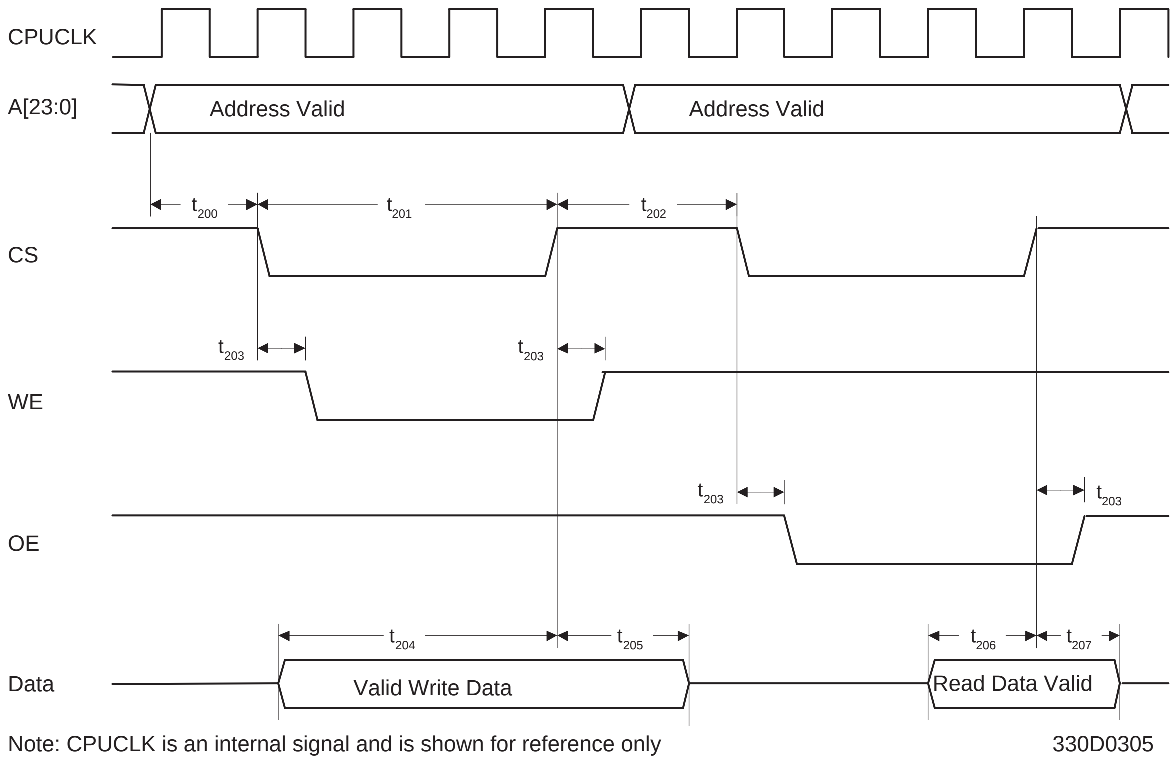


Figure 3-5 PSRAM CPU Read/Write Timing

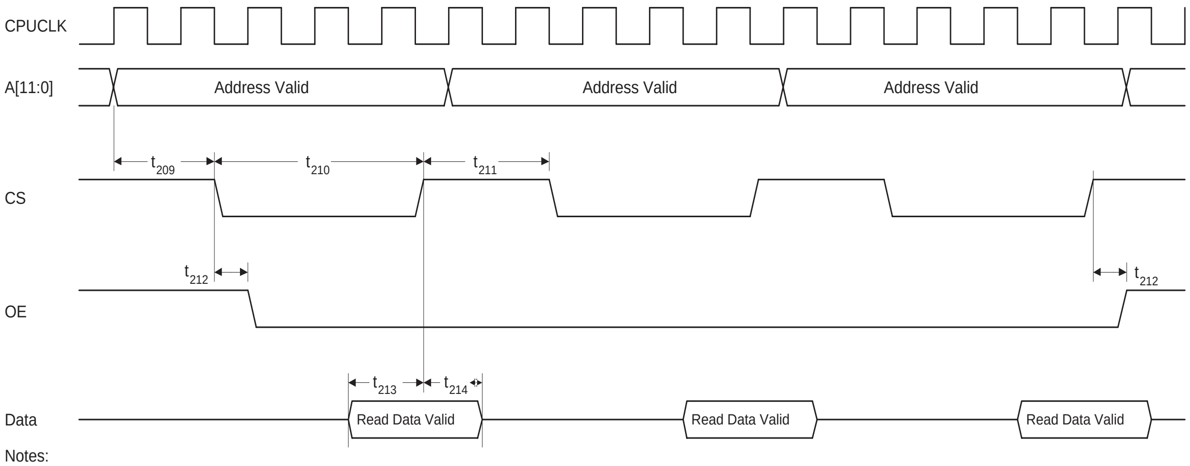
Table 3-5. PSRAM CPU Read/Write Timing

Parameter	Description	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{200}	Address setup to CS	$t_6 + t_7 - 30$			a
t_{201}	CS pulse width		$(3 + W)t_6$		b
t_{202}	CS precharge		$2t_6$		
t_{203}	CS to OE/WE delay	$t_8 - 10$			
t_{204}	Write data setup to CS	$(3+W)t_6$			
t_{205}	Write data hold from CS	t_6			
t_{206}	Read data valid to CS			20	
t_{207}	Read data hold from CS		0		

a. When address latching is enabled, the lead-off delay bit of the RAM Wait State Control register must be enabled and this value then changes to t_6 - 16.

b. *W* is the number of RAM wait states programmed through the RAM Wait State Control register. When bit D7 of RAM Wait State control register at index 07Dh is set to 1, this equation changes to (1+ *W*)t_6.

3.6.6 PSRAM Video Read Timing



Notes:
1. CPUCLK is an internal signal and is shown for reference only.
2. Timing shown is for 80ns speed setting of VIDSPD[1:0] bits.

330D0306

Figure 3-6 PSRAM Video Read Timing

Table 3-6. PSRAM Video Read Timing

Parameter	Description	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{209}	Address setup to CS	$t_6 + t_7$			
t_{210}	CS pulse width		$2t_6+t_8$		a
t_{211}	CS precharge		$t_6 + t_7$		
t_{212}	CS to OE delay		t_8		
t_{213}	Read data valid to CS			20	
t_{214}	Read data hold from CS	0			

a. CS pulse width is programmable through the VIDSPD[6:5] bits of the LCD Configuration Control register.

3.6.7 PSRAM Refresh Timing

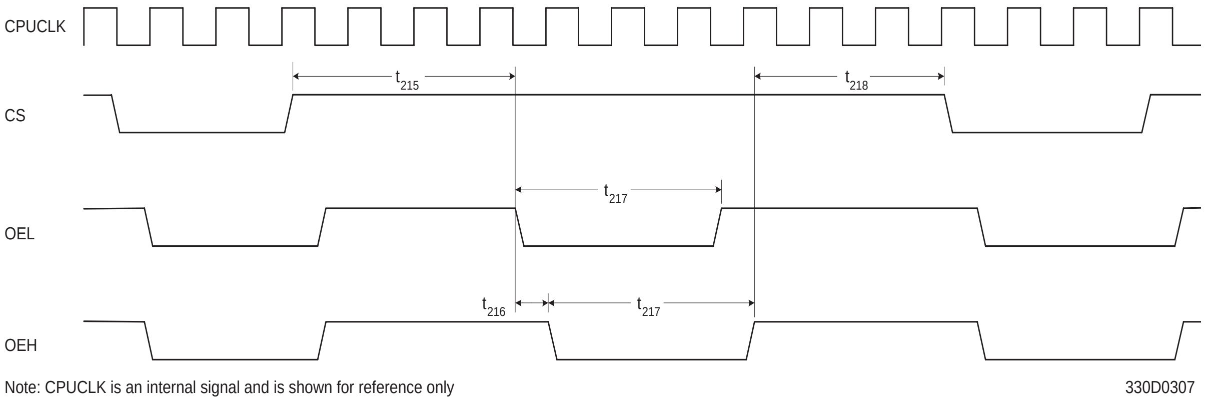


Figure 3-7 PSRAM Refresh Timing

Table 3-7. PSRAM Refresh Timing

Parameter	Description	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{215}	CS to OEL delay	$6t_6$			
t_{216}	OEL to OEH delay		t_6		
t_{217}	OE pulse width		$3t_6$		
t_{218}	OEH to CS	$6t_6$			

3.6.8 ROM/FLASH Timing

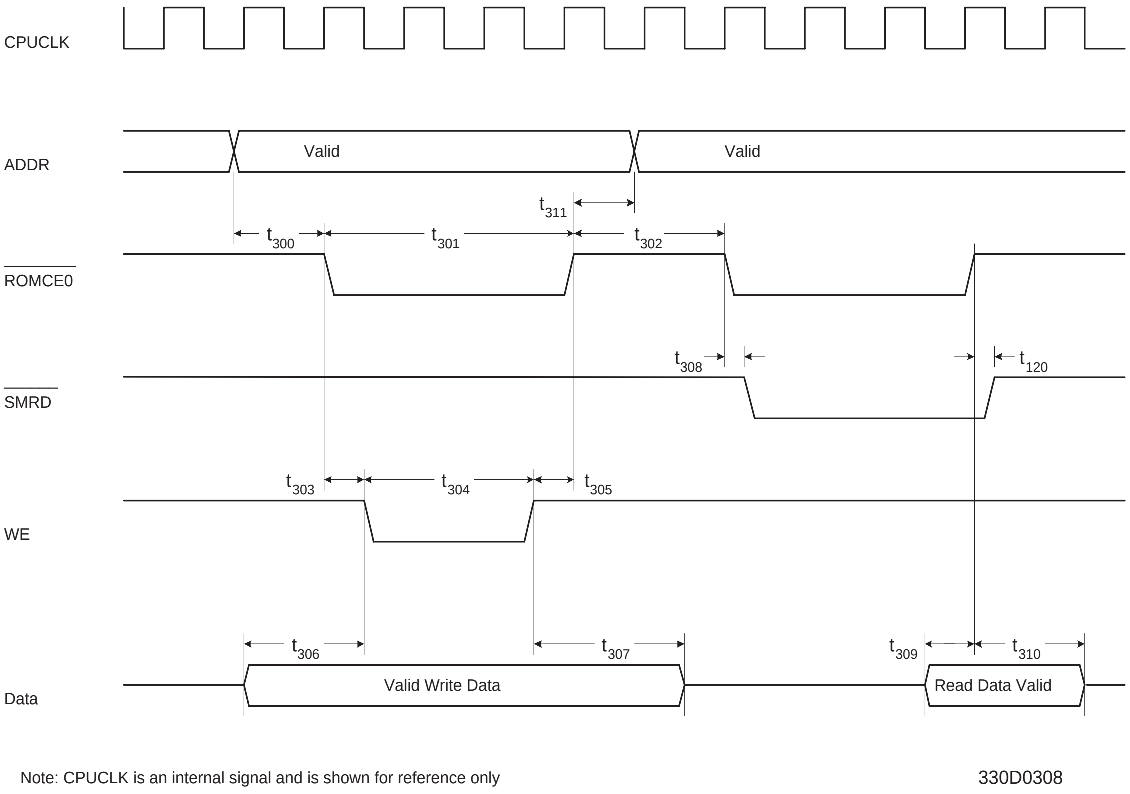


Figure 3-8 ROM Timing

Table 3-8. ROM Timing

Parameter	Description	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{300}	Address setup to $\overline{\text{ROMCE}}$	t_6+t_7-20			a
t_{301}	$\overline{\text{ROMCE}}$ pulse width		(3+*W*) t_6		b
t_{302}	$\overline{\text{ROMCE}}$ precharge		2t_6		
t_{303}	$\overline{\text{ROMCE}}$ to WE delay	t_8-10			
t_{304}	WE pulse width		(2+W)t_6		
t_{305}	WE to $\overline{\text{ROMCE}}$ delay		t_7		
t_{306}	Write data setup to WE	t_8-10			
t_{307}	Write data hold from WE		t_6+t_7		
t_{308}	$\overline{\text{ROMCE}}$ to $\overline{\text{SMRD}}$ delay		0		
t_{309}	Read data valid to $\overline{\text{ROMCE}}$		30		
t_{310}	Read data hold from $\overline{\text{ROMCE}}$	0			
t_{311}	Address hold from $\overline{\text{ROMCE}}$	t_8-10			

a. Address setup for all cycles may be increased to 2t_6 by setting the LODLY bit of the RAM Wait State Control register at Index 7DH.

b. *W* is the number of wait states programmed for the bus cycle as specified in the ROM Wait State Control register at Index 7CH or the RAM Wait State Control register at Index 7DH. When bit D7 of RAM Wait State control register at index 07Dh is set to 1, this equation changes to (1+ *W)*$t_{6.}$

3.6.9 LCD Panel Timing

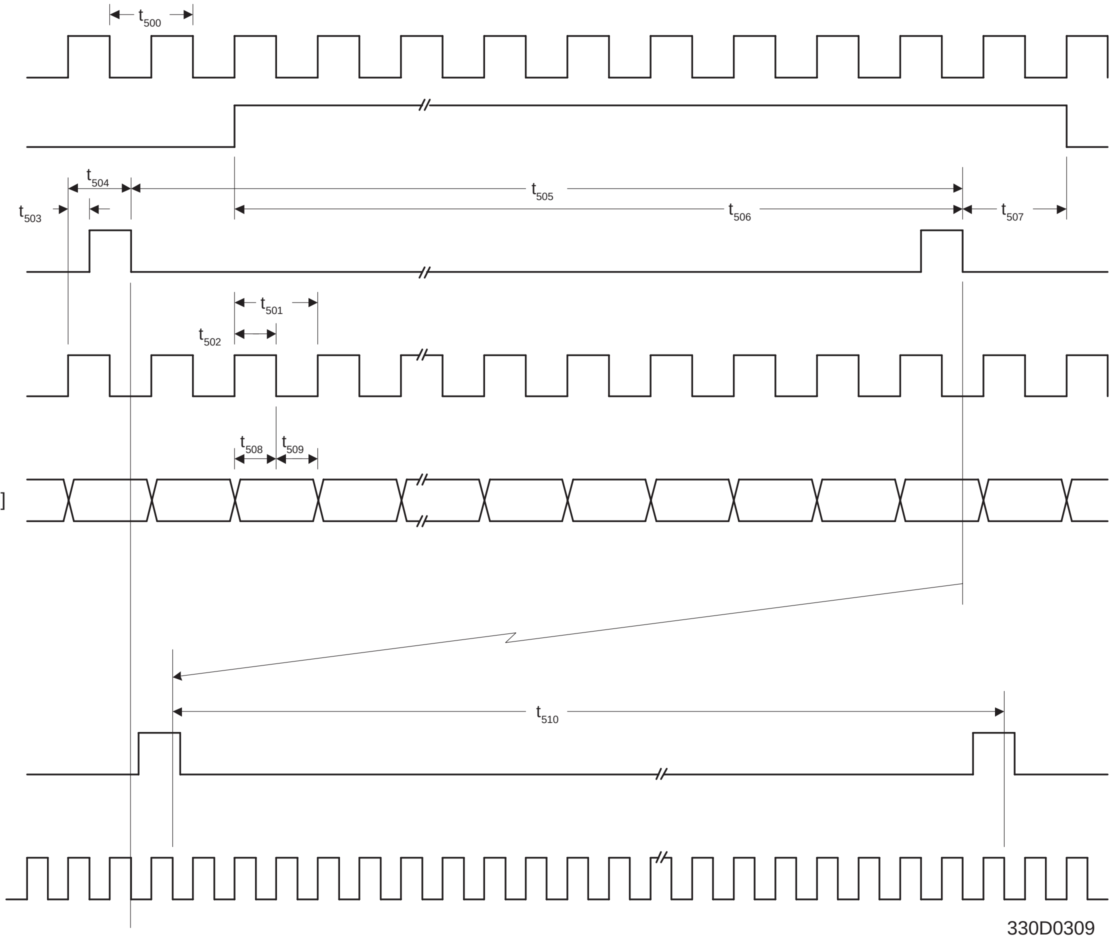


Figure 3-9 LCD Panel Timing

Table 3-9. LCD Panel Timing

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{500}	PCLK period		t_6 x 2 CLKPS[2:0]		a
t_{501}	SHCLK period		(T1D[4:0] + 1) x t_{500}		See T1D register.
t_{502}	SHCLK high time		(T2D[4:0] + 1) x t_{500}		See T2D register.
t_{503}	SHCLK high to LOCLK high time		(T3D[4:0] + 1) x t_{500}		See T3D register
t_{504}	SHCLK high to LOCLK low time		(T4D[4:0] + 1) x t_{500}		See T4D register
t_{505}	LOCLK period		t_{501} x ((LCDX[7:0] + 1)x*W*)		b
t_{506}	FRAME setup to LOCLK		t_{505} - 2 x t_{501}		b
t_{507}	FRAME hold from LOCLK		2 x t_{501}		c
t_{508}	Data setup to SHCLK		t_{502}		
t_{509}	Data hold from SHCLK		t_{501} - t_{502}		
t_{510}	FRAME period		2 x t_{505} x (LCDY[7:0] + 1)		See LCD Vertical Resolution register

a. PCLK is the video prescale clock and is generated by dividing CPU clock by the factor specified in the CLKPS[2:0] bits of the LCD T1 register.

b. *W* is defined based on the bit width of the LCD data bus as follows:

1 bit data : W = 4
2 bit data : W = 2
4 bit data : W = 1

FRAME is asserted 2 SHCLK cycles after assertion of LOCLK for the last display line.

c. FRAME is negated 2 SHCLK cycles after assertion of LOCLK for the first display line.

3.6.10 ISA Timing

Table 3-10. ISA Timing

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)	Notes
t_{400}	Address setup to command	$4t_6$ - 10			a
t_{401}	Command pulse width		1.5 t_9+*W* t_9		b
t_{402}	Write data setup to command	t_6+ t_8 + t_{11}+ 3			c
t_{403}	Write data hold from command	t_7 + t_{11} - 10			
t_{404}	Address hold from command		t_{11} -17		
t_{405}	Command precharge	1.5 t_9			
t_{406}	Address hold from even byte command	t_{11} + t_7 - 10			
t_{407}	Read data valid to command			30	
t_{408}	Read data hold from command		0		
t_{409}	$\overline{\text{IOCS16}}$ setup to command			t_9 + 35	
t_{410}	$\overline{\text{IOCS16}}$ hold from command		0		
t_{411}	Address setup to 16 bit memory command	$3t_6$ - 10			
t_{412}	16 bit memory command pulse width		2 t_9 +*W* t_9		
t_{413}	$\overline{\text{MEMCS16}}$ valid from A[19:1]			3 t_6 - 10	
t_{414}	$\overline{\text{MEMCS16}}$ hold from command		0		
t_{415}	IOCHRDY delay from command			t_9 + *W*t_9 -25	
t_{416}	Command delay from IOCHRDY	t_9 -25		$2t_9$	

a. When address latching is enabled, variable $4t_6$ is changed to $2.5t_6$.

b. *W* is the number of wait states programmed for the bus cycle as specified in the Expansion Bus I/O Wait State Control or Expansion Bus Memory Wait State Control registers at Indexes 35H or 36H respectively.

c. For 16 bit memory cycles, remove parameter t_{11} from equation.

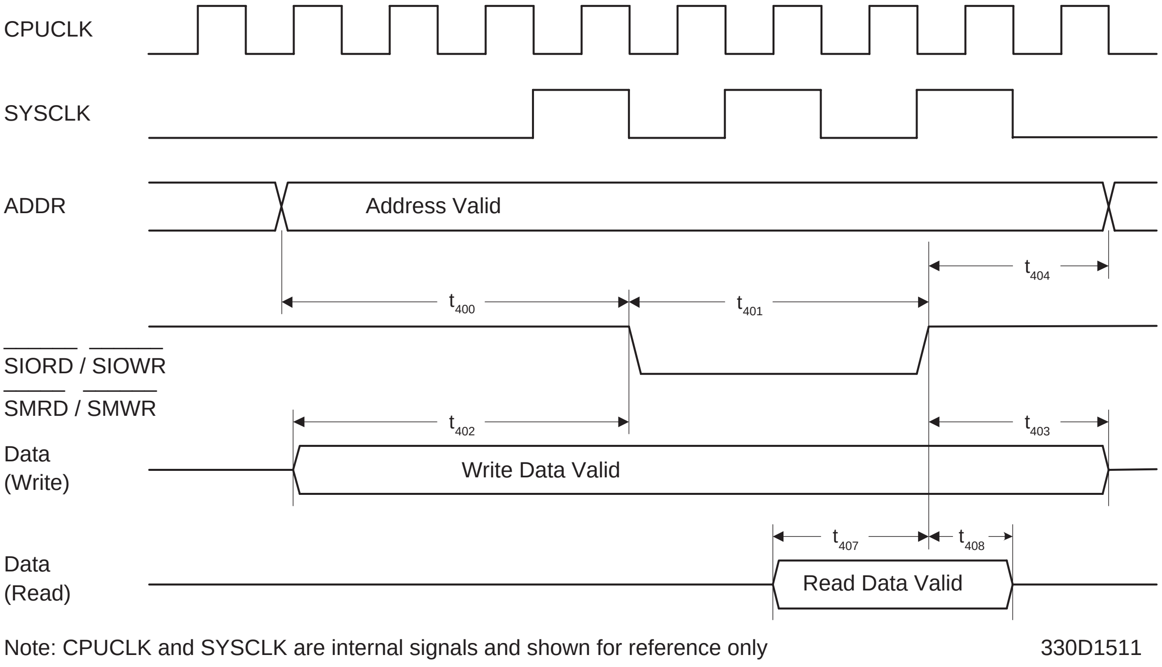


Figure 3-10 ISA Cycle Timing - 8-Bit I/O or Memory Access

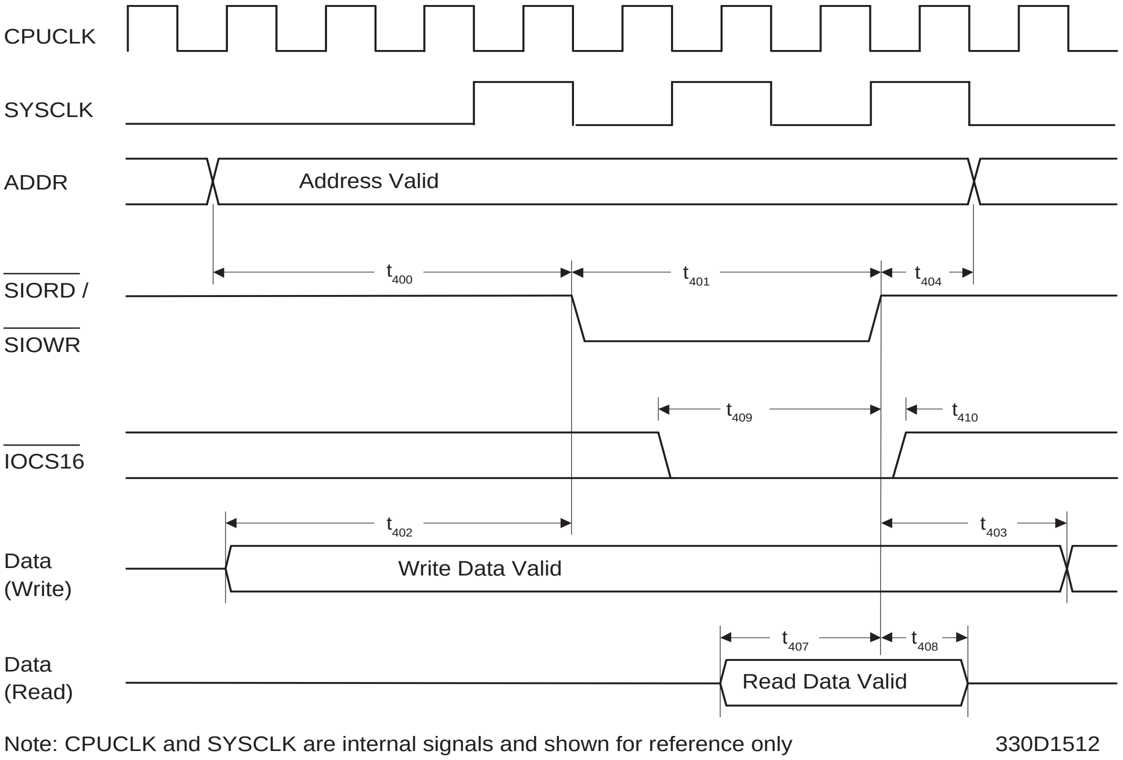
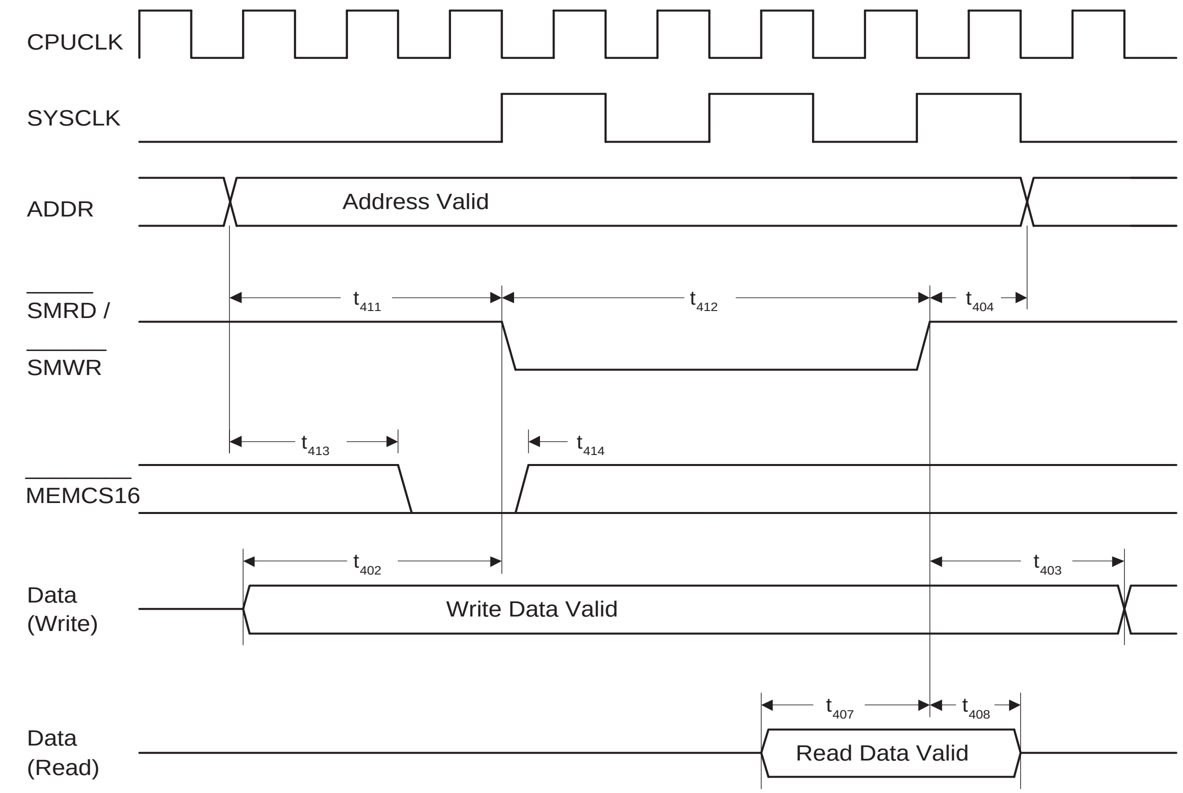
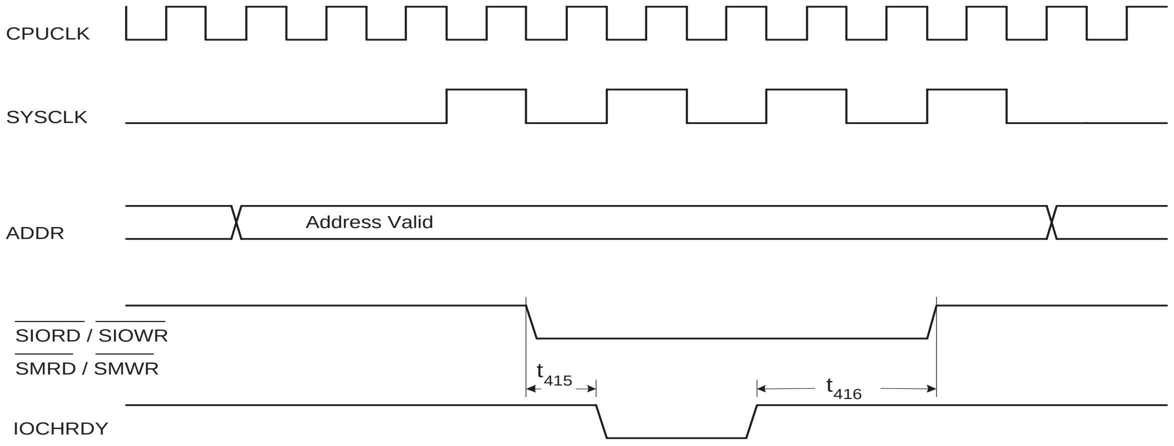


Figure 3-11 ISA Cycle Timing - I/O Access to 16-Bit Device



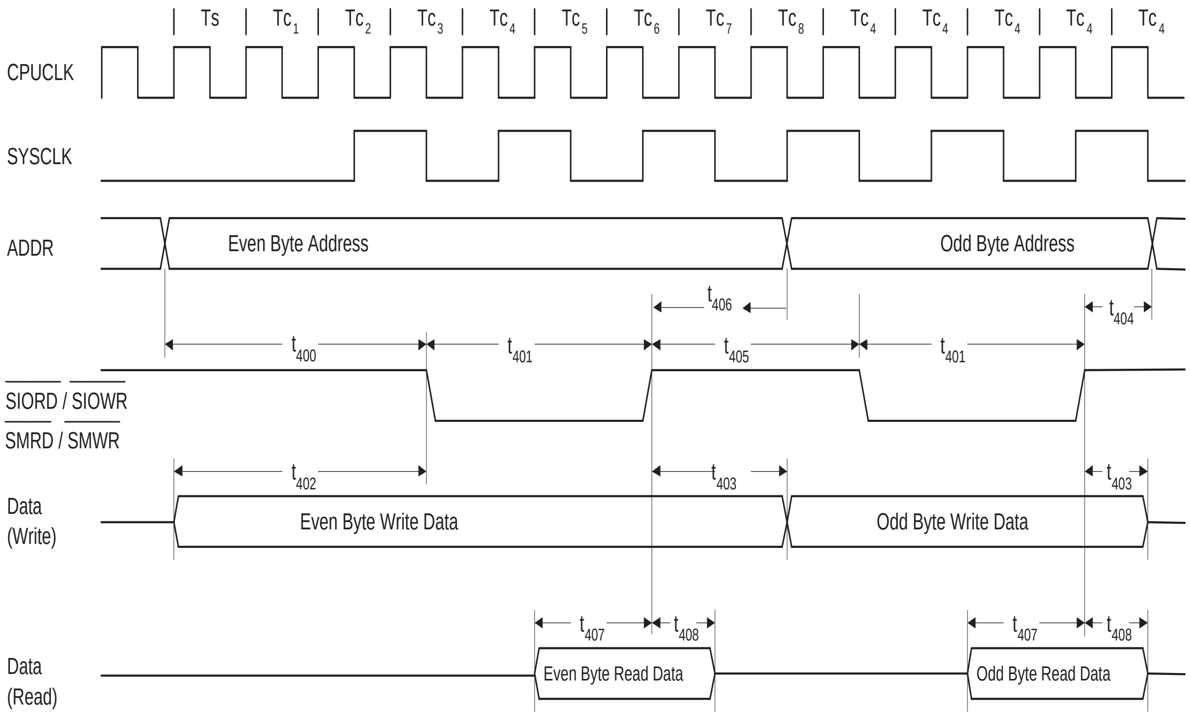
Note: CPUCLK and SYSCLK are internal signals and shown for reference only 330D1513

Figure 3-12 ISA Cycle Timing - Memory Access to 16-bit Device



Note: CPUCLK and SYSCLK are internal signals and shown for reference only 330D1514

Figure 3-13 ISA Cycle Timing - IOCHRDY Timing



Note: CPUCLK and SYSCLK are internal signals and shown for reference only

330D1515

Figure 3-14 ISA Cycle Timing - 16-Bit Access to 8-Bit Device

3.6.11 PC Card Timing

PC CARD MEMORY CYCLE TIMING

Table 3-11. PC Card Memory Cycle Timing

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)	Note
t_{600}	Address setup to command		$3t_6$		
t_{601}	Command pulse width		$t_9 + t_{10} + Wt_9$		a
t_{601}	Command pulse width for 16 bit		$2t_9 + Wt_9$		a
t_{602}	CDIR delay from SMRDB low or SIORDB low		0		
t_{603}	CDIR delay from SMRDB high or SIORDB high		0		
t_{604}	Read data valid to command			30	
t_{605}	Read data hold from command		0		
t_{606}	Write data setup command	$t_6 + t_8 + t_{11}$			b
t_{607}	Write data hold from command	$t_7 + t_{11\text{-}10}$			
t_{608}	WAITB delay from command		$t_9 + Wt_9$		a
t_{609}	Command delay from WAITB	t_9		$2t_9$	

a. W is the number of wait states programmed for the bus cycle as specified in the expansion bus memory wait state register and/or the PC card memory wait state selection register.

b. For 16 bit memory cycle, remove t_{11} from equation.

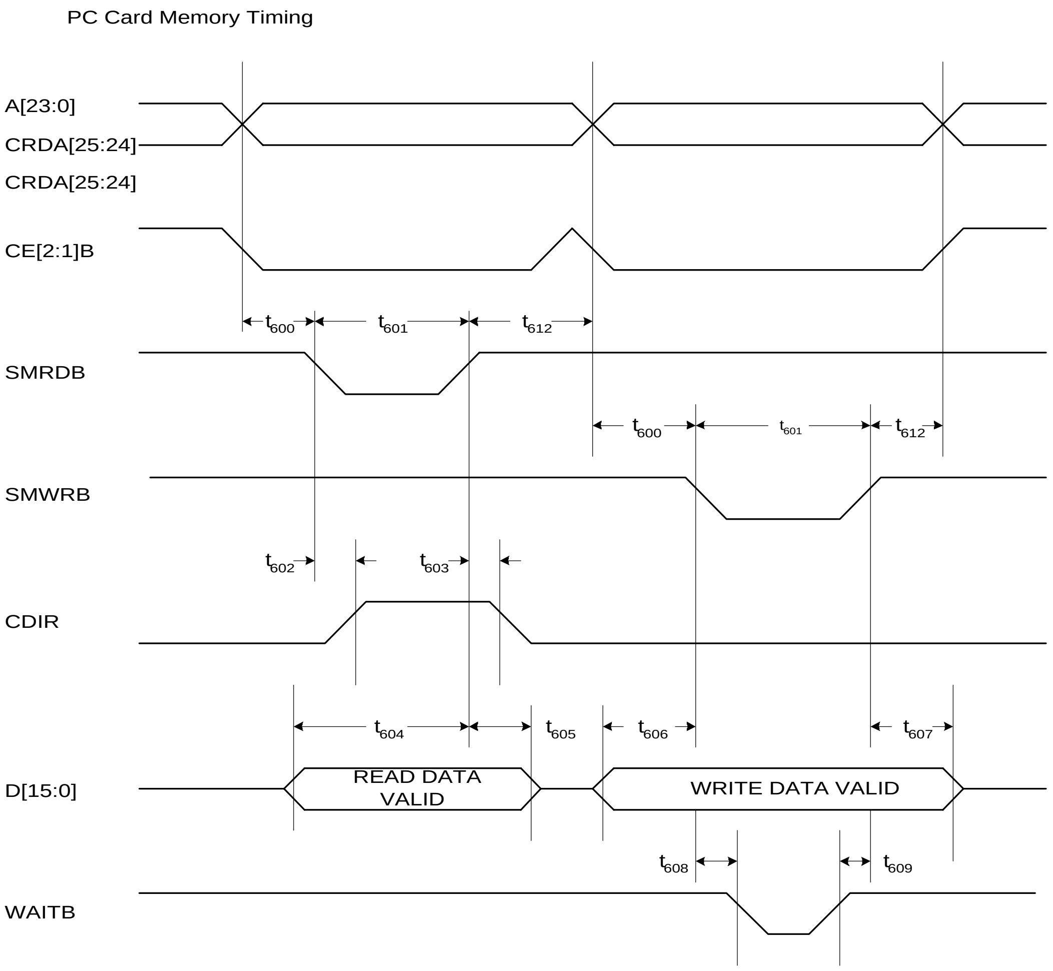


Figure 3-15 PC Card Memory Timing

Table 3-12. PC Card IO Cycle Timing

Parameter	Descriptions	Min. (ns)	Typ. (ns)	Max. (ns)
t_{610}	IOCS16B setup to command			t_9+35
t_{611}	IOCS16B hold from command		0	
t_{612}	Address hold from command	t_{11}-15		

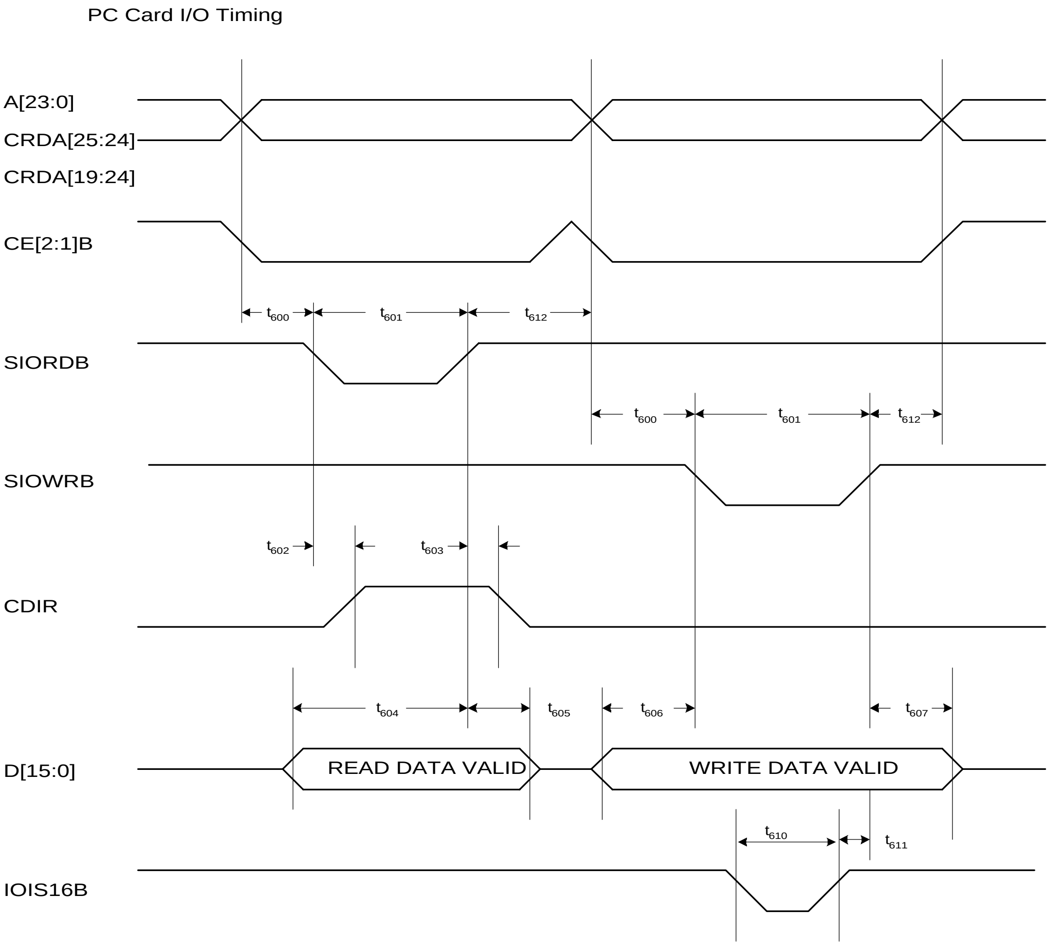
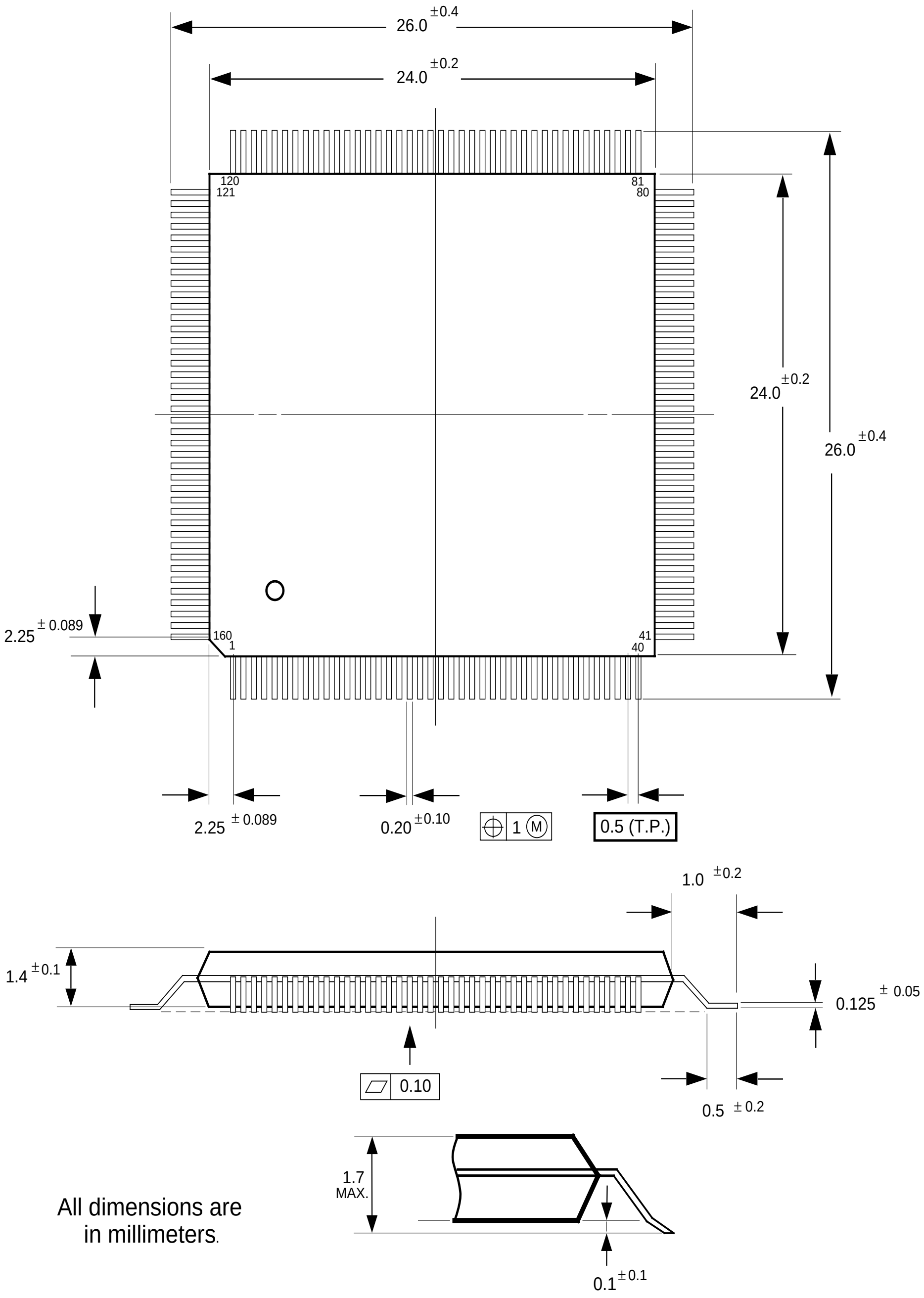


Figure 3-16 PC Card IO Timing

4 Mechanical Data

4.1 Package Dimensions

The VG330 160-pin TQFP package is shown in Figure 4-1.



All dimensions are
in millimeters.

Figure 4-1 Package Dimensions

4.2 Ordering Information

Contact Vadem or customer representative near you.
For list of customer representatives, See us at
WWW.VADEM.COM.

5 System Clocks

5.1 Introduction

The VG330 uses two external clocks. They are:

- 32.768 KHz Low Frequency Clock
- 32 MHz High Frequency Clock

5.1.1 Capabilities

- The VG330 can use either a 32.768 KHz clock crystal or an externally-supplied clock.
- The VG330 can use either a 32 MHz clock crystal or an externally-supplied clock.
- The VG330's 'SmartClock' is a mechanism providing the ability to sense system activities to determine when it is possible to slow the system clock to save power. Subsystems that are not active then consume little power.

5.2 Clocks

Figure 5-1 shows connections and circuit design for the clock crystals.

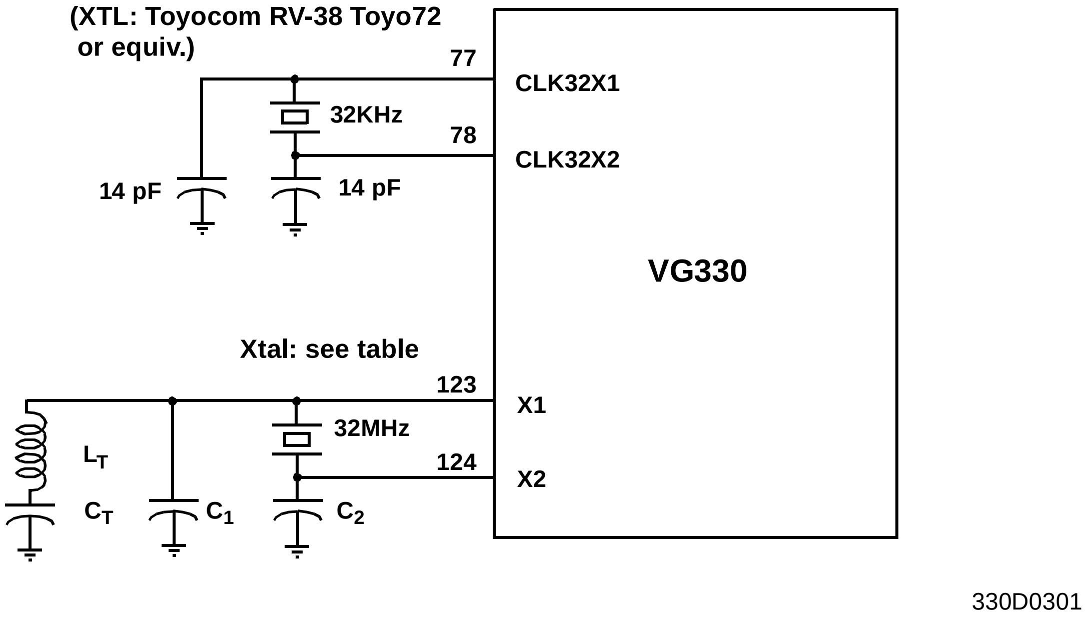


Figure 5-1 VG330 Crystal Oscillator Connections

5.3 Related Pins

Table 5-1. Clock-Related Signals and Pins

Pin Name	Type	Pins	Functions
CLK32X2	XTL	78	32.768 KHz crystal connection
CLK32X1	XTL	77	32.768 KHz crystal connection; external osc. connection
X2	XTL	124	32 MHZ crystal oscillator (system and CPU)
X1	XTL	123	32 MHZ crystal oscillator; external osc. connection

5.3.1 High Frequency Clock

The 32 MHz clock can be supplied by either the internal oscillator, used with a 32 MHz or slower crystal, or an external digital clock source.

The 32 MHz clock is the prime source for the CPU clock and the system clock. The Power Management Unit can control how this clock is used. Depending on the Power Management State, the CPU clock can be slowed or even shut off, reducing CPU power consumption. Levels of system activities can be detected by the PMU's SmartClock, which governs such reductions.

For information on this, see *SmartClock* on page 14-18.

When using an external 32 MHz clock source instead of a crystal circuit, the clock signal must be connected to pin 123, X1, and pin 124 must be left open.

Recommended parameters for the circuit shown in Figure 5-1 are shown in Table 5-2 below:

Table 5-2. High Frequency Clock Parameters

Frequency	External Capacitance		Series Resonation Circuit		Resonator[a]
	C_1 (pF)	C_2 (pF)	C_T (pF)	L_T (μH)	
4 MHz	14	15	-	-	**TOYOCOM 204B-OB**
8 MHz	13	14	-	-	**TOYOCOM 210B-OH**
16 MHz	35	35	-	-	**TOYOCOM 228A-OB**
32 MHz	35	35	670	3.19	**TOYOCOM 229A-OB**

a. Using the part listed here or equivalent.

5.3.2 Low Frequency Clock

The 32 KHz clock can be supplied by either an external 32.768 KHz crystal or an external 32.768 KHz clock source.

The 32 KHz clock runs at all times as long as power is applied to the VG330. This is the only oscillator running when the VG330 is in the SUSPEND or the OFF Power Management states.

When using an external 32 KHz source, it must be connected to pin 77, CLK32X1, with pin 78 left open.

32 KHz Crystal Parameters

Recommended parameters for the 32 KHz crystal are shown in Table 5-3:

Table 5-3. 32 KHz Crystal Parameters

Parameter	Value
Frequency	32.768 KHz +/- 30 ppm
Quality Factor	Q = 80,000 to 100,000
Load Capacitance	CL = 8 to 13 pF
Series Resistance	RS = 20 to 40 KOhms
Shunt Capacitance	C0 = 1.0 to 1.5 pF
Motional Capacitance	C1 = .0025 pF to .0035 pF
Capacitance Ratio	C0/C1 = 400 to 520
Drive Level	1 mW (min)
Aging	3 ppm/year

5.4 Clocks and Power Management States

The nature of system clocking in relationship to power control states is discussed in Chapter 14, *Power Management Unit*.

The following is a brief summary, listed by Power Management state:

Table 5-4. Clock Condition Versus Power Management States

PMU State	32 Khz Clock	32 MHz Clock	Notes
-	Off	Off	System power has been removed .
OFF Mode	On	Oscillator is stopped.	In the OFF mode, the VG330 stops all clock sources except the 32.768 KHz oscillator, and all I/O pins, including the memory interface, are either brought to a high impedance state or driven low. It is assumed that within a system, only the VG330 remains powered during OFF mode, though SIO level translators or PC Card buffers, if used, might remain on.
SUSPEND Mode	On	Oscillator is stopped.	In SUSPEND Mode, the system is in stasis, with almost all activity suspended; however, the MCU still performs memory refresh to retain data.
SLEEP Mode	On	Oscillator is active but system clocks are under control of the SmartClock.	In SLEEP Mode, the PMU's SmartClock mechanism requests that the BCG slow the system clocks to conserve power.
DOZE Mode	On	Oscillator is active but system clocks are under control of the SmartClock.	In DOZE Mode, the PMU's SmartClock mechanism requests that the BCG slow the system clocks to conserve power.
ON Mode	Operational	Operated at full speed.	In ON Mode, the PMU allows all internal clock buses to operate at full speed.

5.4.1 Processor Clock Handling

The processor clock can be optionally stopped under the following conditions:

- Following a HALT command.
- While the CPU is not the bus master.
- During Expansion bus cycles.

Each of the above can be independently enabled. For stop clock on HALT, the processor clock is stopped after a HALT cycle has been detected on the bus and restarted when a bus master request, interrupt, or NMI is generated.

When bus masters such as the MCU performing a memory refresh, or the display controller requiring memory access, are granted the bus, the processor clock may also be stopped. The clock is first stopped after the processor acknowledges the hold request by asserting HLDAK. The clock remains stopped until the requesting device releases HRQ.

In the other cases, the processor clock is stopped once the cycle is under way and remains stopped until the ready signal, RDY, is asserted.

5.5 Clock Usage By Function Block

Figure 5-2 shows how the clocks are distributed to subsystems within the VG330.

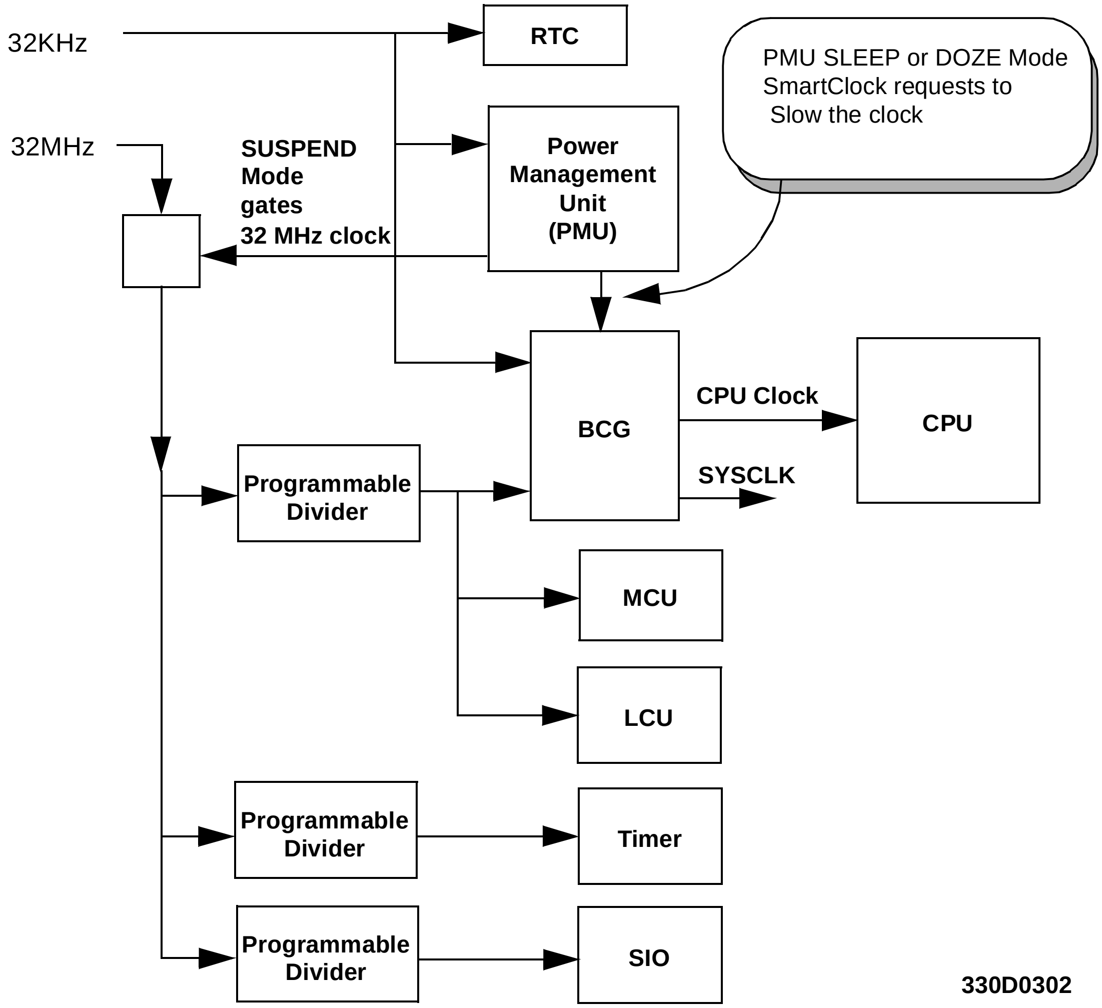

32KHz
32MHz
RTC
PMU SLEEP or DOZE Mode SmartClock requests to Slow the clock
SUSPEND Mode gates 32 MHz clock
Power Management Unit (PMU)
BCG
CPU Clock
SYSCLK
CPU
Programmable Divider
MCU
LCU
Programmable Divider
Timer
Programmable Divider
SIO
330D0302

Figure 5-2 VG330 Clock Tree

5.6 Related Registers

Register	Address
BCG Mode Register	Index 01H
Clock Control Register	Index DEH
SIO Clock Control Register	Index 0FH
Timer Clock Control 1 Register	Index 12H
Timer Clock Control 2 Register	Index 13H

6 Bus Architecture

6.1 Introduction

This chapter describes the VG330's bus architecture and the nature of bus operations. Memory cycles are discussed in Chapter 8, *Memory Controller Unit*.

The VG330 utilizes a single-bus architecture in which all external memory and I/O devices share a common address bus and data bus. The VG330 provides a unique set of control signals for each logical sub-bus such as main memory, Expansion (ISA), and PC Card.

Bus operations are controlled by the Bus Cycle Generator Unit, or BCG, which operates together with the MCU to control cycle activities for all system components.

6.1.1 Capabilities

- Bus Cycle Generator controls all timing
- VG330 automatically sizes data bus activity in hardware to match the size of the target device

6.2 System Memory Organization

This section discusses the nature of memory and I/O handling in a VG330 system.

6.2.1 Bus Architecture

In the VG330, all internal function modules are accessed using ISA bus timing. The BIU provides external devices, as are listed in Table 6-1, with cycle types and rates appropriate for them, and drives external ISA devices on the bus with ISA timing.

The VG330 dynamically reconfigures the address bus, A[23:0], and data bus, D[15:0], on each bus cycle to match the address range and format, data width, and cycle timing of the target I/O or memory device. Table 6-1 identifies these characteristics for the major device types supported. Figure 6-1 shows the major internal buses and their distribution to function modules, along with some of the major system signals.

Table 6-1. Handling of Memory and I/O Devices in the System

Device Type	Address Format	Address Range	Clock Source for Cycles
System DRAM	Multiplexed	16 Mbytes	CPU clock
System SRAM/PSRAM	Latched	16 Mbytes	CPU clock
System ROM0	Latched	16 Mbytes	CPU clock
System ROM1	Latched	16 Mbytes	CPU clock
Memory PC CARD Cards	Latched	64 Mbytes	ISA Expansion bus Clock
I/O PC CARD Card	Latched	64 Kbytes	ISA Expansion bus Clock
Expansion I/O	Latched	64 Kbytes	ISA Expansion bus Clock
Expansion Memory	Latched	1 Mbytes	ISA Expansion bus Clock

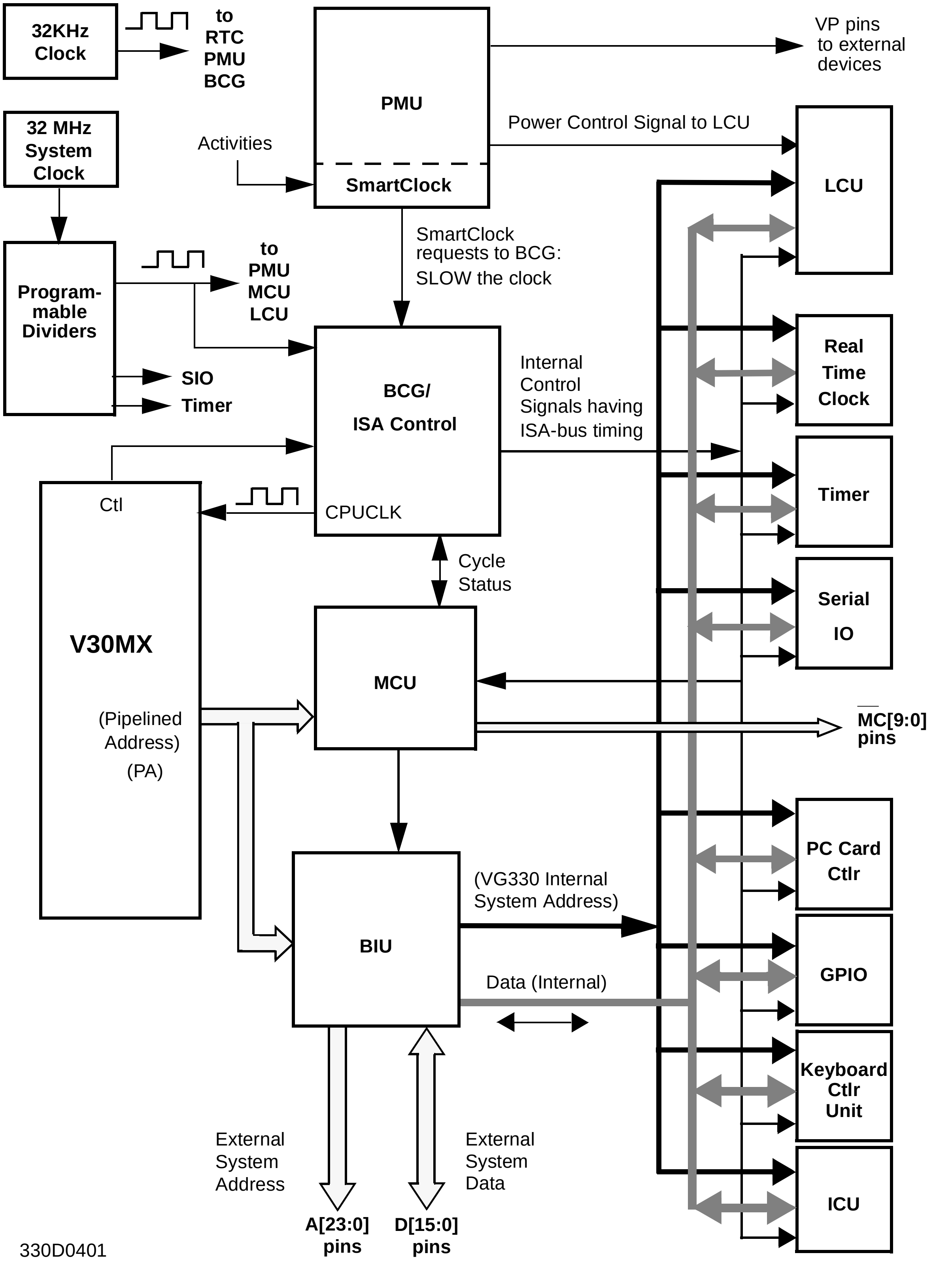


Figure 6-1 System Buses and System Signals

6.3 Address Bus Control

This section discusses VG330 address bus control for memory and for I/O.

For more information on addressing, see also:

- Mapping Registers on page 8-5.
- Register Descriptions in Chapter 16.

6.3.1 Addressing Architecture

The internal components of the VG330 that together provide address management are listed in Table 6-2:

Table 6-2. Address Management Components

Address Management Element	Function Block	Addressing Function
Address Source	V30MX	Provides CPU address output
	LCU	Provides video buffer address source, which is mapped to real memory by MCU
Address Mapping Capability	MCU	Provides EMS mapping registers to map output of CPU or LCU as needed to real memory
	PC Card Controller	Provides PC Card addressing space mapping
Address Selector	BIU	Selects among various address sources

The relationships of these components are shown in Figure 6-2 below:

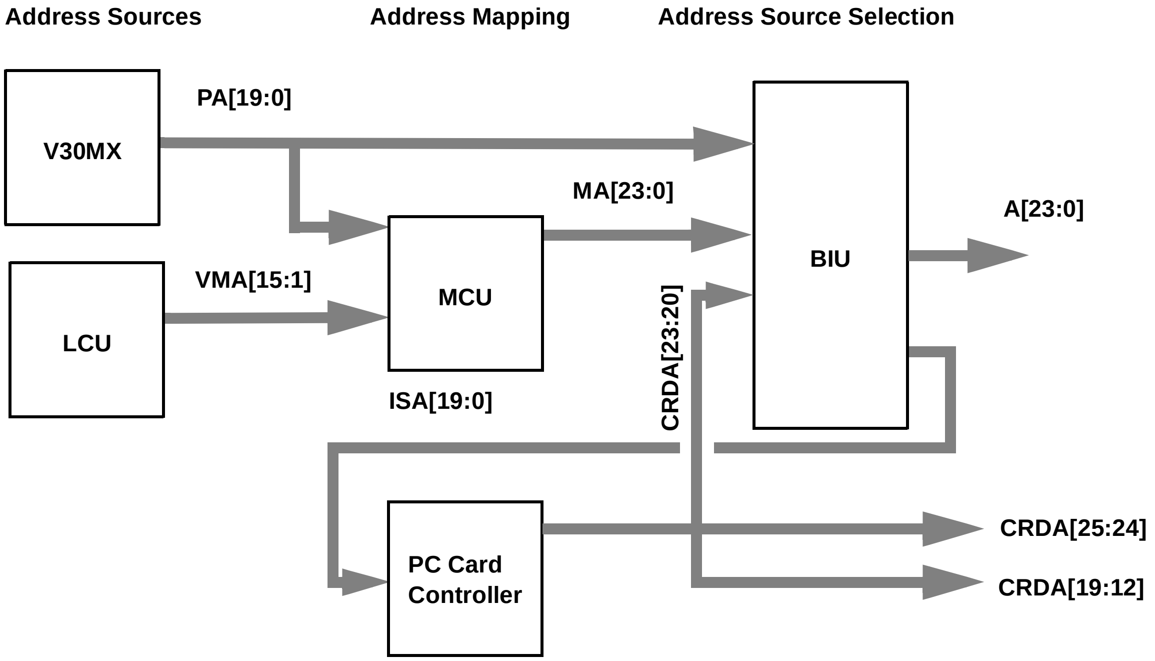


Figure 6-2 Address Management Components

As the diagram shows, the V30MX processor and the LCU are address sources, the MCU and the PC Card Controller provide address mapping functions, and the BIU is the address selector which determines which originator of an address will be used.

During memory cycles, both the MCU and the PC Card Controller monitor their respective address inputs and signal the BIU when a mapped address needs to be generated.

The MCU monitors the raw V30MX processor address, PA[19:0], and the PC Card Controller monitors the internal latched system address, ISA[19:0]. If neither the MCU nor the PC Card Controller claim the cycle, then an ISA cycle is generated by the BCG and the internal latched system address, ISA[19:0], is output by the BIU on the A[19:0] pins.

When both the MCU and the PC Card Controller are attempting to claim the cycle, priority is given to the MCU. An example of such a situation would be:

- Memory mapping is enabled for the memory region C0000H - C3FFFH and defined as either RAM, ROM0, or ROM1 type memory.
- A PC Card memory window is also enabled for the memory region C0000H - C3FFFH.

In this case, a memory cycle generated by the V30MX would be directed to RAM or ROM controlled by the MCU and a PC Card cycle inhibited.

6.3.2 Memory Address Mapping

Address mapping is provided only for memory devices. The following types of memory address mapping are supported by the VG330:

- LIM 4.0 type EMS address mapping for RAM and ROM cycles.
- BIOS ROM mapping for ROMCE0 cycles
- Shadow BIOS memory mapping
- Memory mapping for the display buffer
- PC Card memory mapping

LIM 4.0 EMS Mapping

EMS, also known as expanded memory, permits very large memory subsystems to be supported by processors which have limited physical addressing capabilities. This is accomplished using a technique called paging. In paging, a region of the processor’s address space is defined as a “window” into a larger physical memory space. During accesses to these regions, the processor’s address is translated, or “mapped”, into a physical memory location. The LIM 4.0 EMS mapping logic in the VG330 is a superset of the LIM 4.0 specification. The VG330 provides additional capabilities by allowing not only a physical address to be specified, but also a memory device type, such as RAM, ROM0, or ROM1.

The VG330 implements 16 mapping register pairs, each capable of addressing 16 MBytes of RAM or 32 MBytes of ROM. Each mapping register pair in turn controls one 16 KByte memory window which may be located in the V30MX address space between A0000H and EFFFFH.

A particular mapping register pair is selected for programming by first writing the address of the 16 KByte memory window to be controlled to the Mapper Address register at I/O address 0006CH. Then, the physical memory page and memory type to be mapped into the selected 16 KByte window is programmed by writing the Mapper Low Byte and Map High Byte registers at I/O addresses 06EH and 06FH respectively.

In the memory map in Figure 6-3, the relationship between the V30MX address space and the physical memory address space has been shown. The physical memory space is divided into 16 KByte pages. The first 40 of these pages are reserved for DOS, drivers, and application programs and are directly mapped to the lower 640 KBytes of the V30MX address space.

In this particular example, the LCD Display Buffer Area, addressed by the V30MX in the B8000H - BFFFFH region, has been mapped into the upper two 16 KByte pages of the physical memory space. Finally, four EMS windows have been opened in the V30MX A0000H - AFFFFH address space to map physical memory pages into these locations.

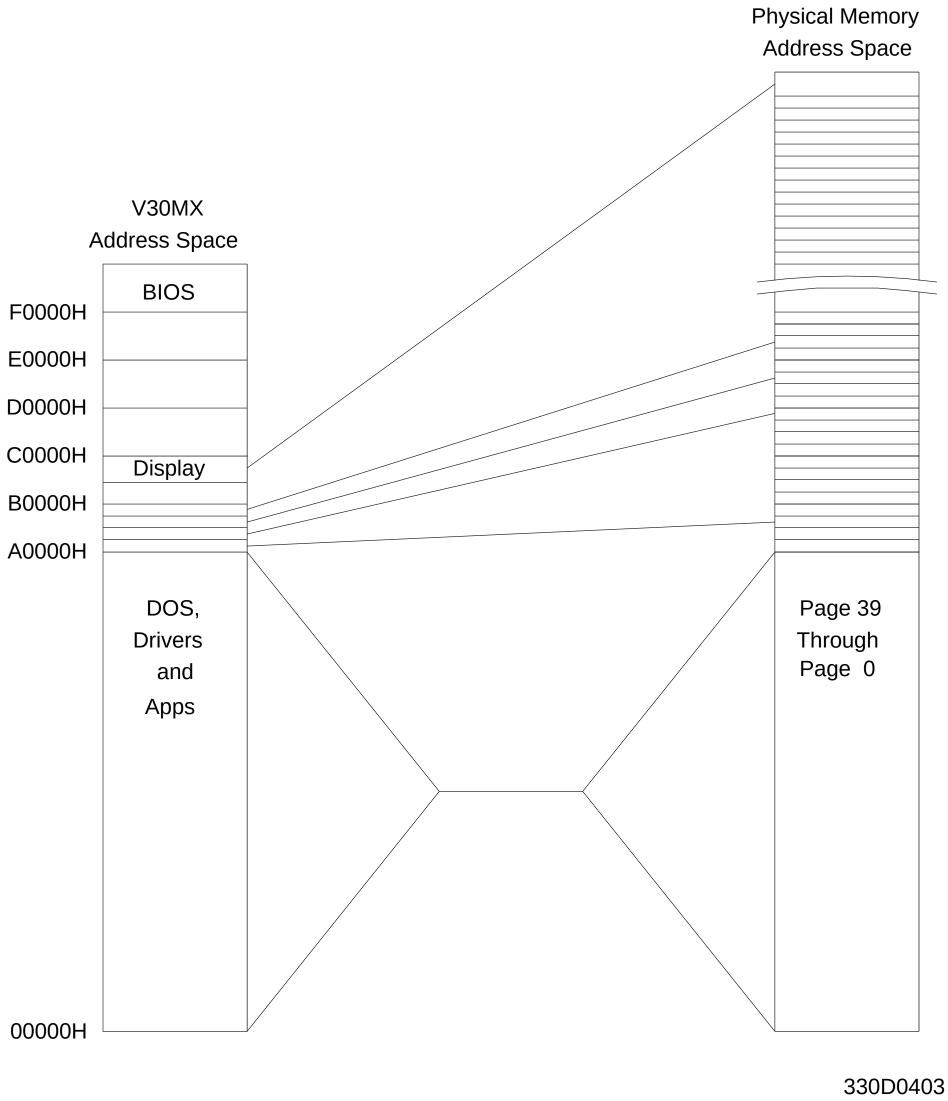


Figure 6-3 Memory Mapping Example

BIOS ROM Mapping for ROMCE0 Cycles

The VG330 provides a form of address mapping during accesses to the BIOS in the V30MX address space F0000H - FFFFFH when the BIOS resides in ROM. During these types of cycles, the VG330 drives the A[23:16] address pins low to force the access to occur in the lowest 64 KByte portion of any size external ROM device. This simplifies the ROM build process when BIOS and applications both reside in the physical ROM or ROM array controlled by the ROMCE0 pin.

Shadow BIOS Memory Mapping

See discussion in Chapter 8, *Memory Controller Unit*, for details.

Address Generation for DRAM

When system RAM is implemented with DRAM and register-configured appropriately, the VG330 generates a multiplexed row/column address on the A[10:0] pins during DRAM accesses. The type of DRAM used determines the format of the address generated and which of the A[10:0] pins are required to interface to the DRAM. Table 6-3 identifies the address bits multiplexed onto the A[10:0] pins for each DRAM type.

Table 6-3. Address Bits Output to DRAM by VG330

	DRAM TYPE									
	256K x 16		**512K x 8**		**1M x 4 1M x 16**		**2M x 8**		**4M x 4**	
Address Pin	**Row**	**Col**	**Row**	**Col**	**Row**	**Col**	**Row**	**Col**	**Row**	**Col**
A0	10	1	10	1	10	1	10	1	10	1
A1	11	2	11	2	11	2	11	2	11	2
A2	12	3	12	3	12	3	12	3	12	3
A3	13	4	13	4	13	4	13	4	13	4
A4	14	5	14	5	14	5	14	5	14	5
A5	15	6	15	6	15	6	15	6	15	6
A6	16	7	16	7	16	7	16	7	16	7
A7	17	8	17	8	17	8	17	8	17	8
A8	18	9	18	9	18	9	18	9	18	9
A9	-	-	19	-	19	20	19	20	19	20
A10	-	-	-	-	-	-	21	-	21	22

6.3.3 High Address Bits Handling Option

The VG330 provides a means of minimizing unneeded transitions on high order address lines, which can minimize power consumption on those pins.

The behavior of the upper address pins, A[23:20], is configured on an individual pin basis. There are three enable bits per pin that allow each of the A[23:20] pins to be enabled for either RAM, ROM0, or ROM1 cycles. (BIOS memory initialization and start-up code are contained in ROM0.)

These enable bits are located in the Address Pin Configuration Registers at Index 14H (for A23 and A22), 15H (for A21 and A20), and 16H (for A19 and certain other address lines). When an address pin is enabled for a particular memory type, that address pin is driven by the address specified in the memory mapping registers.

If the address pin has been set to be disabled for accesses to a particular memory type, when that type of memory is accessed by the system, that address pin output is latched and held at the previous value that was driven on the bus. In this way, unneeded transitions are avoided, saving power in the driver.

The Address Pin Configuration Register at 16H also permits control of the A[19:12] pins of the address bus. During I/O cycles, A[19:16] pins may be disabled causing them to be driven with the previous address. During RAM cycles, when system memory is DRAM, the A[19:12] pins may also be disabled. For more information, refer to the register description in Chapter 16. See also: discussion of *Bus Latching Mode* on page 11 of this chapter.

6.3.4 Display Buffer Memory Mapping

The VG330 provides dedicated logic for mapping the Display Buffer Area into the V30MX address space. The LCD T3 Register’s VIDMODE bit determines where in the V30MX address space the Display Buffer Area window:

Table 6-4. Display Buffer Mapping

VIDMODE	Address Range	Size
0	B8000H - BFFFFH	32 KBytes
1	A0000H - AFFFFH	64 KBytes

The VG330 supports two Display Buffer Areas, a primary Display Buffer Area and an alternate Display Buffer Area. Both Display Buffer Areas always reside in the last memory bank. The bank information is programmed through the BANK[2:0] bits of the Memory Control Register.

The primary Display Buffer Area resides in the upper-most 32 KBytes or 64 KBytes of the last memory bank, depending on the state of the VIDMODE bit. All accesses to the Display Buffer Area through the B8000H - BFFFFH or A0000H - AFFFFH windows always access the primary Display Buffer Area.

However, the VG330 can be configured to allow LCU display refresh cycles to fetch data from either the primary or alternate Display Buffer Areas. This behavior is enabled by programming the Alternate Display Buffer Start Address Register.

Bits D[6:0] of the Alternate Display Buffer Start Address Register are used to specify the starting address in the last memory bank where the alternate Display Buffer Area will reside. Bit D[7] of this register enables the LCU to fetch data to be displayed on the LCD panel from the alternate Display Buffer Area.

The alternate Display Buffer Area is intended to be used for displaying system status messages or system setup type screens without affecting applications which are writing the default Display Buffer Area. Assume, for example, that a system supports a setup screen for specifying power management settings, serial I/O port assignments, date and time settings, and so forth, and that and this setup screen is called using some special key combination, such as <CTL> <ALT> <ENTER>. When such a key combination is detected by the system firmware, the alternate Display Buffer Area could be used to display the setup screen as follows:

- System firmware opens an EMS window and writes the setup screen display image to some location in the last memory bank.
- The Alternate Display Buffer Start Address Register is then programmed to point to the physical memory location where the setup screen display image resides and sets the ALTDBREN bit high.
- The LCU then begins fetching display data from the alternate Display Buffer Area and

outputs this data to the LCD panel. Any applications running in the background while the setup screen is being displayed will continue to update the primary Display Buffer Area at the top of memory.

- Once changes to the setup information have been made, the system firmware resets the ALTDBREN bit low and the LCU resumes fetching display data from the primary Display Buffer Area.

Display Buffer Mapping for Small Memory Configurations

The VG330 provides an option, controlled by the Top of Memory Register, to support display buffer mapping for memory configurations of less than 640 KBytes. In these types of configurations it is sometimes necessary to protect the RAM allocated to the Display Buffer Area from being overwritten by DOS applications. The Top of Memory Register permits the starting address of the Display Buffer Area to be specified within the 640 KByte address space typically reserved for DOS and applications.

Once the Top of Memory register has been programmed, access to memory above this setting is inhibited except through the Display Buffer Area window at either B8000H - BFFFFH or A0000H - AFFFFH.

The Top of Memory register may also be used to define a 16 KByte Display Buffer Area in order to free an additional 16 KBytes for DOS and application use in small memory configurations. This is accomplished by setting the Top of Memory Register's BUF16K bit high.

LCD Controller Unit Display Refresh Addressing

In the VG330 architecture, the Display Buffer Area resides in the top 64, 32, or 16 KBytes of system RAM depending on the display mode and the settings of the Top of Memory and Alternate Display Buffer Start Address registers. These registers are described in Chapter 16.

The LCU generates display refresh cycles by becoming a bus master and then generating cycles to refill its internal line buffer. During display refresh cycles, the MCU drives the upper address pins, A[23:16], high to select the top of physical memory and the LCU generates a 15 bit address offset, VMA[15:1], into the uppermost memory bank.

6.3.5 PC Card Memory Mapping

Refer to Chapter 13, *PC Card/ExCA Controller*, for a description of PC Card memory mapping and CRDA[25:24] and CRDA[19:12] pin functions.

6.3.6 V30MX I/O Addressing

The VG330 does not provide address mapping for I/O cycles. For these cycles, the V30MX processor address, PA[15:0], is latched and output on the A[15:0] pins.

The remaining VG330 address pins, A[23:16], are typically driven low during I/O cycles. However, if Bus Latching Mode is enabled, the state of these pins prior to the I/O cycle may be latched and held during the I/O cycle to reduce power. Refer to *Bus-Related Power Saving Features* on page 6-11, which describes Bus Latching Mode, for details on this behavior.

6.4 Data Bus Control

6.4.1 Data Bus Sizing

In the same manner that the VG330 address lines are handled using Vadem’s Single Bus Architecture, all external memory and I/O devices connect to a single set of data pins, D[15:0]. Timing and data sizing of the D[15:0] pins are dynamically configured during each cycle based on the type of cycle and the data width of the target device involved in a bus transfer. The data width of a transfer target is selected either:

- by VG330 register bits, as in the case of system ROM1, and PC CARD memory addressed by the internal PC CARD controller, or
- by VG330 input pins such as $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ for Expansion bus devices, WP for PC CARD I/O, and the ROM8/$\overline{\text{16}}$ pin for ROM0 cycles.

Data steering is based on cycle type and target data width as follows:

Table 6-5. Data Steering

Cycle Type	Target Data Width	Data Path
Even Byte	8 or 16 bits	D[7:0]
Odd Byte	16 bit	D[15:8]
Odd Byte	8 bit	D[7:0]
Word	16 bit	D[15:0]
Word	8 bit	Two transfers on D[7:0]

Data Width

The data width of the target device is determined as shown in Table 6-6. (The target of expansion memory and/or expansion I/O cycles are assumed to be 8 bits if GPIO pins have not been allocated to provide $\overline{\text{MEMCS16}}$ and/or $\overline{\text{IOCS16}}$.)

Table 6-6. Data Width Selection for Target Device Types

Target Device	Data Width Selector
System RAM	Fixed at 16 bits
ROM0	ROM8/ $\overline{\text{16}}$ input pin
ROM1	Memory Control 2 Register - ROM1SIZ bit
Expansion Memory	Designer must use a GPIO pin defined as $\overline{\text{MEMCS16}}$
Expansion I/O	Designer must use a GPIO pin defined as $\overline{\text{IOCS16}}$
PC Card Memory	PC Card Memory Data Size Register - DSIZ bit
PC Card I/O	PC Card I/O Control Register - IODSIZ bit or WP pin
Programmable Memory CS	Designer must use either the PCS Mode Register - DSIZE bit, or allocate and define a GPIO pin as $\overline{\text{MEMCS16}}$
Programmable I/O CS	Designer must use either the PCS Mode Register - DSIZE bit or GPIO pin defined as $\overline{\text{IOCS16}}$

6.5 Control Signals

6.5.1 RAM and ROM Control

System RAM and ROM are controlled by outputs from the VG330 memory controller. Refer to Chapter 8, *Memory Controller Unit*, for details.

6.5.2 ISA Bus Signals

Expansion bus I/O and memory are controlled by the $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ signals.

$\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ are never asserted during accesses to System RAM. However $\overline{\text{SMRD}}$ may be configured to drive the $\overline{\text{OE}}$ pins of ROM devices controlled by $\overline{\text{ROMCE0}}$ and $\overline{\text{ROMCE1}}$, and both $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ may be active for PC Card memory cycles.

In some cases, it may be necessary to provide separate $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ strobes to Expansion bus memory devices to prevent these devices from misinterpreting ROM or PC Card memory addresses. The VG330 allows PC Card memory strobes to be output on the GPIO pins.

6.5.3 PC Card Control

PC memory Cards may be controlled by Expansion bus $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ signals. See discussion of *Command Signal Handling* on page 13-4.

6.6 Bus-Related Power Saving Features

This section discusses options for controlling general bus activity, and data bus activity in ways that can save system power.

All of the VG330 output pins are 3.3v and driven to CMOS levels.

6.6.1 General Bus Activity Control Options

The VG330 provides two options for reducing overall system power consumption related to activity on buses in general. These are described in this section. Control of these options is shown in Table 6-7.

Bus Inhibit Mode and Bus Latching Mode are used to limit bus interface activity on the A[23:0], D[15:0], and $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ pins.

Bus Inhibit Mode

Causes the VG330 D[15:0], $\overline{\text{SIORD}}$, and $\overline{\text{SIOWR}}$ pins to remain inactive during accesses to internal VG330 I/O peripherals. When Bus Inhibit Mode is enabled, the $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ pins are disabled or inhibited during I/O access to VG330 internal subsystems or registers.

Bus Latching Mode

Enables only those A[23:0] pins required to select an external target device to drive valid address.

Those A[23:0] address bits which are not required for a particular target device are driven with the previous bus cycle address.

Table 6-7. Bus Activity Control Options

Bus Inhibit Mode	Controlled by bit 2 of the BCG Mode Register at Index 01H.
Bus Latching Mode	Controlled by bit 3 of the BCG Mode Register at Index 01H.

6.6.2 Data Bus Activity Control Options

Data Hold and Clamping

Normally, the D[15:0] pins of the VG330 are configured as inputs and are only driven by the VG330 during write cycles. The VG330 supports two options for minimizing power consumption of external devices connected to the D[15:0] bus.

Data Hold Mode

The VG330 may be configured to drive the D[15:0] pins with the last value read or written to the bus. This is referred to as Data Hold mode.

Data Hold mode prevents the input buffers of devices connected to D[15:0] from floating, thereby reducing input oscillations and the resulting increase in power consumption.

During reads from or writes to devices connected to the D[15:0] bus, the data value is latched at the end of the data transfer cycle and is driven back onto the bus by the VG330. The VG330 continues to drive D[15:0] with this data until the next read or write cycle involving an external device connected to D[15:0].

Data Clamping

The other data bus power management option supported by the VG330 is Data Clamping during power management stop clock modes, such as static DOZE or SLEEP, or stop clock HALT.

During these states, the D[15:0] pins are driven low by the VG330 and remain low-driven until the power management state has been exited.

6.7 Related Registers

Register	Address
BCG Mode Register	Index 01H

7 ISA Bus Interface

7.1 Introduction

The VG330 includes bus control logic capable of generating 8- and 16-bit cycles similar to PC-AT bus cycles. This chapter describes the VG330's ISA characteristics, and ISA Bus interfacing with the VG330.

7.1.1 ISA Support

The VG330 supports ISA subject to the following considerations:

- The VG330's BCG/ISA Controller module generates timing compatible with most ISA peripherals.
- The VG330 is not intended to support a full conventional PC, such as a motherboard having ISA slots, and does not support a full ISA bus interface nor is it intended to drive a standard ISA connector. The VG330's ISA control is intended to support only "on-board" peripherals in a small system such as a handheld device.

7.2 Architecture

Figure 7-1 shows internal elements together with pins dedicated to ISA signals on the VG330:

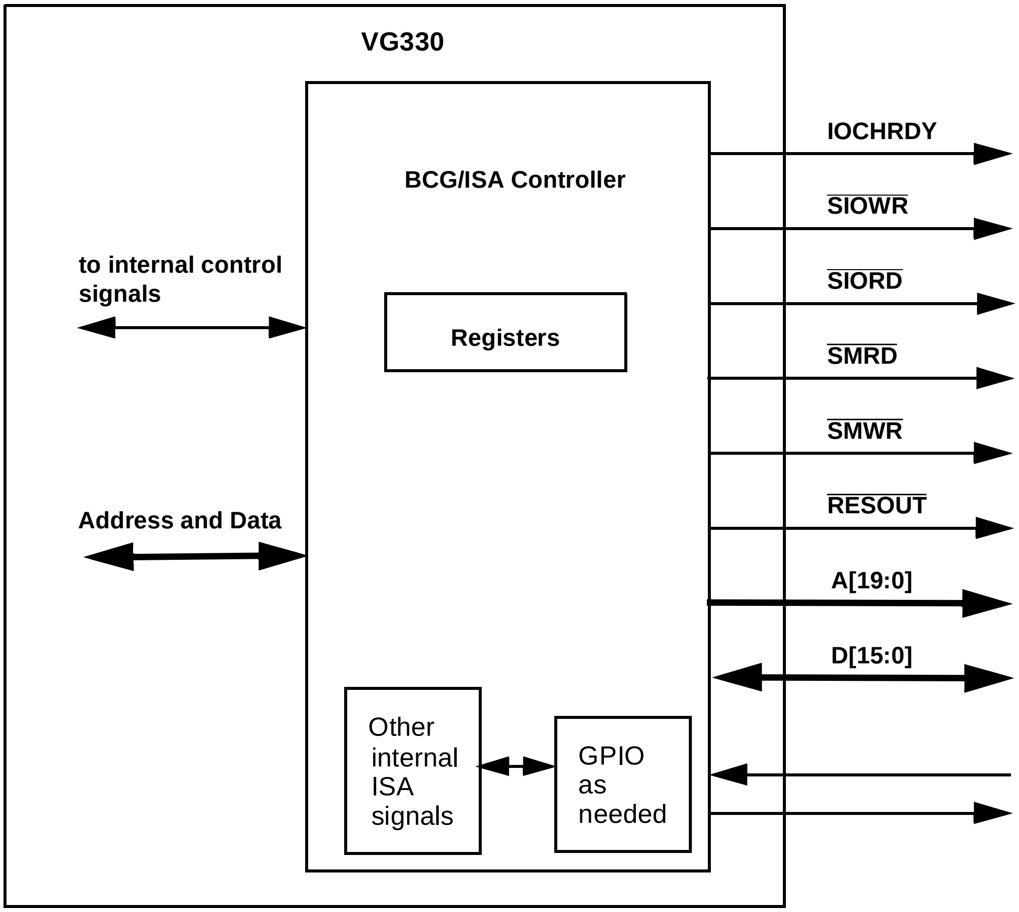


Figure 7-1 VG330 ISA Inputs and Outputs

7.3 ISA Bus Pins and Signals

There are three classes of ISA signals that are discussed here:

- ISA signals for which a dedicated pin is provided on the VG330
- ISA signals available if they are routed through GPIO pins dedicated to that purpose
- ISA signals not supported by the VG330

ISA Signals Provided Through Dedicated Pins

A subset of the ISA signals are supported directly through dedicated VG330 pins. These signals and pins are listed in Table 7-1.

Table 7-1. ISA Signals Provided on VG330 Dedicated Pins

ISA Signal[a]	**VG330 Pin Supporting Signal**	**Function**
I/OCHRDY	IOCHRDY	**ISA bus I/O Channel Ready signal**. To extend the ISA cycle, an ISA device must drive IOCHRDY low.
-IOR	$\overline{\text{SIORD}}$	**ISA I/O Read command strobe.** The selected ISA I/O device drives data onto the bus while this command strobe is low.
-IOW	$\overline{\text{SIOWR}}$	**ISA I/O Write command strobe.** The selected ISA I/O device loads data driven by the VG330 while this command strobe is low.
RESET DRV	$\overline{\text{RESOUT}}$ (Note that this signal must be inverted.)	**ISA Reset signal.**
SA[19:0]	A[19:0]	**ISA Address.**
SD[15:0]	D[15:0]	**ISA Data.**
-SMEMR	$\overline{\text{SMRD}}$	**ISA Memory Read command strobe.** The selected ISA Memory device drives data onto the bus while the VG330 holds this command strobe low.
-SMEMW	$\overline{\text{SMWR}}$	**ISA Memory Write command strobe.** The selected ISA Memory device loads data driven by the VG330 while this command strobe is low.

[a] A minus prefix (-) indicates an active-low ISA signal.

ISA Signals Available Through GPIO Pins

Several other ISA functions are only available through GPIO configuration options. Table 7-2 of this chapter lists these ISA signals and the associated GPIO pins which support them. For additional information, refer to Chapter 12, *GPIO*.

Table 7-2. ISA Signals Available Through GPIO Pins

ISA Signal[a]	Type[b]	Function	GPIO Pins Capable of Supporting the Signal
CLK	I	**ISA bus clock.**	GPIOC7, GPIOB7, GPIOA7, GPIOA3
-IOCS16	O	**I/O Chip Select 16.** Used to signal I/O device supporting data transfers on SD[15:8]. This optional input must be driven low by an ISA I/O device needing to signal that it can accept data transfers on D[15:8].	GPIOC4, GPIOB1, GPIOA5, GPIOA1
IRQ15, IRQ7	O	**Interrupt request.**	GPIOC1, GPIOB1, GPIOA2
IRQ14, IRQ6	O	**Interrupt request.**	GPIOC2, GPIOB2, GPIOA3
IRQ13, IRQ5	O	**Interrupt request.**	GPIOC3, GPIOB3, GPIOA4
IRQ12, IRQ4	O	**Interrupt request.**	GPIOC4, GPIOB4, GPIOA5
IRQ11, IRQ3	O	**Interrupt request.**	GPIOC5, GPIOB5, GPIOA6
IRQ10	O	**Interrupt request.**	GPIOC6, GPIOB6, GPIOA7
IRQ9, IRQ1	O	**Interrupt request.**	GPIOC7, GPIOB7, GPIOB0
-MEMCS16	O	**Memory Chip Select 16.** Used to signal that a memory device supports data transfers on SD[15:8]	GPIOC3, GPIOB0, GPIOA4, GPIOA0
SBHE	I	**Byte High Enable.** Indicates SD[15:8] contains valid data.	GPIOC6, GPIOB6, GPIOA6, GPIOA2

a. A minus prefix (-) indicates an active-low ISA signal.

b. The Type column in the table indicates the signal source, where O represents an output from the ISA peripheral and I is an input to the ISA peripheral.

ISA Signals Not Supported by the VG330

Table 7-3 describes the unsupported ISA bus signals together with recommendations for external control connections:

Table 7-3. ISA Signals Not Supported by the VG330

ISA Signal[a]	Source Type[b]	Function	Recommended Connection
-0WS	O	**Zero Wait State.** Driven low by peripheral to request 0 wait state memory cycle.	Open
AEN	I	**DMA Address Enable.**	Tie low at peripheral.
ALE	I	**Address Latch Enable.** Indicates a valid address is driven on bus.	Tie high at peripheral.
-DACK[7:0]	I	**DMA Acknowledge.**	Tie high at peripheral.
DRQ[7:1]	O	**DMA Request.**	Open
-IOCHK	O	**Parity error for ISA bus.** Typically used to generate NMI.	Open
LA[23:17]	I	**Latchable Address.** Used to generate 0WS signal.	Connect LA[19:17] to A[19:17] and tie LA[23:20] low at peripheral.
-MASTER	O	**Request to become ISA bus master.**	Open
-MEMR	I	**Memory Read.** For entire 16 MByte address space.	Connect to $\overline{\text{SMRD}}$.
-MEMW	I	**Memory Write.** For entire 16 MByte address space.	Connect to $\overline{\text{SMWR}}$.
-REFRESH	I	**Memory refresh cycle**.	Tie high at peripheral.
T/C	I	**Terminal Count for DMA cycles.**	Tie low at peripheral.

a. A minus prefix (-) indicates an active-low ISA signal.

b. The Type column in the table indicates the signal source, where O represents an output- from the ISA peripheral and I is an input to the ISA peripheral.

7.4 System Design Considerations

RAM and ROM

System RAM and ROM are controlled by outputs from the VG330 MCU. If system RAM or ROM is being addressed, the VG330 executes an appropriate memory cycle type. However, if the object being addressed is not system RAM or ROM, the VG330 executes an ISA cycle.

$\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ are never asserted during accesses to System RAM. However, $\overline{\text{SMRD}}$ may be configured to drive the $\overline{\text{OE}}$ pins of ROM devices controlled by $\overline{\text{ROMCE0}}$ and $\overline{\text{ROMCE1}}$, and both $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ may be active for PC Card memory cycles.

In some cases, it may be necessary to provide separate $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ strobes to Expansion bus memory devices to prevent these devices from misinterpreting ROM or PC Card memory addresses. The VG330 allows PC Card memory strobes to be output on the GPIO pins.

PC Memory Cards

PC Card memory cards can be controlled by Expansion bus $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ signals. In this configuration, the Expansion bus command strobes must be buffered to support hot insertion and power management of the PC Card slot.

Optionally, GPIO pins may be configured to directly drive the PC Card slot with memory command strobes. These command strobes do not require external buffering and are driven tri-state when the PC Card slot is unpowered.

Expansion bus I/O and Memory

Expansion bus I/O and memory are controlled by the $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ signals.

Interfacing ISA Peripherals to the VG330

ISA devices are interfaced to the ISA Controller through a combination of dedicated pins on the VG330 and certain signals that must be routed through GPIO pins that can be dedicated to carrying ISA signals.

Table 7-4 lists all relevant pins and signals.

16 bit ISA Bus Support

In order to enable 16-bit I/O cycles, one of the GPIO pins must be configured as $\overline{\text{IOCS16}}$.

Likewise, to support 16-bit Expansion memory, the $\overline{\text{MEMCS16}}$ signal must be enabled on one of the GPIO pins.

If the ISA peripheral does not return $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$, thus indicating it is an 8-bit device, then the VG330 automatically performs two sequential 8-bit transfers when a 16-bit access is attempted by the bus master. This is known as dynamic bus sizing.

Additionally, the GPIO pins may be configured to output the byte high enable signal, $\overline{\text{BHE}}$.

During external I/O or memory cycles, the VG330 will generate 16 bit cycles if the selected device responds with either $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$.

The ISA bus clock, SYSCLK, may also be output on the GPIO pins. 16 bit ISA bus support is available in each of the GPIO pin groups.

SIORD/SIOWR Operation During Bus Inhibit Mode

For information on this behavior, refer to heading *General Bus Activity Control Options* on page 6-11.

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Table 7-4. VG330 Pins Used in ISA Interfacing

VG330 Signal	Type	Signal / Pin Assignment	Function of Signal
A[19:0]	O	Dedicated	Address bus signals
D[15:0]	I/O	Dedicated	Data bus signals
$\overline{SIORD}$	O	Dedicated	ISA I/O Read command strobe.
$\overline{SIOWR}$	O	Dedicated	ISA I/O Write command strobe.
$\overline{SMRD}$	O	Dedicated	ISA Memory Read command strobe.
$\overline{SMWR}$	O	Dedicated	ISA Memory Write command strobe.
IOCHRDY	I	Dedicated	ISA bus I/O Channel Ready signal.
$\overline{RESOUT}$	O	Dedicated	Reset signal.
$\overline{BHE}$	O	on GPIO pin[a]	Byte High Enable.
$\overline{IOCS16}$	I		I/O Chip Select 16. This optional input must be driven low by an ISA I/O device needing to signal that it can accept data transfers on D[15:8].
$\overline{MEMCS16}$	I		Memory Chip Select 16. This optional input is used to signal that a memory device supports data transfers on SD[15:8]

[a] Neither $\overline{IOCS16}$, $\overline{MEMCS16}$, nor $\overline{BHE}$ have dedicated pins on the VG330; to obtain these signals requires routing through a GPIO pin

7.5 ISA Cycle Control

The ISA Controller translates processor cycles timed from CPUCLK, an internal CPU clock signal, into ISA cycles timed from the ISA Expansion bus clock, SYSCLK.

The VG330 provides significant flexibility in the ways by which ISA cycles are generated. Configuration registers permit programming of the ISA bus clock frequency, clocking mode, ISA address setup, and minimum command strobe pulse widths.

This section discusses these configuration items.

7.5.1 SYSCLK Generation

Expansion I/O and memory cycles are timed from SYSCLK, which is derived from the processor clock CPUCLK. The VG330 supports SYSCLK frequencies that are 1/2, 1/3, and 1/4 the processor clock rate.

Divider Settings for SYSCLK

SYSCLK is the timing source for all ISA cycles. It is derived by dividing the full speed processor clock frequency by a factor selected through the BCG Mode Register at VG330 index address 01H as follows:

D[6:5] **OSCDIV[1:0]**

Divisor for generating CPUCLK and Video Clock from input oscillator. These bits select the divisor applied to the input clock frequency generated by either the crystal on pins X1/X2 or external oscillator on X1 :

OSCDIV1	OSCDIV0	CPUCLK and Video Clock Divisor
0	0	X1 frequency
0	1	X1 frequency divided by 2 (default)
1	0	X1 frequency divided by 3
1	1	X1 frequency divided by 4

D[1:0] **SDIV[1:0]**

ISA bus clock divisor select. These bits select the divisor applied to the CPUCLK frequency for generating the ISA bus clock, SYSCLK.

SDIV1	SDIV0	SYSCLK Divisor
0	0	CPUCLK / 4
0	1	CPUCLK / 3
1	0	CPUCLK / 2 (default)
1	1	Reserved setting

For example: if the VG330 X1 pin is driven by a 32 MHz clock and the OSCDIV[1:0] bits are cleared to select a 32 MHz CPUCLK frequency, clearing the SDIV[1:0] bits will select an 8 MHz SYSCLK frequency.

7.5.2 Selecting Clocking Mode

In addition to specifing the SYSCLK frequency, a clocking mode must also be selected for SYSCLK. Clocking modes are programmed through bits D[7:6] of the Expansion Bus Mode Register at VG330 index address 034H. A portion of the register description from Chapter 16, *Registers* is reproduced here for convenience:

SCLKMD[1:0] - These bits determine the operating mode of SYSCLK. They are decoded as follows:

SCLKMD1	SCLKMD0	SYSCLK Mode
0	0	Clock Stop Mode (Default)
0	1	Clock Sync Mode
1	0	Clock Stretch Mode
1	1	Reserved Setting

Clock Stop Mode

Clock Stop Mode provides the lowest power consumption and is intended for systems which do not require that SYSCLK run continuously. In this mode, SYSCLK is normally stopped and starts running only when an ISA bus cycle needs to be generated. At the completion of the ISA bus cycle SYSCLK is again stopped. The timing diagram below illustrates a typical ISA cycle with Clock Stop Mode active.

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Divide by 4 Mode - 0 Wait State ISA Cycle w/Clock Stop

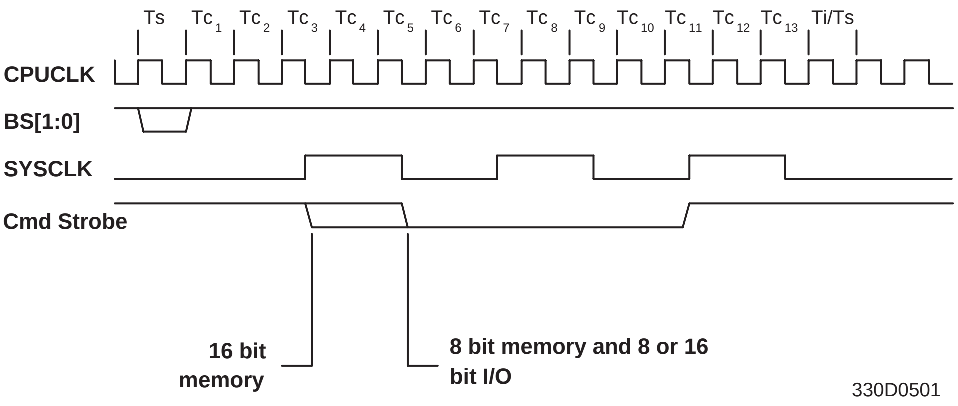

Figure 7-2 Clock Stop Mode

Clock Sync Mode

Clock Sync Mode permits SYSCLK to run continuously and the start of each ISA bus cycle is synchronized to the proper SYSCLK phase. Because ISA cycles must be synchronized, the start of an ISA bus cycle may be delayed by up to 4 processor clock cycles when programmed in this mode.

Clock Stretch Mode

Clock Stretch Mode also permits SYSCLK to run continuously. However, when an Expansion bus cycle is requested, SYSCLK is stretched high or low to synchronize it with the start of the Expansion bus cycle.

Both Clock Sync Mode and Clock Stretch Mode allow SYSCLK to run continuously.

7.5.3 ISA Timing Options

All ISA timing is controlled by three register programmable options. These options are listed at the right and shown in Figure 7-3 :

- Lead Off Delay, which specifies address setup to assertion of an ISA command strobe.
- SYSCLK frequency.
- Wait States, which specifies the minimum width of an ISA command strobe.

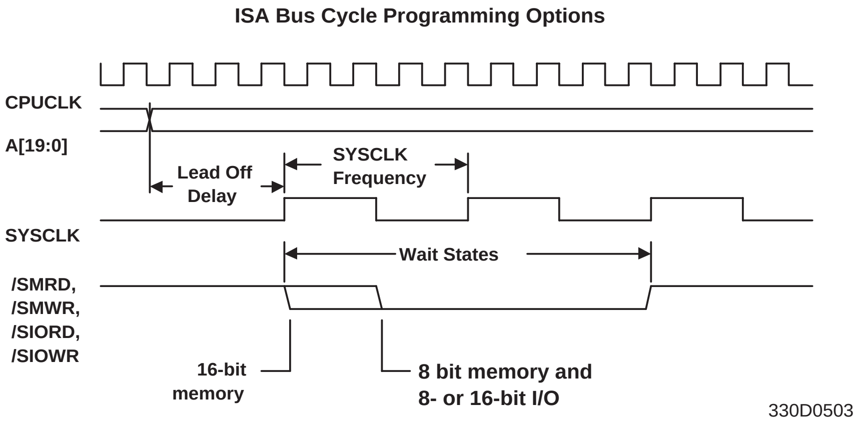

Figure 7-3 ISA Bus Cycle Programming Options

Lead Off Delay

The VG330 inserts a minimum delay between address valid and the assertion of one of the ISA command strobes, $\overline{\text{SMRD}}$, $\overline{\text{SMWR}}$, $\overline{\text{SIORD}}$, or $\overline{\text{SIOWR}}$. This minimum delay varies depending upon the SYSCLK divisor, clocking mode, and type of cycle as follows:

Table 7-5. Lead Off Delay

SYSCLK Frequency	SYSCLK Operating Mode	Minimum Delay for 16-bit Memory Cycles	Minimum Delay for All Other Cycles
1/4 CPUCLK	Clock Stop	3 CPUCLK cycles	5 CPUCLK cycles
	Clock Sync	2 to 5 CPUCLK cycles	3 to 6 CPUCLK cycles
	Clock Stretch	2 to 3 CPUCLK cycles	4 to 5 CPUCLK cycles
1/3 CPUCLK	Clock Stop	3 CPUCLK cycles	4 CPUCLK cycles
	Clock Sync	2 to 4 CPUCLK cycles	3 to 5 CPUCLK cycles
	Clock Stretch	2 to 3 CPUCLK cycles	3 to 4 CPUCLK cycles
1/2 CPUCLK	Clock Stop	2 CPUCLK cycles	3 CPUCLK cycles
	Clock Sync	2 to 3 CPUCLK cycles	3 to 4 CPUCLK cycles
	Clock Stretch	2 CPUCLK cycles	3 CPUCLK cycles

Note: The variations in minimum delays above are caused by synchronizing start of ISA cycle to proper phase of SYSCLK.

If additional address setup is required for external ISA devices, lead off delay may be increased through the Expansion Bus Mode Register LODLY[1:0] bits as follows:

LODLY 1	LODLY 0	Expansion Bus Additional Lead Off Delay
0	0	None
0	1	1 CPUCLK cycle
1	0	2 CPUCLK cycles
1	1	3 CPUCLK cycles

SYSCLK Frequency

Programming the SYSCLK frequency was previously discussed under the heading *SYSCLK Generation* on page 7-8 of this chapter.

SYSCLK frequency determines the minimum ISA command strobe pulse width. Command pulse widths are calculated as follows:

Pulse Width for 16-bit Memory Cycles

$$\mathbf{= (2 * t_{SYSCLK}) + (\mathit{W} * t_{SYSCLK})}$$

Pulse Width for All Other Cycles

$$= \mathbf{t_{SYSCLK} + t_{SYSLOW} + (\mathit{W} * t_{SYSCLK})}$$

Where

$\mathbf{t_{SYSCLK}}$ = SYSCLK period

$\mathbf{t_{SYSLOW}}$ = SYSCLK low time (1/2 SYSCLK or 2/3 SYSCLK period depending on SYSCLK divisor)

W = Register-programmable Wait States

Wait States

The VG330 provides independent ISA Wait State control for:

- Expansion 8 or 16 bit I/O cycles
- Memory cycles to 8-bit devices
- 16-bit memory cycles to 16-bit devices.

Each of these may be independently configured through the Expansion Bus I/O Wait State Control register at VG330 index address 35H and the Expansion Bus Memory Wait State Control register at VG330 index address 36H.

Wait state settings of zero to 7 SYSCLK cycles are supported. A zero wait state Expansion bus I/O or memory cycle will complete in 3 SYSCLK cycles.

The register-programmable wait states define the minimum pulse width driven on the $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, or $\overline{\text{SMWR}}$ pins. Additional wait states may also be inserted into the ISA cycle using the IOCHRDY pin.

It is important to note that the IOCHRDY pin only effects ISA cycles. The IOCHRDY pin is ignored for memory cycles which access system RAM controlled by the $\overline{\text{MC}}$[9:0] pins or system ROM controlled by the $\overline{\text{ROMCE1}}$ or $\overline{\text{ROMCE0}}$ pins.

16 Bit Memory Cycles

Expansion memory cycles result in the generation of $\overline{\text{SMRD}}$ for reads and $\overline{\text{SMWR}}$ for writes. During 16 bit references to Expansion bus memory devices, if the $\overline{\text{MEMCS16}}$ pin is enabled and is sampled low prior to the beginning of the ST2 SYSCLK cycle, the VG330 will execute a 16 bit transfer. If $\overline{\text{MEMCS16}}$ has not been enabled or if $\overline{\text{MEMCS16}}$ has not been returned by the sample point, the VG330 will generate consecutive 8 bit cycles to the Expansion bus device. The first cycle will be an even addressed byte access and the second an odd addressed byte access.

In the AT architecture, 16 bit memory cycles are normally decoded from the Latchable address bus, LA[23:17]. These address signals normally are valid prior to the SA[19:0] address bus. To provide 16 bit memory devices with additional address setup time, the start of an Expansion bus cycle may be delayed by 0, 1, 2, or 3 processor clocks.

I/O Cycles

Expansion I/O cycles result in the generation of $\overline{\text{SIORD}}$ for reads and $\overline{\text{SIOWR}}$ for writes.

During 16 bit references to Expansion bus devices, if $\overline{\text{IOCS16}}$ is enabled and is sampled low, the VG330 will execute a 16-bit transfer.

If $\overline{\text{IOCS16}}$ has not been enabled or if $\overline{\text{IOCS16}}$ has not been returned by the sample point, the VG330 will generate consecutive 8-bit cycles to the Expansion bus device. The first cycle will be an even addressed byte access and the second an odd addressed byte access.

PCMCIA Cycles

In some configurations, the PC Card slot memory signals $\overline{\text{OE}}$ and $\overline{\text{WE}}$ are output on the $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ pins. During 16-bit cycles to PC Cards, $\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ are driven by the internal 82365SL compatible PC Card controller and may be delayed versions of the standard 16-bit $\overline{\text{SMRD}}$ or $\overline{\text{SMWR}}$ memory strobes.

7.6 Related Registers

Register	**Address**
BCG Mode Register	Index 01H
Expansion Bus Mode Register	Index 34H
Expansion Bus I/O Wait State Control Register	Index 35H
Expansion Bus Memory Wait State Control Register	Index 36H

8 Memory Controller Unit

8.1 Introduction

The VG330's Memory Controller Unit allows designs to easily interface various kinds of memory without external glue logic. The VG330 supports DRAM, SRAM, PSRAM, ROM, and Flash memory devices.

The MCU provides all the control signals necessary to perform chip select and control for memory devices. It is designed to control memory refresh in a manner integrated into system operation, so the designer does not have to be concerned about providing external control of memory refresh and synchronizing it with system operation. The MCU also contains EMS mapping registers for greatest addressing flexibility.

8.1.1 Capabilities Summarized

The VG330's MCU supports:

- Fast page-mode DRAM operation for display refresh using:
  1Mx4, 4Mx4, 256Kx16, 512Kx8, 1Mx16 and 2Mx8.
- Staggered refresh for lower power transients
- 128Kx8 and 512Kx8 SRAM and PSRAM.
- 16 bit SRAM, PSRAM, DRAM, SRDRAM memory configurations, and high density x8 DRAM.
- x8 and x16 ROM
- BIOS shadowing
- Extensive support for memory saving "execute-in-place" ROM applications.
- Flash EPROM
- EMS mapping

8.2 MCU Architecture

Figure 8-1 shows the MCU from the viewpoint of system control.

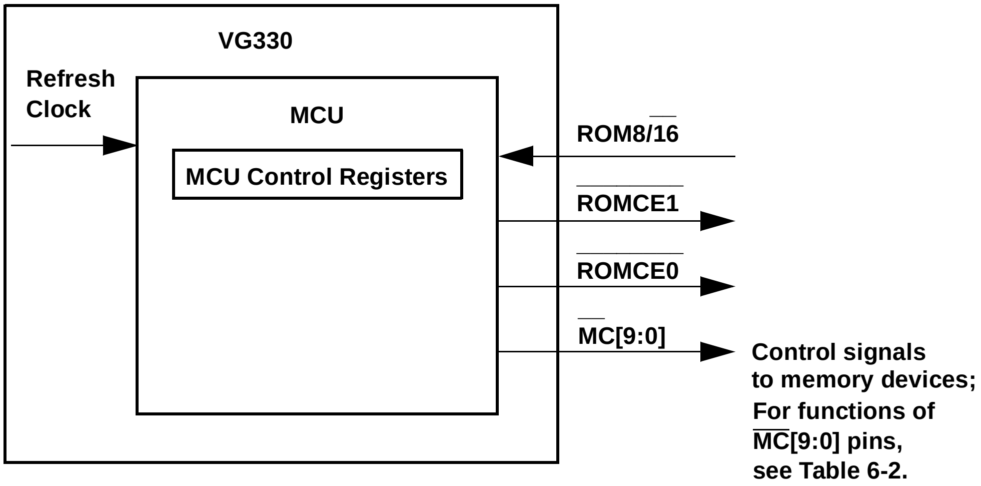

Figure 8-1 Memory Controller Unit

8.3 Related Pins

Table 8-1. Memory Controller-Related Signals and Pins

Pin	Type	Pins	Functions
$\overline{MC}$[9:0]	O	89:98	System RAM control signals. Functions of the pins vary depending on definition of type of system RAM. See Table 8-2.
ROM8/ $\overline{16}$	I	125	Strap pin option allowing selection of BIOS ROM0 width. Strap this pin low when using BIOS ROM that is 16 bits wide; strap high when using an 8 bit ROM.
$\overline{ROMCE[1:0]}$	O	87,88	ROM chip enable outputs. $\overline{ROMCE0}$ is asserted for memory read accesses to the BIOS ROM0 (address range F000:0 - FFFF:F) when the BIOS is not shadowed by RAM. Assertion of ROM chip enable outputs [1:0] for other address ranges may be specified using the VG330 EMS addressing.

8.3.1 Memory Controller Pin Mapping

The $\overline{\text{MC}}$[9:0] outputs are designed to provide memory control signals for RAM and ROM without additional external logic.

The function of each $\overline{\text{MC}}$ pin at any time depends on the type of memory that is being accessed at that time. For example, when the VG330 is accessing 16-bit wide DRAM in bank 0, if bank 0 has been defined as being 16-bit DRAM, then the MCU will output the $\overline{\text{CASL}}$ signal on pin $\overline{\text{MC}}$6 for that access. However, if the design uses PSRAM for bank 0, then the function of $\overline{\text{MC}}$6 for a memory access would be $\overline{\text{OEL}}$.

Table 8-2. Memory Controller Pin Functions

Signal	**Pin #**	**DRAM size (See Notes A and B)**		**SRAM**	**PSRAM (see Note C)**	**Flash ROM (see Notes A and D)**	
		x4 or x8 width	**x16 width**	**16 bit width**	**16 bit width**	**8 bit width**	**16 bit width**
$\overline{\text{MC}}$0	98	$\overline{\text{CAS0}}$	$\overline{\text{RAS0}}$	$\overline{\text{CS0}}$	$\overline{\text{CS0}}$	-	-
$\overline{\text{MC}}$1	97	$\overline{\text{CAS1}}$	$\overline{\text{RAS1}}$	$\overline{\text{CS1}}$	$\overline{\text{CS1}}$	-	-
$\overline{\text{MC}}$2	96	$\overline{\text{CAS2}}$	$\overline{\text{RAS2}}$	$\overline{\text{CS2}}$	$\overline{\text{CS2}}$	-	-
$\overline{\text{MC}}$3	95	$\overline{\text{CAS3}}$	$\overline{\text{RAS3}}$	$\overline{\text{CS3}}$	$\overline{\text{CS3}}$	-	-
$\overline{\text{MC}}$4	94	$\overline{\text{CAS4}}$	$\overline{\text{RAS4}}$	$\overline{\text{CS4}}$	$\overline{\text{CS4}}$ ($\overline{\text{REFL}}$)	-	-
$\overline{\text{MC}}$5	93	$\overline{\text{RASL}}$	$\overline{\text{RAS5}}$	$\overline{\text{CS5}}$	$\overline{\text{CS5}}$ ($\overline{\text{REFH}}$)	-	-
$\overline{\text{MC}}$6	92	$\overline{\text{RASH}}$	$\overline{\text{CASL}}$	$\overline{\text{OEL}}$	$\overline{\text{OEL}}$	-	-
$\overline{\text{MC}}$7	91	$\overline{\text{OE}}$	$\overline{\text{CASH}}$	$\overline{\text{OEH}}$	$\overline{\text{OEH}}$	-	-
$\overline{\text{MC}}$8	90	$\overline{\text{WEL}}$	$\overline{\text{OE}}$	$\overline{\text{WEL}}$	$\overline{\text{WEL}}$	-	$\overline{\text{WEL}}$
$\overline{\text{MC}}$9	89	$\overline{\text{WEH}}$	$\overline{\text{WE}}$	$\overline{\text{WEH}}$	$\overline{\text{WEH}}$	$\overline{\text{WE}}$	$\overline{\text{WEH}}$

A. $\overline{\text{WEL}}$ is the low byte, D[7:0], write strobe. $\overline{\text{WEH}}$ is the high byte, D[15:8], write strobe.

B. $\overline{\text{RASH}}$, $\overline{\text{OEH}}$, and $\overline{\text{WEH}}$ are asserted during Odd Byte and Word accesses for 16 bit DRAM arrays. $\overline{\text{RASL}}$, $\overline{\text{OEL}}$, and $\overline{\text{WEL}}$ are asserted during Even Byte and Word accesses for 16 bit DRAM arrays.

C.The functions of $\overline{\text{MC}}$[8:4] are defined differently depending upon the density of PSRAM interfaced to the VG330. For 128Kx8 PSRAM arrays, $\overline{\text{REFL}}$ drives the even addressed and $\overline{\text{REFH}}$ the odd addressed PSRAM $\overline{\text{REF}}$ pins. For 512Kx8 PSRAM arrays, $\overline{\text{OEH}}$ and $\overline{\text{OEL}}$ replace $\overline{\text{REFH}}$ and $\overline{\text{REFL}}$ and function in the same manner.

D. This is for designs where flash memory is placed in the RAM addressing space, instead of the ROM addressing space selected by $\overline{\text{ROMCE0}}$ and $\overline{\text{ROMCE1}}$. Flash ROM and SRAM/PSRAM cannot be interspersed; flash ROM always must be placed above the RAM in the memory space. For Flash ROM chip select, use the same assignments used for SRAM $\overline{\text{CS1}}$ through $\overline{\text{CS5}}$ as needed.

8.4 Memory Type Support

The VG330 provides hardware support for many kinds of memory devices. This section discusses memory types from the standpoint of system design.

8.4.1 DRAM Support

The VG330 provides complete support for a number of types of DRAM including 1Mx4, 4M x4, 256Kx16, 512Kx8, 1Mx16 and 2Mx8. However, proper operation for refresh cycles requires that you use only one type of memory and do not mix types.

The VG330 supports the following memory speeds (assuming a 32 MHz main clock):

- 60 ns SRAM
- 80 ns PSRAM
- 60 ns DRAM

RAM is placed in the RAM addressing space, which is controlled by the $\overline{\text{MC}}$[9:0] outputs.

For DRAM devices other than 256Kx16 and 1Mx16, the VG330 provides a pair of $\overline{\text{RAS}}$ strobes (odd byte/even byte), and a unique $\overline{\text{CAS}}$ for each DRAM bank. For x16 DRAM, the VG330 provides a pair of $\overline{\text{CAS}}$ strobes (upper byte/ lower byte) and a unique $\overline{\text{RAS}}$ strobe for each bank.

Standard memory access is byte or word access, and is not page-mode. However, the VG330 includes a page-mode DRAM controller and will generate page-mode cycles for LCD display refresh cycles. DRAM refresh is accomplished using CAS before RAS refresh cycles. The benefit of this type of refresh cycle is that a row address is not required and so additional power savings may be realized. The VG330 supports both standard and slow refresh DRAM as well as the newer self-refresh DRAM, (SRDRAM).

Refresh requests for DRAM and PSRAM are provided by an independent 8 bit refresh timer. See *DRAM Refresh Cycles* on page 8-8.

8.4.2 SRAM/PSRAM support

The VG330 provides support for 128Kx8 and 512Kx8 SRAM and PSRAM. During normal operation, if the system is configured for PSRAM, the VG330 generates auto-refresh cycles for PSRAM. When the VG330 enters SUSPEND mode, self-refresh is performed by the PSRAM.

8.4.3 ROM Support

The VG330 supports x8 and x16 ROM. The system may be programmed to use ROM devices that are either 8 bits or 16 bits, by means of a strap option and a programmable register bit.

The ROM 8/$\overline{\text{16}}$ pin can be strapped to define whether 8-bit wide or 16-bit wide ROM is being used for ROM0. Memory Control Register 2, at Index 05H, is used to define the size of ROM1.

Normally, ROM is used in the ROM addressing space, which is selected by the ROM chip selects.

The VG330 provides two ROM chip selects, $\overline{\text{ROMCE0}}$ and $\overline{\text{ROMCE1}}$. These signals are asserted any time the memory mapping registers are set to indicate one of these devices. This allows ROM arrays of up to 16 MBytes to be constructed using external decode logic.

$\overline{\text{ROMCE0}}$ is the BIOS ROM chip select and is asserted during memory accesses in the range F0000H - FFFFFH, unless the BIOS is shadowed by RAM. $\overline{\text{ROMCE0}}$ may also be asserted when one of the memory mapping registers are set to select ROM 0. When accessing the BIOS at addresses F0000H - FFFFFH, the upper address bits A[23:16] are forced low. This means the BIOS always occupies the first 64 Kbytes of any size ROM in which it is installed.

$\overline{\text{ROMCE1}}$ may only be accessed through one of the memory mapping registers when the device type is set to indicate ROM1.

8.4.4 Flash ROM Support

Flash ROM is supported by the VG330. It may be intermixed with standard ROM devices. Normally, Flash ROM is used in the ROM addressing space and is selected by the ROM chip selects, $\overline{\text{ROMCE0}}$ or $\overline{\text{ROMCE1}}$. The $\overline{\text{OE}}$ pins of Flash ROM may be connected to $\overline{\text{SMRD}}$ if this output has been enabled to provide $\overline{\text{OE}}$ for the ROM. See description of Expansion Bus Mode Register (Index 34H) bit D3 in Chapter 16.

It is also possible to connect $\overline{\text{OE}}$ of the Flash

ROM to one of the GPIO pins and disable $\overline{OE}$ during Flash writes. The $\overline{WE}$ pin of the Flash ROM may be connected to $\overline{MC}$8 or $\overline{MC}$9 depending on the Flash data width. See Table 8-2.

Note: The MC8 and MC9 pins remain active during suspend. It is the responsibility of the system designer to assure that these pins are properly buffered if the flash is to be powered down.

8.4.5 Shadow BIOS Support

BIOS ROM shadowing is supported by the VG330. See *Shadow RAM Usage* on page 8-8 of this chapter for more information.

8.5 Memory Controller Functional Description

The design of the MCU requires that system RAM on the data bus must always be 16 bits wide[1]. This may consist of one or more 16-bit wide RAMs, or two 8-bit RAMs, or four 4-bit RAMs. Where more than one chip is used, the devices must be of the same type. That is, DRAM may only be used with DRAM, PSRAM with PSRAM, and so on.

The system ROM arrays can be defined to the VG330 as being organized as 8-bit bytes or 16-bit words. Timing for accesses to this memory is based upon the processor clock, CPUCLK.

8.5.1 Mapping Registers

The CPU address space is 1 Mbyte. The lowest 640 Kbytes are reserved for system RAM. Out of the remaining 384 Kbytes of address space, 256 Kbytes can be accessed through memory mapping registers allowing access to large physical RAM or ROM memory spaces. There are 16 mapping registers, and each allows 16 Kbyte blocks of the memory map to be defined as RAM, ROM or Expansion bus memory.

The VG330 mapping registers are a super-set of the LIM EMS 4.0 mapping registers, and are accessed through the Mapper Address Registers at I/O Addresses 6CH, 6EH, and 6FH. See also Chapter 6, *Bus Architecture*.

When the CPU outputs an address that falls within the range of one of the memory mapping registers (for example, if the CPU address is A0xxxH, if mapping is enabled, this address will be translated by mapping register A0H; a CPU address of E0xxxH would be handled by mapping register E0H), the VG330 translates that address using a 10-bit value stored in the appropriate mapping register that provides physical address bits 23:14 to the external address bus.

To store a translation address for a 16 KByte block in the appropriate mapping register:

1. First write the high byte of the CPU address to the Mapper Address Register located at I/O address 6CH.

   For example: for a CPU address range starting with C0xxxxH, write C0H to I/O address 6CH.

2. Next, define the configuration for this block by writing into the Mapper High Byte and Low Byte Data Registers (at I/O addresses 06FH and 06EH) the physical address to which this should be translated. Also write an enabling flag into bit D7 of register 6FH, and define the memory type used at this physical address, using bits 5:4.

In addition, Global Map Enable must be enabled to use mapping. This bit is located in the Memory Control 1 Register at Index 04H.

The indexes of some of the mapping registers, and the regions of memory they map, are automatically shifted by the VG330 depending on which the video graphics mode the system is in. The assignment of address region in memory for the display buffer in a PC is at different places for CGA (640x200 or 640x400) graphics and VGA (640x480) graphics.

The diagram in Figure 8-2 shows the location of the mapping registers for CGA graphics mode, and for VGA monochrome video mode 11H. Note that the position of the mapping registers in both memory and in the I/O addressing space change depending on video mode: the Display Area Buffer for video changes places with the region of memory accessed by Mapping Registers 1 through 4.

8.5.2 Upper Address Pin Configura-

[1] (Memory on the ISA bus is not subject to this restriction.)

tion

The upper address pins, A[23:20], are configured on an individual pin basis. Three enable bits per pin allow each of the A[23:20] pins to be enabled for either RAM, ROM0, or ROM1 cycles.

These enable bits are located in the Address Pin Configuration Registers. When an address pin is enabled for a particular memory type, that address pin is driven by the address specified in the memory mapping registers.

For one of the upper address pins, if Bus Latching Mode (see Chapter 6, *Bus Architecture*, for discussion of this mode) is enabled and that address pin is configured to be disabled for accesses to a particular memory type, then upon such an access that address pin is latched and held at the last address driven on the bus. This allows power to be conserved because these address lines are not switched under this condition.

The Address Pin Configuration Registers also allow control of the A[19:12] pins of the address bus in the same way. If Bus Latching Mode is enabled, then during I/O cycles, A[19:16] pins that have been configured for latching will be driven with the previous address. Similarly, During RAM cycles, when system memory is DRAM, the A[19:12] pins may also be latched if so configured.

8.6 CPU Read/Write Cycles

8.6.1 Wait States

RAM, ROM0, and ROM1 wait states are each independently controlled through the ROM Wait State Control and RAM Wait State Control Registers. Wait state selections are from zero to 7. For slow DRAM or PSRAM, the start of the $\overline{\text{RAS}}$ or $\overline{\text{CE}}$ cycle may be delayed by one processor clock cycle to provide additional address setup timing.

8.6.2 Flash Cycles

See *ROM/FLASH Timing* on page 3-13, for timing diagrams for ROM/flash cycles.

8.6.3 BIOS ROM Cycles

See *ROM/FLASH Timing* on page 3-13 for timing information for ROM selected by $\overline{\text{ROMCE0}}$.

Address	Usage in 640x200/640x400 Video Mode	Usage in 640x480 Video Mode
FFFF:FH F000:0H	ROM BIOS	ROM BIOS
EFFF:FH E000:0H	Mapping Registers 13-16	Mapping Registers 13-16
DFFF:FH D000:0H	Mapping Registers 9-12	Mapping Registers 9-12
CFFF:FH C000:0H	Mapping Registers 5-8	Mapping Registers 5-8
BFFF:FH	CGA (640x200/640x400) Mode - Display Buffer Area	Mapping Registers 1-4
B800:0H	---	---
B000:0H		
AFFF:FH A000:0H	Mapping Registers 1-4	Video Mode 11h - 640x480 Display Buffer Area
9FFF:FH 0000:0H	Reserved for System RAM	Reserved for System RAM

Figure 8-2 VG330 Memory Mapper Regions Depend on Video Modes[1]

[1] Note that panel resolution is independent from video mode resolution, of course.

8.7 Refresh Cycles

8.7.1 Enabling and Selecting Refresh Period

Refresh requests for DRAM and PSRAM are provided by an independent 8 bit refresh timer. This timer is the Refresh Timer Register at Index 7FH. Refresh rates range from a refresh every 15.26 µs, down to as slow as every 3.89 ms.

8.7.2 DRAM Refresh Cycles

See Chapter 3, *Electrical Specifications*, for timing diagrams for DRAM cycles.

8.7.3 PSRAM Refresh Cycles

See Chapter 3, *Electrical Specifications*, for timing diagrams for PSRAM cycles.

8.7.4 SUSPEND Mode Refresh Cycles

For a discussion of the behavior of memory refresh during the SUSPEND power management state, refer to Chapter 14, *Power Management Unit*.

8.7.5 Staggered Cycles and Power Buses

When using more than one DRAM or PSRAM chip, it is generally desirable to have a means of staggering refresh cycle operations for the chips so as to minimize instantaneous high-current drains. The VG330 automatically staggers cycles for memory banks (odd and even) when configured for more than one DRAM or PSRAM. (It only staggers refresh when there are physical odd and even banks.) To do this, the $\overline{\text{CAS}}$ strobes for banks other than the primary chip are each delayed by one cycle. In this way, the VG330 automatically reduces instantaneous demand on system power.

8.8 Shadow RAM Usage

The ROM BIOS image located in the lower 64 Kbytes of ROM0 may be shadowed in system RAM to improve system performance. The RAM location of the BIOS image is programmable and may reside anywhere in the 16 MByte RAM memory space.

When an 8-bit BIOS ROM is used, if it is shadowed to 16-bit RAM, a system performance advantage can be gained due to increased access speed. That is, only one RAM fetch is required, versus two 8-bit ROM cycles.

The VG330 provides two registers to control Shadow RAM: the BIOS Shadow RAM Address register and the BIOS Shadow RAM and EMS Control register. The starting address of the BIOS image in RAM is specified by the BIOS Shadow RAM Address register.

Refer to the Chapter 16 description of the BIOS Shadow RAM Address Register (Index E8H), and the BIOS Shadow RAM and EMS Control register (Index E9H) for programming information on controlling shadowing.

The following outlines the process of enabling BIOS Shadow RAM:

1. Define the physical starting address in RAM where BIOS image will reside, using the BIOS Shadow RAM Address Register at Index E8H.
2. Make ROM read-only, and BIOS Shadow RAM area write-only, by programming the following values into bits in the BIOS Shadow RAM and EMS Control Register (Index E9H):
   bit D7 = 1
   bit D6 = 0.
   (continued)
3. Copy the BIOS code from ROM to RAM by copying F0000H - FFFFFH segment to itself (BIOS image will be copied from ROM to RAM). The 8086 string move instruction is useful for this.
4. Write-protect the RAM by programming the following values in to the register at Index E9H:
   bit D7 = 0
   bit D6 = 1.

Once enabled, all accesses to the BIOS region at F0000H - FFFFFH will be remapped to the address programmed in the BIOS Shadow RAM Address register.

8.9 Display Memory

The VG330 implements a unified main system RAM and video Display Buffer RAM architecture. This means that the Display Buffer Area is physically part of main system RAM. Use of this area is configured by the LCD Configuration Control Register, Index 07H, bit D7. Once this is done, the position in RAM of the Display Buffer Area is controlled by the setting for the system's video mode. See Figure 8-2 and the discussion under *Mapping Registers* on page 8-5 of this chapter. See also the discussions in Chapter 9, *LCD Controller Unit*:

The Display Buffer Area size is set using the register at Index 38H.

The Display Buffer Area is typically located in the upper-most 32 or 64 Kbytes (the top of the last RAM bank), depending on video mode. However, the exact location within the last RAM memory bank is register selectable. The default location of the Display Buffer Area is always accessible through the standard CGA address space, B8000H - BFFFFH or the VGA address space, A0000H-AFFFFH, depending on the video mode.

The Display Buffer Area is physically part of main RAM and is also accessible through the memory mapping registers. The Alternate Display Buffer Start Address Register at Index 06H controls usage of an alternate Display Buffer Area also in main RAM.

Note that the speed of video memory accesses can be adjusted using the LCD Configuration Control Register at Index 07H.

8.9.1 Effects of RAM Refresh Cycles on Display Refresh

The LCU includes internal line buffers used to temporarily store data from the Display Buffer Area. This data is then processed and output to the LCD.

A Panel Refresh is the action of sending data to the LCD panel from the Line Buffer within the LCU. (There are two sections in the line buffer, which are alternately filled in a ‘ping-pong’ fashion’. The VG330 automatically sends the output of the alternate halves at the correct time.)

A Video Refresh is the process of refreshing the Line Buffer from the Display Buffer Area within main RAM memory. Periodically, the LCU requires access to main memory to refill the Line Buffer. When this occurs, the LCU arbitrates for control of the bus, much the same as the MCU refresh logic does.

Once granted control of the bus, the LCU performs a burst read from the Display Buffer Area in main system RAM and stores the data in the appropriate line buffer. The VG330 provides register programmable bits to specify the access timing of these bursts.

For DRAM-based systems, the LCU will perform page-mode DRAM cycles to refill the line buffers. These cycles offer a 60% performance improvement over standard DRAM cycles.

DRAM refresh interacts with Video Refresh in the following way:

Once a Video Refresh is in progress, one of three things can happen:

1. The Video Refresh can proceed to completion uninterrupted should no other activity get in the way.
2. If a DRAM Refresh is invoked by the MCU, then the Video Refresh is halted, the DRAM refresh occurs to completion, and the MCU allows the Video Refresh to continue.
3. If a row miss occurs in RAM access, the MCU needs to perform a recovery from row fetch, and then it resumes the transfer from the Display Buffer Area in RAM to the Line Buffer.

8.10 Related Registers

The MCU registers are accessed using the standard VG330 Index and Data registers.

Table 8-3. Memory and Memory Controller-Related Registers

Register	Address
Alternate Display Buffer Start Address Register[a]	Index 06H
Address Pin Configuration Register 1	Index 14H
Address Pin Configuration Register 2	Index 15H
Address and Data Pin Configuration Register 3	Index 16H
Memory Control 1 Register	Index 04H
Memory Control 2 Register	Index 05H
LCD Configuration Control Register[b]	LCD Index 07H
LCD T3 Register[c]	LCD Index C8H
RAM Wait State Control Register	Index 7DH
Refresh Control Register	Index 7FH
Refresh Timer Register	Index 7EH
ROM Wait State Control Register	Index 7CH
BIOS Shadow RAM Register	Index E8H
BIOS Shadow RAM and EMS Control Register	Index E9H
Mapper Address Register	I/O Address 6CH
Mapper Low Byte Data Register	I/O Address 6EH
Mapper High Byte Data Register	I/O Address 6FH
Top of Memory Register[d]	Index 38H

a. Enables the Alternate Display Buffer
b. Enables LCU; reserves part of main memory for Display Buffer Area; sets speed of access to video memory.
c. Determines location of Display Buffer Area in memory
d. Sets Display Buffer Area size

8.10.1 Initialization, Setup, and Dependencies

Designing system memory in a VG330 system is relatively uncomplicated, though designers must ensure that the appropriate registers are configured. Once this is done, memory performance is determined by several factors:

- processor clock rate
- wait state settings
- memory access speed
- the amount of loading on the address and data buses.

8.10.2 Design Example

Figure 6-3 shows usage of the $\overline{\text{MC}}$[9:0] pins in an example.

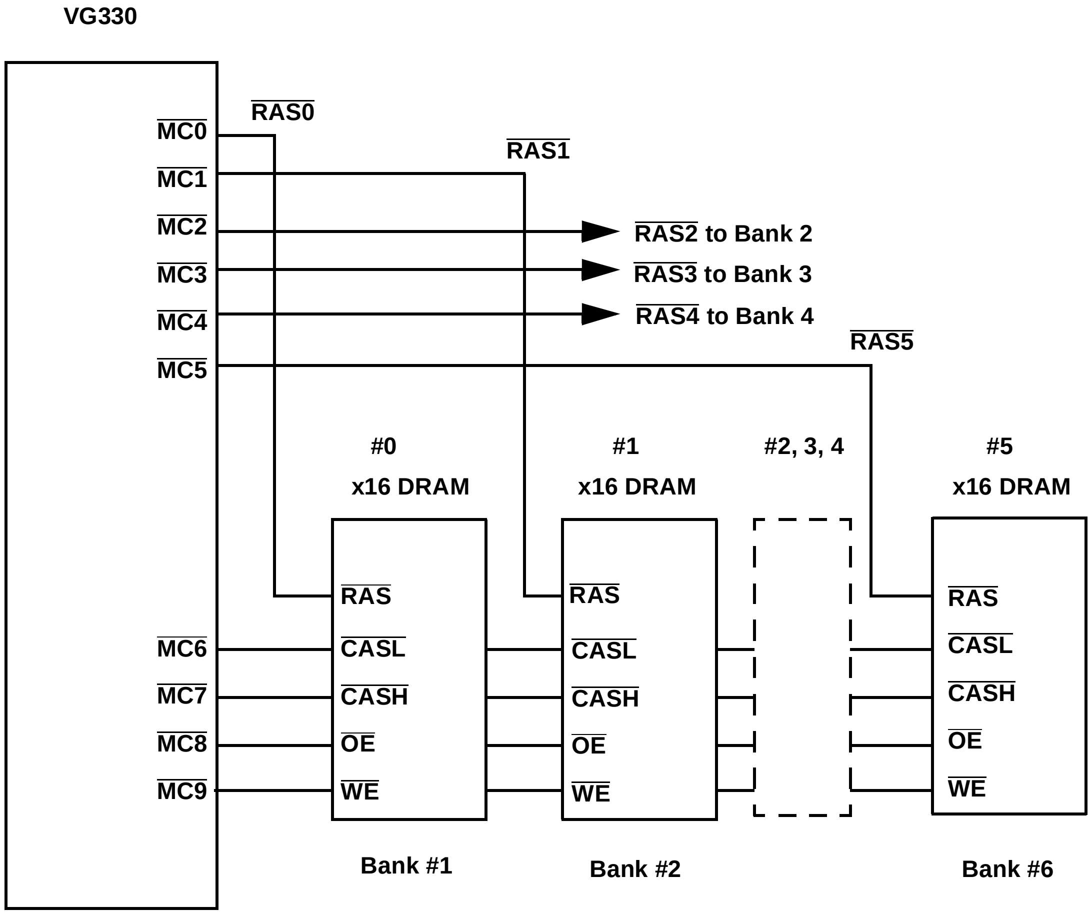

Figure 8-3 x16 DRAM Design Example

9 LCD Controller Unit

9.1 Introduction

The VG330 integrates an LCD panel controller unit (LCU) which may be configured to support a wide variety of LCD resolutions. The VG330's Power Management Unit works in conjunction with the LCU to fully control all LCD activities such as power-up and power-down sequencing and control during various power-management states of the system.

9.1.1 Capabilities Summarized

The VG330 LCD Controller Unit supports these video modes:

- CGA (640x200/640x400) 2 color (monochrome) graphics (mode 6)
- VGA (640x480) 2 color (monochrome) graphics, (VGA mode 11).

Note: VG330 LCD controller is neither fully CGA or VGA compatible.

For 200 line graphics mode, the LCD controller supports 'double-scanning' of the 200 line display data, either to fill a display greater than 200 lines or to provide a 2x zoom.

CGA-compatible display images can be viewed on sub-CGA resolution displays using a technique called "panning".

9.2 Architecture

The block diagram in Figure 9-1 shows the LCD Controller Unit's major internal function blocks, the main interface pins, and major internal system connections.

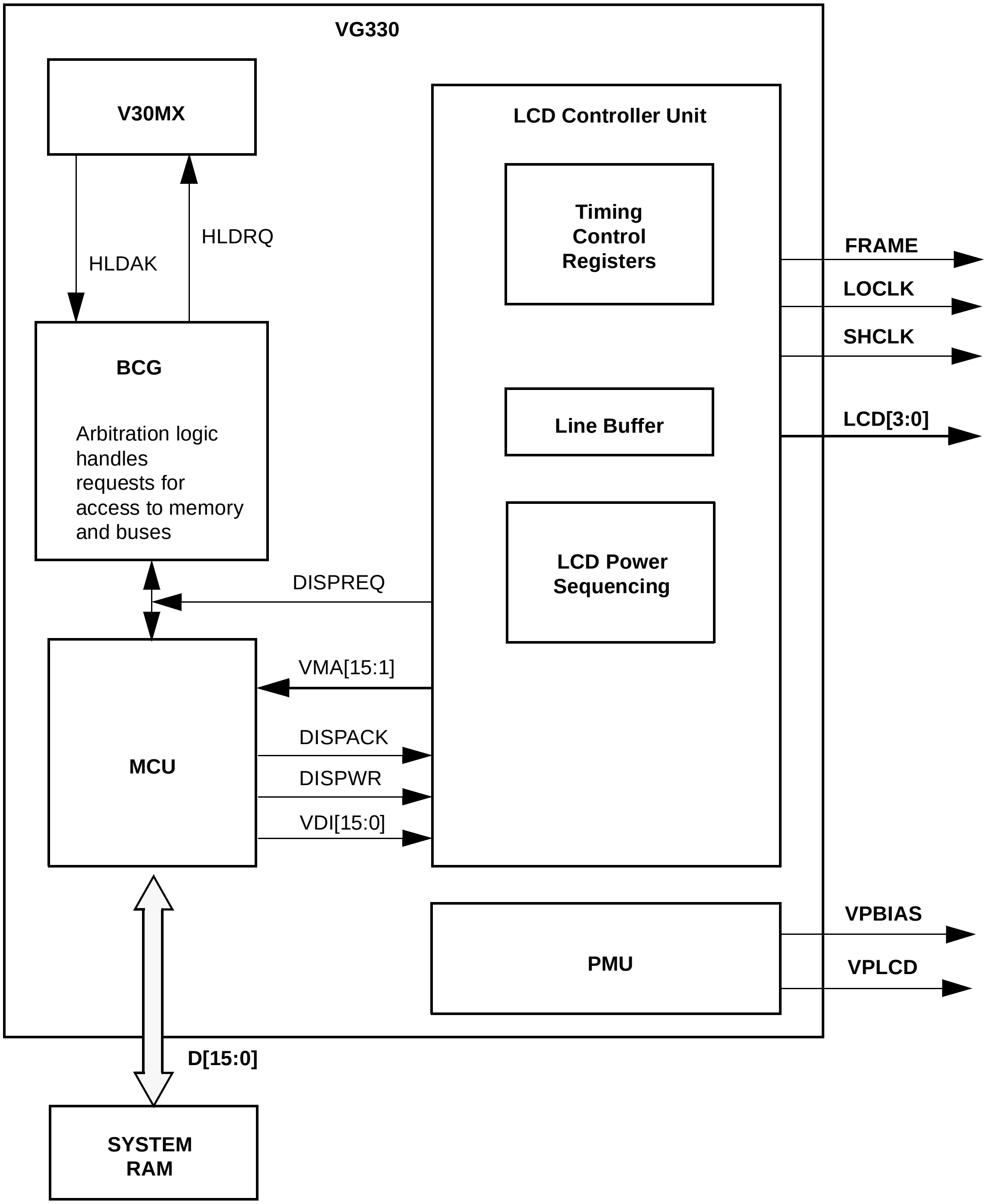

Figure 9-1 LCD Controller Main Elements

9.3 Related Pins

Table 9-1. LCD Controller Unit Pins and Related Signals

Name	Type	Pins	Function
FRAME	O	50	Frame clock to LCD.
LCD [3:0]	O	56:53	Display data out to LCD.
LOCLK	O	51	Load clock out to LCD.
SHCLK	O	52	Shift clock out to LCD.
VPBIAS	O	48	BIAS power gate for LCD panel, from VG330 PMU.
VPLCD	O	49	VCC power gate for LCD panel, from VG330 PMU.

9.4 LCU Control Registers

The LCU registers are in an indexed group accessed through control registers in the CGA-compatible I/O space, 3D4H - 3DEH. Programmers may use the standard CGA index and data registers located at I/O addresses 3D4H and 3D5H to access the VG330-specific registers which are included for selecting LCD panel resolutions and controlling LCD timing.

9.5 Memory Assignment

The VG330 implements a unified main system RAM and video RAM architecture. This means that the display buffer is physically part of main system RAM.

The display buffer is typically located in the upper-most 32 or 64 Kbytes depending on video mode. However, the exact location within the last RAM memory bank is register-selectable. The default location of the display buffer (last 32 or 64 Kbytes of last RAM bank) is always accessible through the standard CGA address space, B8000H - BFFFFH or VGA address space, A0000H-AFFFFH depending on the video mode.

Since the display buffer is physically part of main RAM, it is also accessible through the memory mapping registers.

For a discussion of video memory in the system, refer to Chapters 6 and 8 in this document.

The LCU includes internal line buffers which temporarily store display buffer data which is processed and output to the LCD. Periodically, the LCU requires access to main memory to refill these line buffers. When this occurs, the LCU arbitrates for control of the bus, much the same as the Refresh logic does. Once granted control of the bus, the LCU performs a burst read from the display buffer in main system RAM and stores the data in the appropriate line buffer. The VG330 provides register programmable bits to specify the access timing of these bursts. For DRAM based systems, the LCU will perform page-mode DRAM cycles to refill the line buffers. These cycles offer a 60% improvement over standard DRAM cycles.

9.6 LCD Panel Interface Timing

9.6.1 Clock Prescaler

Refere to the LCU section of Chapter 16 for a description of the registers controlling:

- prescaling for the LCD clock
- Shift Clock Generation
- Load Clock Generation

9.7 LCD Power Control

The LCU works together with the VG330's power management logic to provide power control of the LCD panel. The LCU can be programmed to provide a number of options for LCD power-up or power-down sequences. Each option is independently selectable so power sequencing can be disabled on a power-down during critical system situations such as a battery failure.

LCD power control is coordinated with the VG330 Power Management Unit operation under the various power states of the system. (For more information, refer to Chapter 14, *Power Management Unit*.)

9.8 Related Registers

The LCD video-related registers reside in the CGA-compatible I/O space, 3D4H - 3DEH. A number of additional VG330-specific registers are included for selecting LCD panel resolutions and controlling LCD timing. These registers are accessed using the standard CGA index and data registers located at I/O addresses 3D4H and 3D5H. The VG330 may be placed in VGA mode using the LCD T3 register at LCU Register Index C8H.

Table 9-2. LCD Controller Unit Registers

Register	Address
LCU Index Register	I/O Address 3D4H
LCU Data Register	I/O Address 3D5H
LCU Mode Select Register A	I/O Address 3D8H
LCU Mode Select Register B	I/O Address 3DEH
The following LCU registers are reached through the LCU Index Register at I/O Address 3D4H and the LCU Data Register at I/O Address 3D5H:	
LCD Configuration Control Register	Index 07H
Display Start Address MSB Register	Index 0CH
Display Start Address LSB Register	Index 0DH
LCD T1 Register	Index C6H
LCD T2 Register	Index C7H
LCD T3 Register	Index C8H
LCD T4 Register	Index C9H
LCD Horizontal Resolution Register	Index CAH
LCD Vertical Resolution Register	Index CBH
LCD Mode Register	Index CCH

10 Keyboard Controller Unit

10.1 Introduction

The VG330 includes a Keyboard Controller Unit, or KCU, that handles almost all hardware functions required for interfacing the chip with a keyboard. This section discusses the controller's capabilities and the nature of its usage.

For information on VADEM BIOS extensions supporting scanned keyboard interfacing, refer to the VADEM OEM BIOS Adaptation Manual.

10.1.1 Capabilities

Types of Keyboards Supported

When set up for serial keyboard interface, the VG330 is compatible with a standard PC/XT keyboard.

When set up for keyboard matrix scanning, the VG330 can be used with any keyboard matrix proving a contact closure when a key is pressed. The VG330 provides key debouncing capability through a BIOS call.

Types of Keyboard Interfaces Supported

The VG330's KCU supports using either of two main types of keyboard interfaces.

The first type is a standard XT serial keyboard interface using bi-directional Keyboard Clock and Keyboard data pins, KBCLK and KBDAT. (An AT style keyboard may also be interfaced to the VG330 using an external 8042-based keyboard controller.)

The second type of interface performs scanning of a keyboard matrix, using Scan and Return pins as discussed later in this chapter. The VG330 also supports two types of scanning, each with its own advantages. All three forms are listed in Table 10-1.

Table 10-1. Supported Types of Keyboard Interfaces

Type	Capabilities
XT Serial	Allows attaching a standard PC/XT keyboard through two serial lines.
Full Scan	Allows scanning a keyboard matrix; requires assigning a quantity of GPIO pins for the SCAN and RETURN sides of the matrix. The largest matrix supported is 12 x 12, which takes up all available GPIO pins.
Partial Scan	Allows scanning a keyboard matrix; requires fewer pins than Full Scan; requires use of an external buffer chip.

10.2 Keyboard Controller Unit Architecture

The design of the VG330 provides for keyboards to be interfaced to the KCU through the GPIO pins. See Figure 10-1. The KCU has no direct pins to the outside. Instead, GPIO pins are assigned to the KCU by programming the GPIO mode registers. Refer to the discussion of GPIO in Chapter 10 for details on assigning GPIO pins to KCU signals.

Since the keyboard interface is routed through the GPIO function block, an overall system design involves evaluating trade-offs between desired functionalities, and available I/O pins.

Once pins have been assigned, the KCU configuration is programmed through the Keyboard Scan Enable Register at the VG330 register index 066H. Details are given later in this chapter.

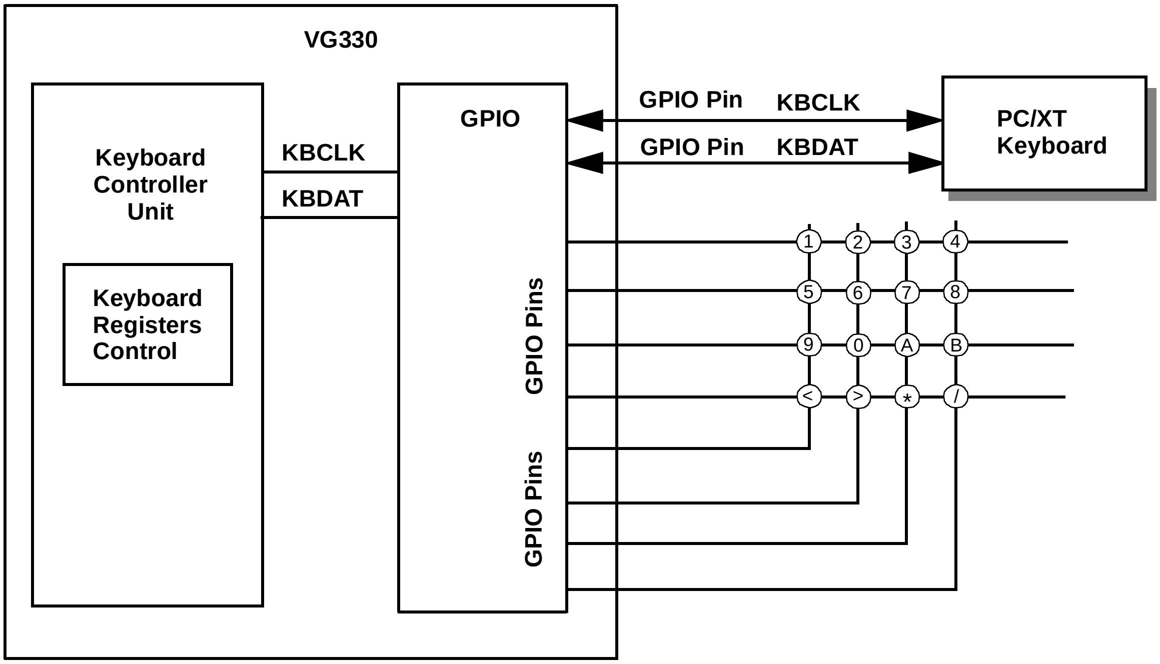

Figure 10-1 Keyboard Controller Unit Block Diagram

10.3 Related Pins and Signals

For convenience of discussion, the KCU signals used in keyboard interfacing that can be routed through the GPIO pins are listed in Table 10-2, which also shows the GPIO pins they can be routed to.

Note that every GPIO pin can alternatively be used as either a SCAN or RETURN pin, for convenience in physical layout. However, also note that non-sequential assignments require extra software overhead for handling.

Table 10-2. Keyboard Signals and GPIO Pins

Mappable Signal	I/O Type	GPIO Group C Pin								GPIO Group B Pin								GPIO Group A Pin							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
KBCLK	I																	■							■
KBDAT	I																		■					■	
RET	I	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCAN	O	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCS0	O							■				■			■					■					
PCS1	O						■				■			■			■		■						■
PCS2	O					■				■			■					■						■	

Note: Black cells in table show where a signal in Mappable Signal column can be mapped through a GPIO pin. Example: Keyboard SCAN signal 22 can be mapped as an output through GPIO Group C pin 6. KBCLK signal can be mapped as an input through GPIO Group A pin 7 or through pin 0.

10.4 PC/XT Serial Keyboard Interfacing

The PC/XT serial keyboard interface may only be enabled on select pins in the GPIO pin group A.

The Keyboard Controller Unit may be configured to support a PC/XT-compatible serial keyboard interface. This interface is composed of two signals, KBCLK and KBDAT, which must be enabled on a pair of GPIO pins. The following GPIO pins support KBCLK or KBDAT configurations:

KBCLK	KBDAT
GPIOA7	GPIOA6
GPIOA0	GPIOA1

Both KBCLK and KBDAT are defined as “wire-or” signals, which means that each source, the keyboard and the VG330, can drive these signals low but not high. The GPIO pins defined as KBCLK and KBDAT must therefore be externally pulled high using a resistor pull-up.

Normally, the keyboard interface is driven by the external keyboard. The VG330 only drives the interface under one of the following conditions:

- Following receipt of a scan code transmitted by the external keyboard, the VG330 drives both KBCLK and KBDAT low to acknowledge the transfer and hold off further transfers until the scan code has been read by the keyboard handler.
- During a keyboard reset when the PPIB Keyboard Control register bit D6 is reset low, the VG330 drives KBCLK low until bit D6 is set back high.

The PC/XT serial keyboard interface makes use of two registers located at compatible I/O addresses.

The PC/XT PPIA Keyboard Data Register at I/O address 060H is read to obtain the keyboard scan code shifted into the VG330 through the KBDAT signal.

The PC/XT PPIB Keyboard Control Register at I/O address 061h controls the keyboard interface as well as other PC/XT compatible functions such as reading system switches and the speaker.

These registers are described in the Related Registers section of this chapter. The following paragraphs summarize usage:

Bit D3, ENASCAN, of the Keyboard Scan Enable Register at index 066H controls the source driving the PC/XT compatible PPIA Keyboard Data Register accessed at I/O address 060H and how IRQ1 is generated. This bit essentially selects the primary keyboard interface and controls how keyboard scan codes are passed to system software.

When the ENASCAN bit is low, the PC/XT serial keyboard interface is selected as the primary keyboard interface. (When the ENASCAN bit is set high, the scanned keyboard matrix is selected as the primary keyboard interface.) The PPIA Keyboard Data Register is configured as Read Only and keyboard scan codes read from this register are generated by the PC/XT serial keyboard interface shift register. The shift register also generates an IRQ1 when one character has been received to signal the standard keyboard handler that keyboard data is available.

Keyboard scanning can still be performed while the ENASCAN bit is low, but in this case BIOS must use another mechanism to pass scan codes to the system. An example of such an implementation would be an icon based touch pad where primary keyboard input is handled by the PC/XT serial keyboard interface and the touch pad is handled by the keyboard scanner.

Just as keyboard scanning is permitted while the PC/XT serial keyboard interface is defined as the primary keyboard interface, the serial keyboard interface remains enabled when keyboard scanning is selected as the primary interface.

However, access to data received through the serial interface shift register is handled differently in this case. For this mode, data transmitted through the PC/XT serial interface may be read in the Shadow XT Shift Register at VG330 index address 068h. Also, note that the PC/XT serial keyboard interface is not able to generate an interrupt when a character has been received and so the interface must be polled.

10.4.1 Serial Keyboard Protocol

The PC/XT serial keyboard interface uses a 9-bit protocol where the first bit received by the interface is defined as the start bit and is followed by 8 bits of data. The timing diagram in Figure 10-2 illustrates a typical serial transfer from the keyboard.

The PC/XT serial keyboard interface performs the serial to parallel conversion of keyboard data using a 9-bit shift register. Bits D[8:0] of this register represent the keyboard scan code and bit D0 drives IRQ1. The external keyboard drives new data onto KBDAT on rising edges of KBCLK and the VG330 clocks this data into the shift register on the falling edge of KBCLK.

As the diagram in Figure 10-2 shows, the first bit transmitted by the keyboard is the start bit. Following the start bit, data is transferred in ascending order. On the falling edge of KBCLK when bit 7 is captured in the shift register, the start bit is shifted into bit D0 and IRQ1 is asserted. At the same time, the VG330 drives KBCLK and KBDAT low to acknowledge receipt of the keyboard data and prevent the external keyboard from transmitting new data. The VG330 continues to drive KBCLK and KBDAT low until the keyboard handler clears the PPIA Keyboard Data Register and IRQ1.

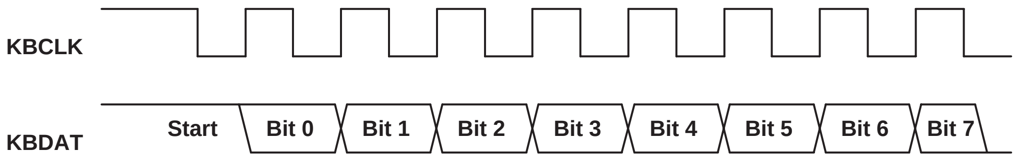

Figure 10-2 Serial Keyboard Interface Timing

10.5 Scanned Matrix Keyboard Interfacing

Keyboard scanning is supported for normally open switch matrixes where a key press causes a connection to a column and row in the matrix.

This section describes the two types of matrix keyboard scanning. In the first case, called Full Scan, the VG330 is directly connected to the keyboard matrix via the SCAN and RETURN signals.

In the second case, called Partial Scan, the VG330 only provides the SCAN signals for the keyboard matrix and the RETURN status is read from an external three-state buffer connected to the D[15:0] pins.

For keyboard scanning, any of the GPIO pins may assigned as either a SCAN output (three-state output) or RETURN input (active low input).

10.5.1 Full Scan Theory of Operation

For Full Scan operation, the keyboard scanner is intended to interface to a normally open switch matrix. External pull-up resistors hold the return inputs at a high level while all switches are open. The scan signals are three-state outputs which become low driven when enabled.

The basic scan method is summarized as follows: a keypress causes a RETURN line to go low; logic internal to the KCU then triggers an NMI; the VG330 is commanded to scan the matrix to determine which key is down. The following describes details of this.

1. The BIOS sets all SCAN lines low when the keyboard is idle, and the RETURN lines are externally pulled to VCC using a resistor network.

2. Any key depressed while all scan outputs are enabled will cause one of the RETURN lines to go low, causing an NMI to be generated, telling the BIOS that a key has been depressed. The BIOS enables a programmable timer in the keyboard scan logic which generates a periodic NMI so that the BIOS may scan the keyboard for the depressed key and perform software debouncing.

4. After receiving the NMI, the BIOS begins scanning the keyboard by first making all SCAN lines high-impedance, then selectively enabling individual SCAN lines to be driven low. The BIOS reads the RETURN status register to determine which return line is low. After the location of the key has been determined and the system has been notified that keyboard input is available, the BIOS:

- returns all the Scan lines to their low state
- translates the key input into an XT scan code
- writes this scan code to the keyboard data register at I/O address 60H, which causes an IRQ1 which then calls the keyboard handler
- then waits for the next key press.

Selecting the KCU’s Full Scan Mode

Full scan mode is selected by setting to zero bit D2, SCANMD, of the Keyboard Scan Enable Register.

Assignment of a particular GPIO pin to support either SCAN or RETURN functions is made by programming the appropriate GPIO mode register. Please refer to the GPIO section for details on programming the GPIO mode registers.

Only those GPIO pins configured as SCAN outputs may be controlled by the SCAN control registers. Once selected as a SCAN output, that GPIO pin is driven low when its associated SCAN control register bit is set high and driven to a high impedance state when its SCAN control register bit is reset low. Likewise, when reading the RETURN status registers, only those bits which have corresponding GPIO pins configured as RETURN inputs will return valid status. All other bits will read back high.

The diagram in Figure 10-3 illustrates a typical implementation for an 8x8 keyboard matrix where the GPIOB[7:0] pins are defined as SCAN outputs and the GPIOA[7:0] pins as RETURN inputs.

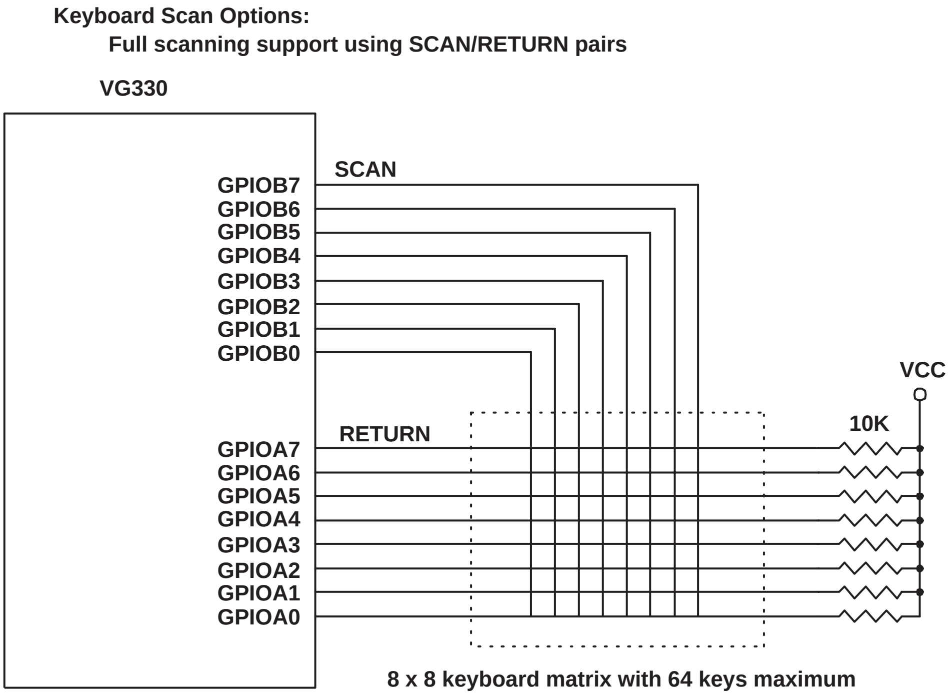

Figure 10-3 Configuration for Keyboard Full Scan

10.5.2 SCAN and RETURN Signals and the GPIO

The Keyboard Controller provides three SCAN control registers and three RETURN status registers.

Each SCAN control register can control eight GPIO pins and each RETURN status register can return the state of eight GPIO pins when read. These registers are mapped as shown in Table 10-3:

Table 10-3. SCAN and RETURN Control and Status Bits

Bit of the SCAN Control A Register that controls the state of the GPIO pin listed in column 2:	Controlled GPIO Pin	Bit in the RETURN Status A Register that shows the status of the GPIO pin in column 2 when sensing RETURN
D7	GPIOA7	D7
D6	GPIOA6	D6
D5	GPIOA5	D5
D4	GPIOA4	D4
D3	GPIOA3	D3
D2	GPIOA2	D2
D1	GPIOA1	D1
D0	GPIOA0	D0

Bit of the SCAN Control B Register that controls the state of the GPIO pin listed in column 2:	Controlled GPIO Pin	Bit in the RETURN Status B Register that shows the status of the GPIO pin in column 2 when sensing RETURN
D7	GPIOB7	D7
D6	GPIOB6	D6
D5	GPIOB5	D5
D4	GPIOB4	D4
D3	GPIOB3	D3
D2	GPIOB2	D2
D1	GPIOB1	D1
D0	GPIOB0	D0

Bit of the SCAN Control C Register that controls the state of the GPIO pin listed in column 2:	Controlled GPIO Pin	Bit in the RETURN Status C Register that shows the status of the GPIO pin in column 2 when sensing RETURN
D7	GPIOC7	D7
D6	GPIOC6	D6
D5	GPIOC5	D5
D4	GPIOC4	D4
D3	GPIOC3	D3
D2	GPIOC2	D2
D1	GPIOC1	D1
D0	GPIOC0	D0

10.5.3 Matrix Partial Scan Operation

This configuration has the advantage of freeing up more GPIO pins for use as other functions.

Partial Scan Hardware Configuration

Unlike full scan operation, the partial scan hardware design approach does not allocate many GPIO pins for RETURN inputs. Instead, it uses a single GPIO pin configured as a programmable chip select that is connected to an external three-state buffer located between the RETURN lines from the keyboard matrix and the D[15:0] bus. The programmable chip select is configured for a single byte or word I/O address, depending on the number of return lines from the keyboard matrix, and is I/O read qualified. The diagram in Figure 10-4 illustrates a typical partial scan implementation for an 8x8 keyboard matrix.

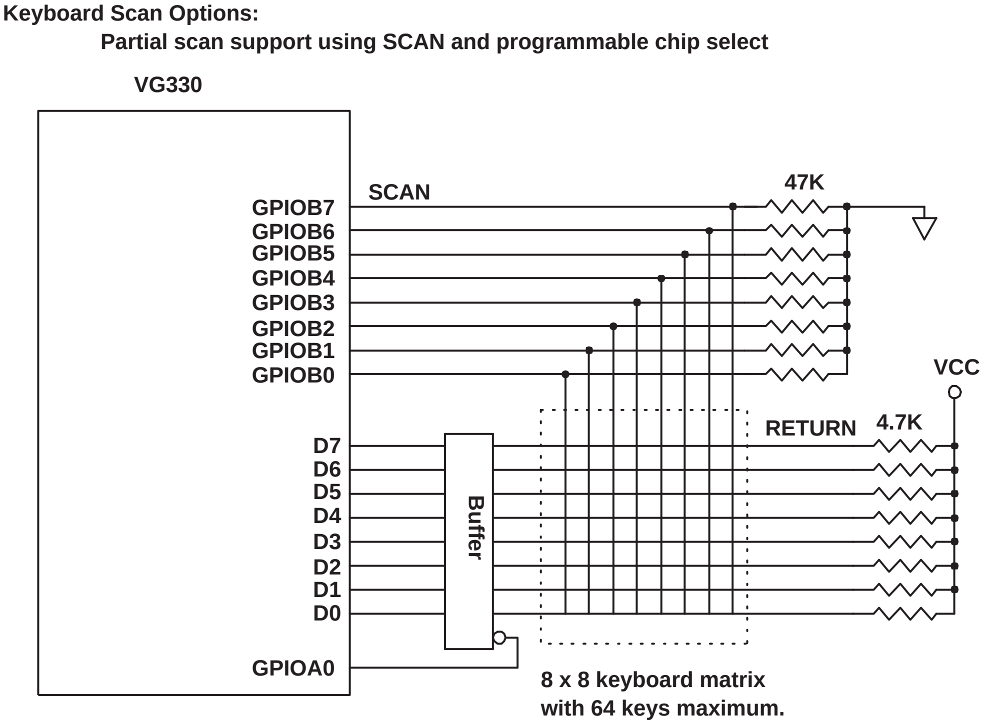

Figure 10-4 Configuration for Keyboard Partial Scan

Partial Scan Theory of Operation

One major difference between partial scan mode and full scan mode is that RETURN status is read from the external data bus, D[15:0], instead of the RETURN Status Registers and the SCAN signals are initialized as three-state (high impedance) in order to generate NMI on any key press.

In the Partial Scan configuration, external three-state buffers such as the 74LVT244 are utilized for reading the RETURN lines from the keyboard matrix. One of the programmable chip selects must be reserved for decoding of the I/O address where the RETURN status will be read and should be configured as I/O read qualified. This chip select output can then be directly connected to the enable pins of the external 74LVT244 buffers.

In full scan mode, the VG330 detects a line pulled low upon keypress, but in partial scan mode the VG330 looks for a line going high. The SCAN lines are externally pulled low using large value resistors, typically 47K Ohms. The RETURN lines are pulled to VCC by much smaller resistors, typically 4.7K Ohms.

The KCU monitors the status of the SCAN lines and generates an NMI to inform the system of a key press when any one of these SCAN lines are set high. Software then selectively drives each SCAN line low while making the others go to a high impedance state to search for the depressed key, pulled to VCC by the smaller value resistors.

For partial scan, the BIOS initializes the SCAN Control B Register to 00H causing all SCAN signals to be driven to a high impedance state. With no keys pressed, the 47 KOhm pull-down resistors hold all SCAN lines low. Any keypress will cause one of the SCAN signals to be pulled high through the 4.7K/47 KOhm resistor divider, which will then generate an NMI to inform the BIOS of a keydown event.

The active scanning is identical to that done in full scan mode except that return status is read from the external buffer connected to the D[7:0] pins and the SCAN signals are taken to a high-impedance state once the scan process is complete.

Configuring KCU for Partial Scan Mode

Partial scan mode is selected by setting bit D2, SCANMD, of the Keyboard Scan Enable Register to 1.

10.6 Related Registers

Table 10-4. Keyboard-Related Registers

Register	Address
PC/XT Compatible PPIA Keyboard Data Register	I/O address 060H
PC/XT Compatible PPIB Keyboard Control Register	I/O address 061H
PC/XT Compatible PPIC Keyboard Control Register	I/O address 062H
Keyboard Scan Enable Register	Index 66H
Scan NMI Control and Status Register	Index 67H

See also: Scan Control registers; Return Status Registers; GPIO Group Registers.

11 Serial I/O

11.1 Introduction

This chapter describes the VG330's Serial I/O functions. The SIO supports both standard serial I/O and infrared communication data formats for bits. It also is designed to assist in power saving operation and has the ability to power down automatically after a period of inactivity.

11.1.1 Capabilities

General Features

- Uses an industry-standard 16450-compatible UART
- Supports the HP Serial Infrared Interface (HP SIR)

Configuration

- Programmable address range
- Programmable interrupt number 3, 4, or 7
- Dedicated SIO TXD and RXD can be programmed for either HP-SIR conditioning or standard serial I/O
- GPIO pins can also be programmed for either infrared or standard serial I/O, allowing a VG330 to provide both infrared I/O or standard serial I/O without using additional external hardware to switch from one to the other.

Power-Saving Features

- Can be programmatically powered down
- Can automatically power down after a user-defined period of inactivity

11.2 SIO Architecture

Figure 11-1 shows a block diagram of the SIO subsystem.

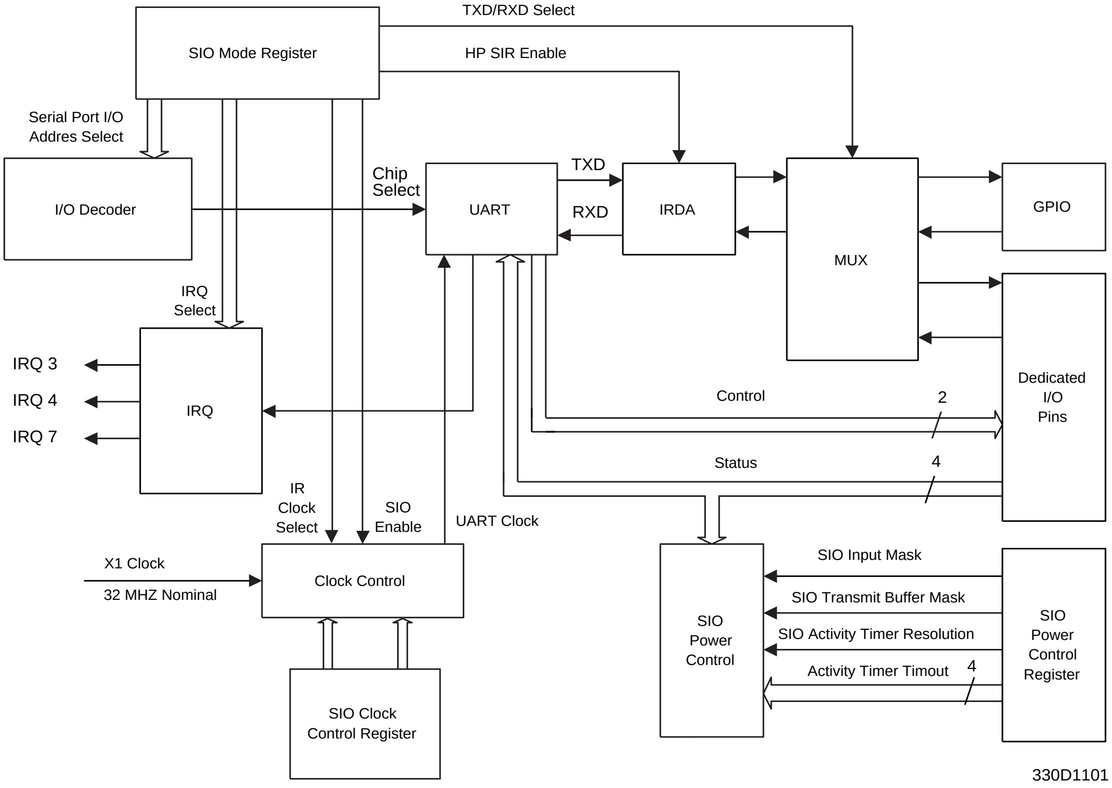

Figure 11-1 SIO Block Diagram

11.2.1 Related Pins

Symbol	Type	Pin No.	Description	Group
$\overline{\text{CTS}}$	I	34	Clear To Send	Status
$\overline{\text{DCD}}$	I	36	Data Carrier Detect	Status
$\overline{\text{DSR}}$	I	35	Data Set Ready	Status
$\overline{\text{DTR}}$	O	44	Data Transmit Ready	Control
$\overline{\text{RI}}$	I	32	Ring Indicator	Status
$\overline{\text{RTS}}$	O	45	Request To Send	Control
RXD	I	33	Receive Data	Data
TXD	O	46	Transmit Data	Data

Note that GPIO pins can be programmed to route standard serial and IR-formatted serial signals into and out of the VG330. For details, refer to Chapter 12, *GPIO*.

11.3 SIO Addressing and Interrupts

11.3.1 Addressing

The Serial Port is based upon an internal 16C450- compatible UART. Use the SPSEL bits of the SIO Mode Register at Index 10H to program the SIO to use one of the following PC I/O address ranges:

- 2E8H to 2EFH
- 2F8H to 2FFH
- 3F8H to 3FFH

11.3.2 Interrupts

Use the SIRQS bits of the SIO Mode Register at Index 10H to program the SIO to use one of three interrupt channels:

- IRQ3
- IRQ4
- IRQ7

The assignment of interrupts is controlled independently of I/O port address. An interrupt is generated when the receive buffer is full or when there is a change in the UART status.

11.4 General Operation Discussion

This section discusses routing and processing options for serial signals.

11.4.1 Processing Options

The VG330 can be configured to provide either standard serial I/O processing or signal conditioning that is appropriate for infrared signals using the HP-IR (HP-SIR) standard.

HP-IR Processing

The SIO Mode Register at Index 10H enables and disables applying signal conditioning for infrared data transmission to the serial data. If SIO Mode Register bit 5, HPIREN, is set to one, the signal from the UART is converted into the 3/16 modulation form necessary for the HP-SIR standard. Incoming data is converted from a 3/16 modulation scheme to normal serial data.

Standard Serial Processing

If HPIREN = 0, the UART signal passes through the IRDA Control Block without modification and is treated as a normal serial signal.

11.4.2 Routing Options

Serial signals can be routed either through dedicated serial pins or through GPIO pins assigned for that purpose.

The SIO Mode Register at Index 10H also controls routing of the serial signals. When serial data is routed through the GPIO block, the programmer must assign a pair of GPIO pins to these signals.

A multiplexer in the SIO block is connected to both the dedicated SIO pins and the GPIO block. Serial data can be routed to/from either of these destinations.

Either HP_IR-conditioned signals or standard serial signals can be placed on either the dedicated SIO pins or the GP_SIO pins. The following sections discuss each of the four design cases.

11.5 Standard Serial I/O Operation

A design may use standard serial I/O through the dedicated TXD and RXD pins. No other routing is used nor is IR processing applied. This section describes that case.

To use just the dedicated SIO pins for standard SIO:

1. Set SIO Mode Register SIOENA bit D7 to 1 which enables serial port use.
2. Clear bit 4 of the SIO Mode Register to 0. This switches TXD and RXD to the dedicated pins (as opposed to routing them through the GPIO block).
3. Clear SIO Mode Register bit 5, HPIREN, to 0 to remove IR signal conditioning from the processing path.

The standard SIO signals will then be applied to the TXD and RXD pins:

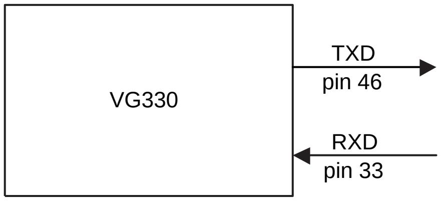

Figure 11-2 Standard Serial I/O on Dedicated Pins

11.6 IR-Conditioned Serial I/O

To implement HP-IR signal conditioning on the serial lines, and routed through the dedicated serial I/O pins, the system design must drive an IR transmitter diode driver from the TXD pin and provide an IR diode receiver circuit as source for the RXD pin.

To use just the dedicated SIO pins (but no GPIO pins) for IR-conditioned serial I/O:

1. Set SIO Mode Register bit D7, SIOENA, to 1 which enables serial port use.
2. Clear bit 4 of the SIO Mode Register to 0. This switches TXD and RXD to the dedicated pins (as opposed to routing them through the GPIO block).
3. Set SIO Mode Register bit 5, HPIREN, to 1 to enable IR processing on the serial signals.

The serial signals will then be conditioned for IR and will be applied to the TXD and RXD pins:

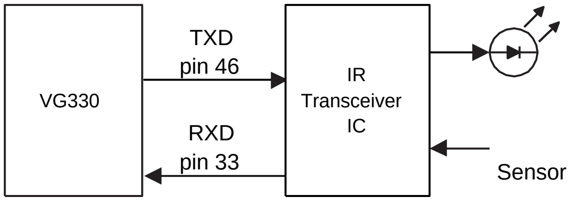

Figure 11-3 Serial I/O Using Dedicated Pins and IR Conditioning

11.7 Using Both Standard Serial I/O and IR-Conditioned I/O

In certain situations it may be desirable to allocate separate serial and infrared signal lines, with the internal UART then switched between the standard serial device I/O lines and the IR I/O devices. This configuration prevents standard serial devices from being confused when communicating with IR devices due to the IR specific communication protocol. It also prevents activation of the IR LED(s), thereby saving power during communication with standard serial devices.

To Implement two sets of serial I/O lines, it is necessary to assign GP_TXD and GP_RXD functions to two of the general purpose I/O pins. For programming details see Chapter 16, *Registers* and also Chapter 12, *GPIO*.

Once that is implemented, there are two design alternatives:

Using Dedicated Pins with Standard Serial I/O and GPIO Pins with IR I/O

The dedicated TXD/RXD pins can be used for normal serial I/O, and the GPIO pins for infrared:

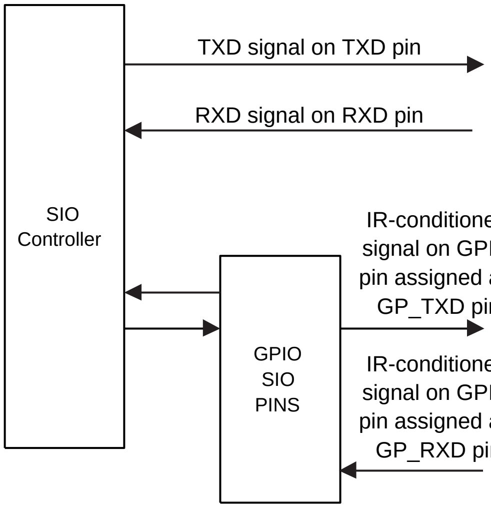
TXD signal on TXD pin
RXD signal on RXD pin
SIO Controller
IR-conditioned signal on GPIO pin assigned as GP_TXD pin
GPIO SIO PINS
IR-conditioned signal on GPIO pin assigned as GP_RXD pin

Figure 11-4 Using Dedicated Pins with Standard Serial I/O and GPIO with IR I/O

The programmer then must provide a means of switching (rerouting) between using the TXD/RXD pins when needed, or else activating the GP_RXD/TXD pins when needed.

The following are programming values used to switch between the above routings:

	SIO Mode Register (Index 10H)	
Pins	**Bit 4 TXDSEL**	**Bit 5 HPIREN**
To route to Dedicated Pins	0	0
To route to GP Pins	1	1

Using Dedicated Serial I/O Pins with IR-Conditioning and GPIO Pins with Standard Serial I/O

Alternatively, the dedicated pins can be used for IR, and the GPIO pins can be used for standard serial I/O:

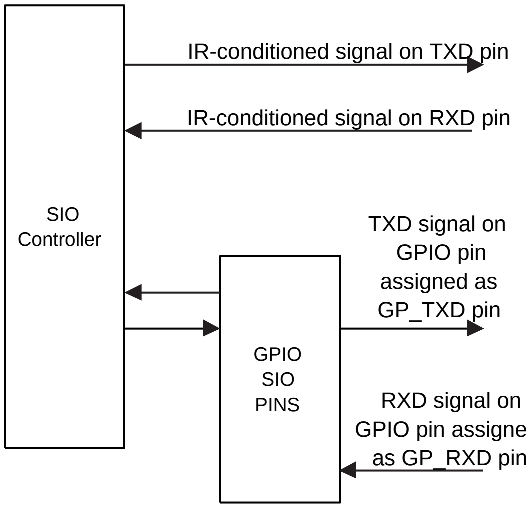
IR-conditioned signal on TXD pin
IR-conditioned signal on RXD pin
SIO Controller
TXD signal on GPIO pin assigned as GP_TXD pin
GPIO SIO PINS
RXD signal on GPIO pin assigned as GP_RXD pin

Figure 11-5 Using IR on the Dedicated Serial I/O Pins and Standard Serial I/O on the GPIO Pins

In this case, the programmer then must provide a means of switching between using standard serial I/O on the GP_RXD/TXD pins when needed, or else activating IR communication on the TXD/RXD pins when needed.

The following parameter values switch between these uses:

	SIO Mode Register (Index 10H)	
Pins	**Bit 4 TXDSEL**	**Bit 5 HPIREN**
To route to Dedicated Pins	0	1
To route to GP Pins	1	0

11.7.1 Additional configurations

The previous examples are the most practical configurations of Serial I/O that can be implemented without adding external hardware, other than level shifting or IR drivers. However, many other configurations are possible with the addition of external devices.

11.8 Power Management of SIO

The SIO block provides its own power management in addition to the PMU’s power management for the entire system. The SIO has three power-managed operating states. The Serial Port SLEEP State may be triggered independently of the System power management control.

An internal activity timer monitors accesses to the serial port transmit buffer and/or serial inputs and may automatically stop the serial port clock to achieve SIO SLEEP mode. Table 11-1 shows the three serial port power states and their effects.

Table 11-1. Serial Port Power Management States Table

Mode	Entry to State	Exit from State	Status
ON	Programmatically achieved	Timer causes SLEEP	Full operating condition
SLEEP	Timer causes entry	Wakes up upon write to Transmit Buffer and/or Activity on Serial Port Inputs, if these events are enabled for this	Input clock is gated off
OFF	Programmatically achieved	Programmatically achieved	Input clock is gated off

The SIO block can be power-managed through use of two registers, the SIO Mode Register, and the SIO Power Control Register. The relevant bits and related elements are shown in Figure 11-6.

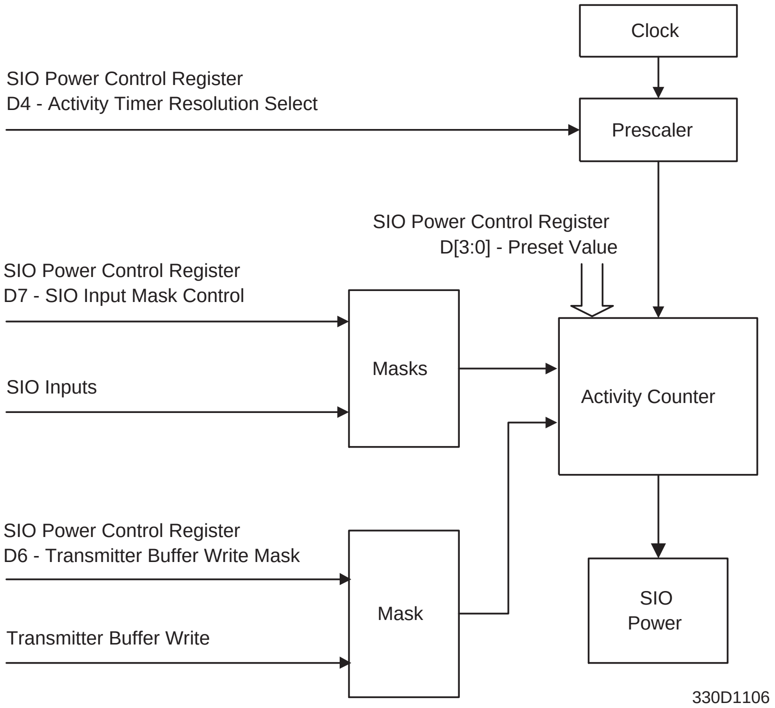
Clock
SIO Power Control Register
D4 - Activity Timer Resolution Select
Prescaler
SIO Power Control Register
D[3:0] - Preset Value
SIO Power Control Register
D7 - SIO Input Mask Control
Masks
SIO Inputs
Activity Counter
SIO Power Control Register
D6 - Transmitter Buffer Write Mask
Mask
Transmitter Buffer Write
SIO
Power
330D1106

Figure 11-6 SIO Power Management Control

11.8.1 Powering SIO ON/OFF

The SIO can be programmatically powered down (SIO OFF State) by clearing bit D7 of the SIO Mode Register to zero. This disables the UART by gating off its clock, and it frees the interrupts to be used for other devices.

11.8.2 Activity-Based Power Control of SIO

The SIO also can automatically power down to a SLEEP state after a user-defined period of inactivity. This operates as follows: the SIO Activity Timer, when enabled, continuously counts down from a preset value. When it reaches zero, the SIO is powered down and enters SLEEP state. However, when activity is detected, the SIO awakens and enters the SIO ON state.

This is controlled by the SIO Power Control Register. Its bit fields are listed in Table 11-2.

Table 11-2. SIO Power Control Register Bits

Bit	Name	Function
D7	INPMSK	Enables/disables having any change in SIO inputs refresh the SIO Activity Timer. D7 = 0: If D7 is zero, any change to an SIO input will refresh the activity timer. D7 = 1: If D7 is 1, an input to the SIO is masked and has no effect on the activity timer.
D6	TXDMSK	Enables/disables having any change in SIO transmit buffer refresh the SIO Activity Timer. D6 = 0: If D6 is zero, a write to the transmit buffer causes a refresh of the activity timer. D6 = 1: If D6 is one, a write to the transmit buffer has no effect on the activity timer.
D4	TCLKSEL	D4 controls the activity timer resolution. D4 = 0: If D4 is zero, the activity timer can be set to expire in a range of 1 to 15 seconds. D4 = 1: If D4 is one, the activity timer can be set to expire in a range of 8 seconds to two minutes.
D[3:0]	TMO	D[3:0] sets the activity time preset value. This value is loaded into the SIO activity timer when the timer is refreshed.

11.9 Related Registers

Table 11-3. Serial I/O-Related Registers

Register	Address or Index
UART registers	Address ranges: 2E8H to 2EFH 2F8H to 2FFH 3F8H to 3FFH
SIO Clock Control Register	Index 0FH
SIO Mode Register	Index 10H
SIO Power Control Register	Index 11H

12 GPIO

12.1 Introduction

This chapter discusses the VG330's GPIO function block, which provides configurable I/O pins. This chapter discusses the nature of the GPIO pins, describes the signals and functions available for routing to these pins, and identifies programming and design considerations.

12.1.1 Capabilities

The VG330 has 24 GPIO pins which provide highly flexible configuration of I/O lines.

- The GPIO pins are separated into three 8-bit GPIO pin groups
- Each GPIO pin offers up to 4 input configurations and 4 output configurations

Definition of the function of each GPIO pin is performed using corresponding bits in the set of twelve GPIO configuration registers. For details, refer to the register descriptions in Chapter 16.

12.2 GPIO Architecture

Figure 12-1 shows the GPIO from the viewpoint of system control. The GPIO pins are separated into three 8-bit GPIO pin groups named GPIOA[7:0], GPIOB[7:0], and GPIOC[7:0].

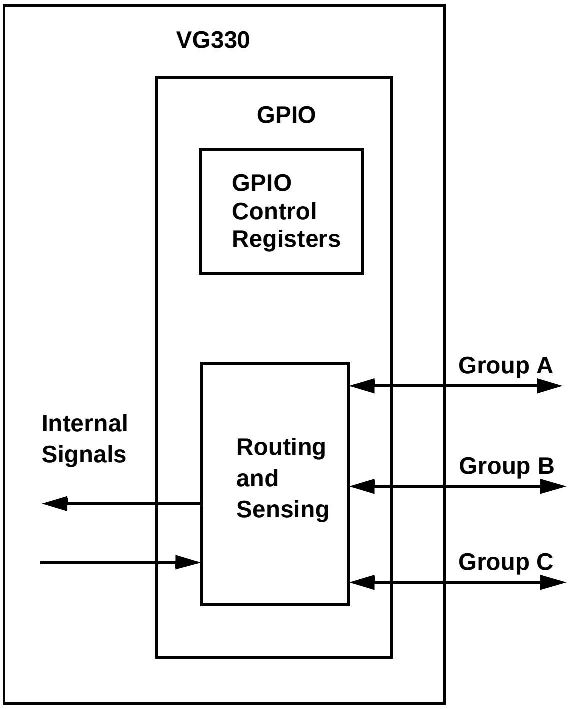

Figure 12-1 General Purpose Input-Output

12.2.1 Functions Available Through GPIO Pins

General-Purpose Input and Output

Each one of the GPIO pins may be configured to provide general purpose input or output capabilities. When a pin is configured as general purpose output, a value written to any GPD data bit in the corresponding GPIO register appears on its respective GPIO pin. When a pin is configured as general purpose input, a value driven on the GPIO pin can be read from its respective GPD data bit.

Routing of Internal Signals Through GPIO

Additionally, certain VG330 internal signals can be selected to be routed through GPIO pins. This capability is provided for maximum flexibility in system design without having the burden of too many package pins. For example, the keyboard functions for matrix scanning are designed to be routed through GPIO pins, rather than requiring many dedicated package pins.

Table 12-1 identifies the internal signals that can be routed in this way. Chapter 2 contains signal descriptions for these internal signals.

The GPIO pins are configured using the GPIO Mode registers which are accessed at register indexes 50H through 5BH. For more information, refer to Chapter 16, *Registers*.

LB2 Signal Available Through GPIO

The GPIO pins can be used to convey into the VG330's PMU a caution signal, LB2, telling of battery-low conditions. Normally, the VG330 default operating capability provides a single level of battery monitoring using the LB1 pin LB1 is intended to convey into the chip a 'battery failure imminent' warning).

However, the VG330 also supports a second, lower priority level of battery sensing, using a GPIO pin configured as the LB2 input. Typically, LB2 would be used to generate an NMI to inform the system that battery failure is approaching. System software would then perform an immediate SUSPEND.

12.3 Related Pins

Table 12-1. GPIO Pin Mapping Options

Mappable Signal	I/O Type	GPIO Group C Pin								GPIO Group B Pin								GPIO Group A Pin							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
IRQ15 / IRQ7	I							■								■							■		
IRQ14 / IRQ6	I						■								■							■			
IRQ13 / IRQ5	I					■								■							■				
IRQ12 / IRQ4	I				■								■							■					
IRQ11 / IRQ3	I			■								■							■						
IRQ10	I		■								■							■							
IRQ9 / IRQ1	I	■								■							■								
$\overline{\text{IOCS16}}$	I				■											■				■				■	
$\overline{\text{MEMCS16}}$	I					■											■				■				■
KBCLK	I																	■							■
KBDAT	I																		■					■	
LB2	I	■					■				■		■		■		■					■			
GP_RXD	I		■					■		■		■		■									■		
RET	I	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI	I	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
SYSCLK	O	■								■								■				■			
$\overline{\text{BHE}}$	O		■								■								■				■		
$\overline{\text{CRDMOE}}$	O	■																							
$\overline{\text{CRDMWE}}$	O		■																						
CA22	O			■																					
CA21	O				■																				
CA20	O					■																			
PCS0	O							■				■			■					■					
PCS1	O						■				■			■			■		■						■
PCS2	O					■				■			■					■						■	
CRD_ALE	O								■																
M	O								■												■		■		
GP_TXD	O			■									■		■		■								
SCAN	O	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO	O	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■

Note: Black cells in table show where a signal in Mappable Signal column can be mapped through a GPIO pin. Example: Keyboard SCAN signal 22 can be mapped as an output through GPIO Group C pin 6. KBCLK signal can be mapped as an input through GPIO Group A pin 7 or through pin 0.

12.4 Programmable Chip Selects

Up to three programmable chip selects are available on the GPIO pins. Programmable chip selects are available in all of the GPIO pin groups.

Each chip select has the following capabilities:

- It may be defined as either I/O or memory
- It supports 8 bit or 16 bit cycles (data size may be specified)
- An 8-bit start address and an 8-bit end address may be specified for the range the chip select will recognize
- The select may be qualified as to whether it is address-only, Read, or Write
- Each programmable chip select supports NMI trapping for device emulation, device monitoring, and so on. NMI can be generated during read, write, or both reads and writes to the chip select range.

These capabilities are described in the following paragraphs.

12.4.1 I/O Decoding

For I/O decoding, the start and stop addresses correspond to system addresses A[7:0] and the base address corresponds to A[15:8]. This permits a minimum I/O decode range of 1 byte and a maximum of 256 bytes.

The programmable chip selects are configured for I/O addresses by specifying an 8 bit start address, an 8 bit stop address, and an 8 bit base address.

12.4.2 Memory Decoding

For memory decoding, the start and stop addresses correspond to system addresses A[15:8] and the base address corresponds to A[19:16]. This permits a minimum memory decode range of 256 bytes and a maximum of 65536 bytes.

The programmable chip selects are configured for memory addresses by specifying an 8 bit start address, an 8 bit stop address, and an 8 bit base address.

12.4.3 Data Width Selection

Data width may be selected using the PCS Mode Registers. For details, see register descriptions.

12.4.4 Address Range Selection

In addition to the three programmable chip selects, there is a fourth programmable chip select called the Alternate Programmable Chip Select that can be linked to any one of the primary three. In this way, two separate address ranges can be used to determine generation of one chip select. The APCS is described in Chapter 16 through registers at Index numbers 2CH through 2FH.

12.4.5 Type Definition

Chip selects may be qualified with read or write strobes or may be defined as address decode only.

For details, see descriptions in Chapter 16 of the PCS Mode Registers.

12.5 Interrupts and the GPIO Pins

The VG330 provides two dedicated steerable interrupt input pins, IRQA and IRQB. Additional interrupts may be supported via the GPIO pins. Up to 7 additional interrupt inputs are supported. These inputs may be configured to be one of the following primary or secondary interrupts:

Primary IRQ	Secondary IRQ
IRQ15	IRQ7
IRQ14	IRQ6
IRQ13	IRQ5
IRQ12	IRQ4
IRQ11	IRQ3
IRQ10	N/A
IRQ9	IRQ1

The VG330 does not internally resolve interrupt conflicts. It is the responsibility of the system software to assure that GPIO interrupt assignments do not conflict with internal interrupting sources. Interrupt inputs are available in all of the GPIO pin groups.

Table 12-2 lists interrupts for which dedicated use is made within the VG330:

Table 12-2. Dedicated IRQs

IRQ	Internal Devices
IRQ0	timer 0
IRQ1	keyboard
IRQ3	serial
IRQ9	RTC

12.6 16 bit ISA Bus Support

To support external 16 bit I/O or memory devices, certain GPIO pins may be configured to output the byte high enable signal, $\overline{\text{BHE}}$, and also accept the $\overline{\text{IOCS16}}$ and/or $\overline{\text{MEMCS16}}$ inputs.

During external I/O or memory cycles, the VG330 will generate 16 bit cycles if the selected device responds with either $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$. The ISA bus clock, SYSCLK, may also be output on certain GPIO pins. 16-bit ISA bus support is available in each of the GPIO pin groups.

12.7 Power Management and the GPIO Pins

During SUSPEND, all GPIO pins are driven low.

12.8 Keyboard Functions and GPIO

The operation of the Keyboard Controller Unit is primarily described in Chapter 10, *Keyboard Controller Unit*. However, since that functional block operates in conjunction with the GPIO block, overlapping areas of operation are discussed here.

The VG330 supports both a PC/XT serial keyboard interface and a scanned keyboard matrix. Either or both interfaces may be independently enabled on GPIO pins.

The keyboard scanner offers complete flexibility when configuring for a particular keyboard matrix. Any one of the GPIO pins may be defined as either SCAN (three-state output) or RETURN (active low input).

The keyboard scanner is intended to interface to a normally open switch matrix, using a design as follows:

- External pull-up resistors hold the return inputs at a high level while all switches are open.
- The scan signals are three-state outputs which become low driven when enabled. Any key depressed while all scan outputs are enabled will cause one of the return lines to go low.
- A key press generates an NMI to inform the BIOS that a key has been depressed.
- The BIOS enables a programmable timer in the keyboard scan logic which generates a periodic NMI so that the BIOS may scan the keyboard for the depressed key and perform software debouncing.
- When the keyboard input has been received, the BIOS returns all the Scan lines to their low state, translates the key input into an XT scan code and writes this scan code to the keyboard data register at I/O address 60H, and then calls the keyboard handler.

12.8.1 Keyboard Interface

The GPIO pins support using either of two types of keyboard interfaces:

The first type is a standard XT serial keyboard interface using bi-directional Keyboard Clock and Keyboard data pins, KBCLK and KBDAT.

The second type uses scanning of a keyboard matrix using Scan and Return pins.

The XT serial keyboard interface may only be enabled on select pins in the GPIO pin group A.

For keyboard scanning, each one of the GPIO pins may assigned as either a SCAN output or RETURN input. The VG330 supports two types of keyboard scanning. In the first case, the VG330 is directly connected to the keyboard matrix via the SCAN and RETURN signals. In the other case, the VG330 only provides the SCAN signals for the keyboard matrix and the RETURN status is read from the external D[15:0] data bus.

In the default configuration the VG330 utilizes both SCAN and RETURN signals to communicate with the keyboard matrix. Software sets all SCAN lines low when the keyboard is idle and the RETURN lines are externally pulled to VCC using a resistor network.

When any key is pressed, one or more RETURN lines will be driven low causing an NMI to be generated. After receiving the NMI, software begins scanning the keyboard by first bringing all SCAN lines to a high impedance state, then selectively enabling individual SCAN lines to be driven low.

After the location of the key has been determined and the system has been notified that keyboard input is available, software sets all SCAN lines back low and waits for the next key press.

In the alternate configuration, external three-state buffers such as those in a 74LVT244 are utilized for reading the RETURN lines from the keyboard matrix. One of the programmable chip selects must be reserved for decoding of the I/O address where the RETURN status will be read and should be configured as I/O read qualified. This chip select output can then be directly connected to the enable pins of the external 244 buffers.

This configuration has the advantage of freeing up more GPIO pins for use as other functions. The SCAN lines are externally pulled low using large value resistors, typically 47K Ohms. The RETURN lines are pulled to VCC by much smaller value resistors, typically 4.7K Ohms.

The VG330 keyboard controller then monitors the status of the SCAN lines and generates an NMI to inform the system of a key press when any one of these SCAN lines are set high. Software then searches for the depressed key by selectively driving each SCAN line low while bringing the others to a high impedance state, pulled to VCC by the smaller value resistors.

12.9 Serial Infrared Interface and GPIO

Serial infrared communication is supported by the VG330. Signal conditioning appropriate for infrared-specific applications may be enabled for the standard UART transmit and receive pins, TXD and RXD, or for GPIO pins configured as GP_TXD and GP_RXD.

In certain situations it may be desirable to allocate separate serial TXD/RXD and infrared GP_TXD/GP_RXD signals with the internal UART ‘multiplexed’ between interfacing to a standard serial device and the IR LEDs. This configuration prevents standard serial devices from being confused when communicating with IR devices due to the IR-specific communication protocol. It also prevents activation of the IR LEDs, which saves power during communication with standard serial devices.

See also the discussion in Chapter 11, *Serial I/O*.

12.10 PC Card Buffering

The VG330 supports direct connection to a PC Card slot for many of the PC Card interface signals. However, external buffers are still required to provide address, data, and control isolation for “Hot Insertion” and power management of the PC Card slot and to minimize loading of these buses.

The GPIO group C pins may be configured as dedicated PC Card interface signals. These interface signals do not require external buffering and therefore may be connected directly to the PC Card slot. When these PC Card interface signals are enabled, one three-state buffer IC can be eliminated for the PC Card slot.

The following PC Card interface signals may be assigned to the GPIO pins:

- PC Card address bits, A[22:20]
- PC Card memory command strobes, $\overline{\text{CRDMOE}}$ and $\overline{\text{CRDMWE}}$

In addition to providing selected PC Card interface signals, the GPIO can also be configured to support external PC Card interface buffering using three-state transparent latches in place of three-state buffers. The CRD_ALE signal for driving these latches can be conveyed out through GPIO pin C0 as shown in Table 12-1. This configuration has the advantage of lowering overall system power consumption since PC Card addresses are only activated during accesses to the cards themselves. When the card is not being accessed, the PC Card address bus is latched and held static.

12.11 Related Registers

Table 12-3. GPIO-Related Registers

Register	Index
GPIO Group A Mode Register 1	50H
GPIO Group A Mode Register 2	51H
GPIO Group A Mode Register 3	52H
GPIO Group A Mode Register 4	53H
GPIO Group B Mode Register 1	54H
GPIO Group B Mode Register 2	55H
GPIO Group B Mode Register 3	56H
GPIO Group B Mode Register 4	57H
GPIO Group C Mode Register 1	58H
GPIO Group C Mode Register 2	59H
GPIO Group C Mode Register 3	5AH
GPIO Group C Mode Register 4	5BH
GPIO Group A Data Register	5CH
GPIO Group B Data Register	5DH
GPIO Group C Data Register	5EH
Scan Control A Register	60H
Scan Control B Register	61H
Scan Control C Register	62H
Return Status A Register	63H
Return Status B Register	64H
Return Status C Register	65H
Keyboard Scan Enable Register	66H
Scan NMI Control and Status Register	67H
Shadow XT Shift Register	68H

13 PC Card/ExCA Controller

13.1 Introduction

This chapter describes the PC Card function block in the VG330. For full details of PC Card controller behavior, refer to the Vadem VG365 Data Manual, document number M151016-02, or the data manual for the Intel 82365SL.

13.1.1 Capabilities

- The VG330 provides support for one PC Card 2.1/ExCA/JEIDA 4.2 PC Card socket.
- VG330 internal PC Card controller is fully register compatible with the industry standard Intel 82365SL.
- Additional PC Card sockets may be supported by attaching standard Vadem PC Card socket controllers, such as the VG465 or VG468, to the VG330 single-bus.

13.2 PC Card Controller Architecture

Figure 13-1 shows the PC Card Controller from the viewpoint of bus signals.

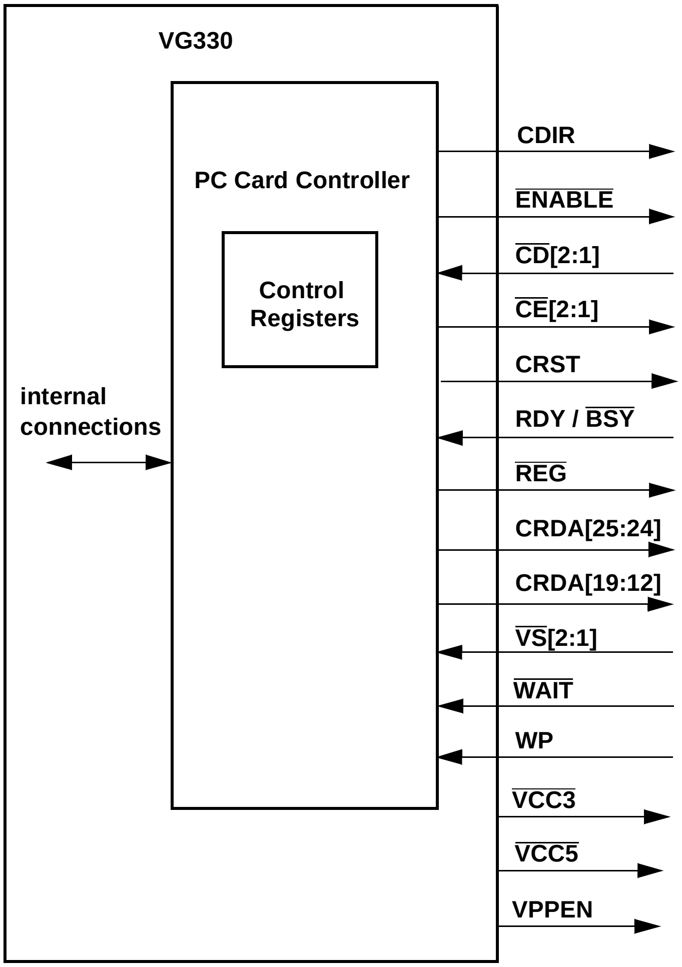

Figure 13-1 PC Card Interface in VG330

13.3 Related Pins

Table 13-1. PC Card-Related Signals and Pins

Pin or Signal	Function
$\overline{\text{CD}}$[2:0]	Card detect status inputs from PC Card socket.
CDIR	Direction control for PC Card Odd and Even Byte data buffers.
$\overline{\text{CE}}$[2:1]	Odd and even byte chip select signal to PC Card memory and I/O cards.
CRDA[25:24]	PC card address bits.
CRDA[19:12]	PC card address bits.
CRST	Reset signal for PC Card memory and I/O cards
$\overline{\text{ENABLE}}$	Enable for PC Card address/control buffers.
RDY / $\overline{\text{BSY}}$	Ready / $\overline{\text{Busy}}$ status input from PC Card memory card. May be redefined as $\overline{\text{IREQ}}$ for PC Card I/O cards.
$\overline{\text{REG}}$	Register select signal for PC Card memory and I/O cards.
$\overline{\text{VCC3}}$	Active low; enable for the 3 volt supply for the PC Card
$\overline{\text{VCC5}}$	Active low; enable for the 5 volt supply for the PC Card
VPPEN	Program voltage enable for PC Cards.
$\overline{\text{VS}}$[2:1]	PC card voltage sense inputs. (See Interface Register 1FH)
$\overline{\text{WAIT}}$	Extend bus cycle for PC Card cards.
WP	Write protect input from PC Card memory cards. May be redefined as $\overline{\text{IOIS16}}$ for PC Card I/O cards.

13.4 Address, Data, and Command Buffering

13.4.1 Address and Data Handling

The address and data of the PC Card socket requires external buffers to minimize loading and to support power management of the PC Card socket, including mixed voltage use.

The VG330 PC card address bits, CRDA[25:24] and CRDA[19:12] support direct connection to the PC Card socket. The upper memory address bits, A[23:20] may be enabled on an individual pin basis to directly drive the PC Card socket if these bits are not required for either system RAM or ROM. Additional direct connection address options are available on the GPIO pins. Refer to Chapter 12, *GPIO*, for details.

All VG330 address pins shared between any other peripheral or memory device and the PC Card socket are required to be buffered using a 74LVT244 type three-state buffer. The enable for the three-state address buffer is controlled by the VG330 $\overline{\text{ENABLE}}$ pin.

Data buffering for the PC Card socket always requires a pair of 74LVT245 or equivalent bi-directional three-state buffers. The direction control is provided by the CDIR pin of the VG330. The Enables for the data buffers may be provided by the $\overline{\text{CE}}$[2:1] pins. $\overline{\text{CE}}$[2:1] must be externally buffered before connecting to the PC Card socket.

Refer also to the discussion: *PC Card Buffering* on page 12-7 of Chapter 12, *GPIO*.

13.4.2 Command Signal Handling

PC Memory Cards may be controlled by Expansion bus $\overline{\text{SIORD}}$, $\overline{\text{SIOWR}}$, $\overline{\text{SMRD}}$, and $\overline{\text{SMWR}}$ signals. In this configuration, the ISA Expansion bus command strobes must be buffered to support hot insertion and power management of the PC Card socket.

Optionally, the VG330 allows PC Card memory strobes to be output on the GPIO pins. GPIO pins may be configured to directly drive the PC Card socket with memory command strobes. These command strobes do not require external buffering and are driven to a high impedance state when the PC Card socket is unpowered.

See also the discussion: *PC Card Buffering* on page 12-7.

Command buffering of $\overline{\text{SMRD}}$ and $\overline{\text{SMRW}}$ is required if GPIO pins are not assigned to provide direct connection to the PC Card socket. Command strobe buffering is identical to address buffering and is enabled by the VG330 $\overline{\text{ENABLE}}$ pin.

13.5 PC Card Memory Mapping

This section discusses the PC Card Controller memory mapping and CRDA[25:24] and CRDA[19:12] pin functions.

The PC Card controller provides its own memory mapping functions, which are compatible with the Intel ExCA architecture.

ExCA memory mapping is similar to LIM 4.0 EMS mapping in that memory windows are defined in the V30MX address space between A0000h and EFFFFh which allow the portions of 64 MByte PC Card address space to paged into these windows.

The ExCA architecture defines a minimum memory mapping window size of 4 KBytes, which requires that 14 of the 26 PC Card address bits be mappable. Of the 14 mappable PC Card address bits, the VG330 provides 10 dedicated address pins, CRDA[25:24] and CRDA[19:12], and the remaining four are shared with other functions connected to the VG330 A[23:20] address pins. The least significant 12 address bits of the PC Card address are not mappable and are shared with the A[11:0] pins.

The VG330 also allows some PC Card address bits to be output on GPIO pins. Refer to Chapter 12's discussion of GPIO for details on configuring GPIO pins to support this function.

Figure 13-2 illustrates a typical PC Card connection to the VG330.

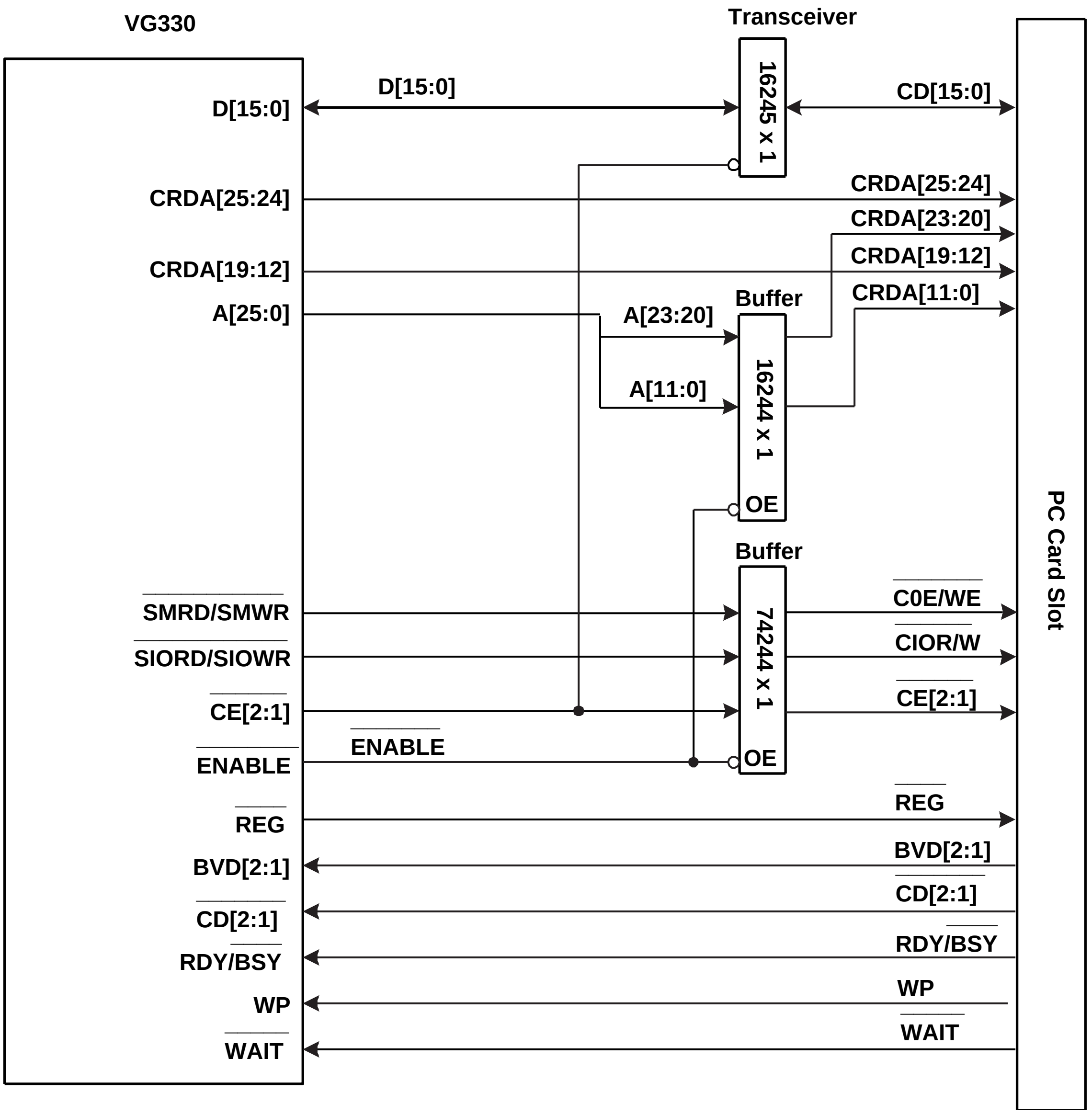

Figure 13-2 PC Card Connection to VG330

13.6 Related Registers

Table 13-2. PC Card-Related Registers

Register	Address
PC CARD/ExCA Controller	3E0H for Index Register, 3E1H for Data Register
For other PC Card Registers, refer to Chapter 16.	

13.7 PCMCIA cycle timing

Table 13-3. PCMCIA Cycle Timing

Cycle Type	Cycle Duration
8 bit I/O	3 SYSCLK+ max of {Expansion I/O w.s. and WAIT signal active}
16 bit I/O	3 SYSCLK+ max of {Expansion I/O w.s. and I/O Window w.s. and WAIT signal active}
8 bit Memory	3 SYSCLK+ max of {Expansion Mem8 w.s. and WAIT signal active}
16 bit Memory	3 SYSCLK+ max of {Expansion Mem8 w.s.and Mem Window w.s. and WAIT signal active}

Note: Compatible 365SL timing for 8 bit cycle types are set when Expansion I/O w.s. is ≥ 3 and Expansion Mem8 w.s. is ≥ 3.

14 Power Management Unit

14.1 Introduction

This section discusses the Power Management Unit. It provides the following:

- Introduction to the PMU and overview of its use.
- Describes the PMU's main functional elements.
- Describes the PMU's operating environment.
- Lists and discusses the PMU-related pins on the VG330.
- Lists and discusses the power-management states of the PMU.
- Discusses the power states of the VG330.

14.1.1 Main Capabilities of PMU

- Controls running the CPU clock at normal speed or at slow speed
- Provides output pins for external power switches for various devices
- Monitors various system activities so as to provide a basis for deciding which power management state to enter.

14.1.2 PMU Overview

The VG330 Power Management Unit, or PMU, provides hardware that can assist in managing system elements with power conservation as a goal.

Power management provides a means for managing both internal and external device power. The VG330's Power Management Unit, or PMU, contains programmable and automatic mechanisms for monitoring system activity and controlling the nature of power usage.

The PMU provides several levels of power control for the rest of the VG330 and outside devices. Activity timers monitor the system and may automatically reduce the processor clock rate or generate an NMI to inform system software that the system is idle.

The PMU supports five power management states for the system that uses a VG330: ON, DOZE, SLEEP, SUSPEND, and OFF. These are outlined in Table 14-1.

Table 14-1. Power Management Mode Usage

MODE	MAJOR CHARACTERISTICS	GRANULARITY/TIME DOMAIN
ON	Runs all system operations at full speed and enables all activities	na
DOZE	Slows down or stops the system clock to reduce power use	The PMU DOZE Timer Register at index CCH has time-outs in the seconds range.
SLEEP	Usually used to shut off the display	The PMU SLEEP Timer Register at index CDH has time-outs in the minutes range.
SUSPEND	Shuts off the system oscillator, thus reducing CPU power consumption; PMU assumes control of memory refresh; the real time clock still runs.	The PMU SUSPEND Timer Register at index CEH has time-outs in the minutes range.
OFF	Shuts off the system oscillator and only maintains the real time clock; memory refresh ceases; power usage is lowest of all states	

14.2 PMU Main Functional Elements

PMU Registers

The PMU registers allow control of the PMU functions, including timing values used by activity timing monitors, power pin control, and masking of detectable activities. The registers are summarized at the end of this chapter, and their various uses are discussed throughout the chapter.

State Timers

The PMU contains timers that allow the system to automatically enter power management states if no activity has been detected during the timer period.

Activity Monitor

The Activity Monitor is a mechanism that provides monitoring of various system activities. It allows whether an activity can trigger an interrupt or a state change, by means of programmable masks.

SmartClock

SmartClock continuously monitors system activity and attempts to quickly slow down or speed up the processor clock in response to changing system requirements. See “SmartClock” on page 18. of this chapter.

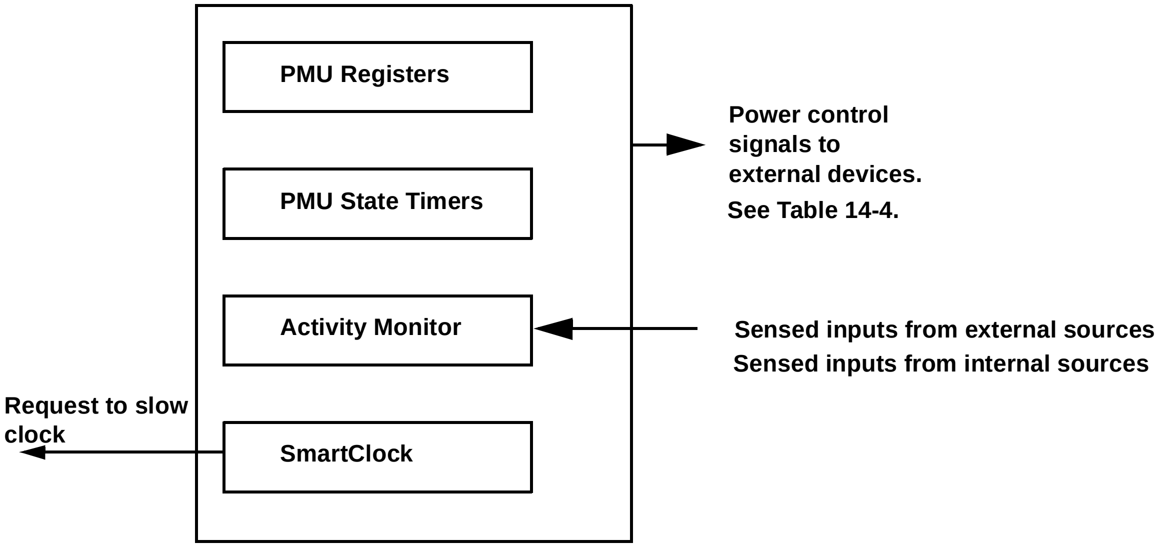
PMU Registers
PMU State Timers
Activity Monitor
SmartClock
Power control signals to external devices.
See Table 14-4.
Sensed inputs from external sources
Sensed inputs from internal sources
Request to slow clock

Figure 14-1 Main Elements in the PMU

14.3 Related Pins

This section lists the VG330 signals and pins related to power management. These signals and pins are discussed in detail in the next section.

Table 14-2. PMU-Related Signals and Pins

Pin Name	Signal Name	I/O Type	Pin No.	Voltage	Type	Current
EXT	-	I	158	3.3 V	CMOS Schmitt	
SYSPWG	-	I	153	3.3 V	CMOS Schmitt	
LB1	-	I	155	3.3 V	CMOS Schmitt	
(LB2 signal is routable through a GPIO pin)	LB2	Input signal[a]	see note below			
$\overline{\text{RI}}$		I	32	3.3 V	CMOS Schmitt	
$\overline{\text{RSTIN}}$	-	I	154	3.3 V	CMOS Schmitt	
VPBIAS	-	O	48	3.3 V	CMOS Three-state	3 mA
VPLCD	-	O	49	3.3 V	CMOS Three-state	3 mA
VPRAM	-	O	156	3.3 V	CMOS	3 mA
VPSYS	-	O	157	3.3 V	CMOS	3 mA

[a] See GPIO description in Chapter 12, *GPIO*, for more information on configuring a GPIO pin to convey this signal into the VG330.

14.4 PMU Operating Environment

This section describes the relationship of the PMU to the rest of the system.

In general, the PMU conserves power by slowing down or stopping clocks, by turning off the main CPU oscillator, and by controlling power to the system logic, LCD, and memory. It does this using both programmable parameters and by use of sensing mechanisms designed into the hardware. The Activity Monitor provides guiding information; the SmartClock causes changes in system clock speed to vary power use.

14.4.1 PMU Connectivities

The VG330's PMU monitors internal activities of the chip, and can control certain internal items and external items. The following discusses internal and external connectivities.

14.4.2 Activities Monitorable by the PMU

The PMU can monitor some internal activities of the VG330 and some external activities such as keyboard input, I/O ports, certain pins, and so on. Monitoring can be configured under program control. This section describes these capabilities.

Monitor for System Activities

The activity monitor provides the PMU with information about system activity. The PMU uses this information as one source of data governing when to change states. The activity monitor can monitor activity of the following PC I/O devices as described in Table 14-3 below.The VG330 also monitors the following input pins, which are described in the next section:

- External Input (EXT)
- SYSPWG
- $\overline{\text{RSTIN}}$ Pin
- Low Battery Input (LB1), and the LB2 signal, when LB2 is routed to a GPIO pin
- Modem Ring Indicator Input ($\overline{\text{RI}}$)

.

Table 14-3. Activities Monitored by PMU

Area	Region Monitored
Keyboard Port	I/O Reads to port 60H
Serial I/O COM1 COM2	I/O R/W access to COM1 and COM2 • 2E8H to 2EFH • 2F8H to 2FFH • 3E8H to 3EFH • 3F8H to 3FFH
Hard Disk	I/O R/W access to hard disk • 3F6H - 3F7H • 1F0H - 1F7H
Video Memory Access	Writes to video memory
ExCA	I/O accesses to the PC Card controller. (See description of SmartClock Activity Mask register at Index DFH bit D2.)
Programmable I/O	I/O accesses to GPIO. (See description of PMU I/O Range Register (Index C5H) bit field IORNG.)

14.5 Control Inputs Monitored by PMU

The VG330 provides two classes of outside signal inputs for the PMU.

In this system, the VG330 provides two dedicated inputs, $\overline{\text{RSTIN}}$ and LB1, for monitoring or reacting to the status of the main battery source. In addition, a third battery-monitoring signal, LB2, is provided internally. LB2 is also a PMU input and can be connected to an outside signal by routing through a GPIO pin dedicated to the purpose.

External Input (EXT)

The EXT input is used to turn the system power on or off. This signal is typically connected to a momentary contact switch. The EXT input is internally debounced by the VG330 and can be directly connected to a mechanical switch. When the system is in the SUSPEND state and the EXT switch is low for more than 60 ms, and then becomes high, the VG330 will be placed into the ON state.

When the VG330 is in the ON, DOZE or SLEEP state, a positive transition on the EXT input after it has been low for 60 ms will cause an NMI to be generated, to inform the system that a request to power down has been received. The BIOS can place the system into the SUSPEND or OFF state.

Modem Ring Indicator Input ($\overline{\text{RI}}$)

The VG330 can be placed into the ON state from the OFF or SUSPEND state through the modem ring-in signal. The signal must be supplied as a TTL level signal and be a filtered square wave. The $\overline{\text{RI}}$ input is a positive edge triggered input. The VG330 will go into the ON state after the number of positive transitions on the $\overline{\text{RI}}$ line specified in the PMU Control Register (Index C2H). If the $\overline{\text{RI}}$ input is not used, the $\overline{\text{RI}}$ input should be tied high.

14.5.1 Power Supply Interface Input Pins

These input pins are used to monitor status of the main power supply and of the main sub-system.

The block level diagram in Figure 14-2 illustrates a typical VG330 interface to the power supply.

SYSPWG

This section discusses the relationship between VPSYS and SYSPWG in a design, and use of SYSPWG. See also the discussion of VPSYS under the heading *Voltage Control Output Pins* on page 7 of this chapter.

First of all, note that power must be supplied to the VG330 at all times, but other components are powered on or off as necessary. (Note that RAM may be powered in such a way, perhaps involving a backup battery, as to allow retaining data while the main battery is being changed.) In a typical system design, VPSYS is used to control SYSVCC, power for most components external to the VG330. VPSYS is asserted by the VG330 at the beginning of a resume sequence.

System designs must provide a means for detecting when SYSVCC is stabilized after VPSYS goes active. The System Power Good input pin, SYSPWG, tells the VG330 when system operating power is stabilized and that it is safe to start executing code. SYSPWG is active high.

Once SYSPWG is asserted, code execution begins after a delay period, Resume Delay, controlled by PMU RESUME Control Register, Index DDH. This period may be programmed as one of several preset values in the range 0 to 250 ms.

Resume Delay can be used in the following context. There are many ways to design a source for the System Power Good signal. One design approach might use a simple RC circuit with a comparator to generate SYSPWG and trigger the code execution. However, this inexpensive mechanism is not precise and might trigger resumption before power is stable. Therefore, to allow designers to provide a known delay after SYSPWG activation, Vadem provides programmable Resume Delay values.

System designs providing more elaborate voltage monitoring mechanisms may not need to use Resume Delay capability.

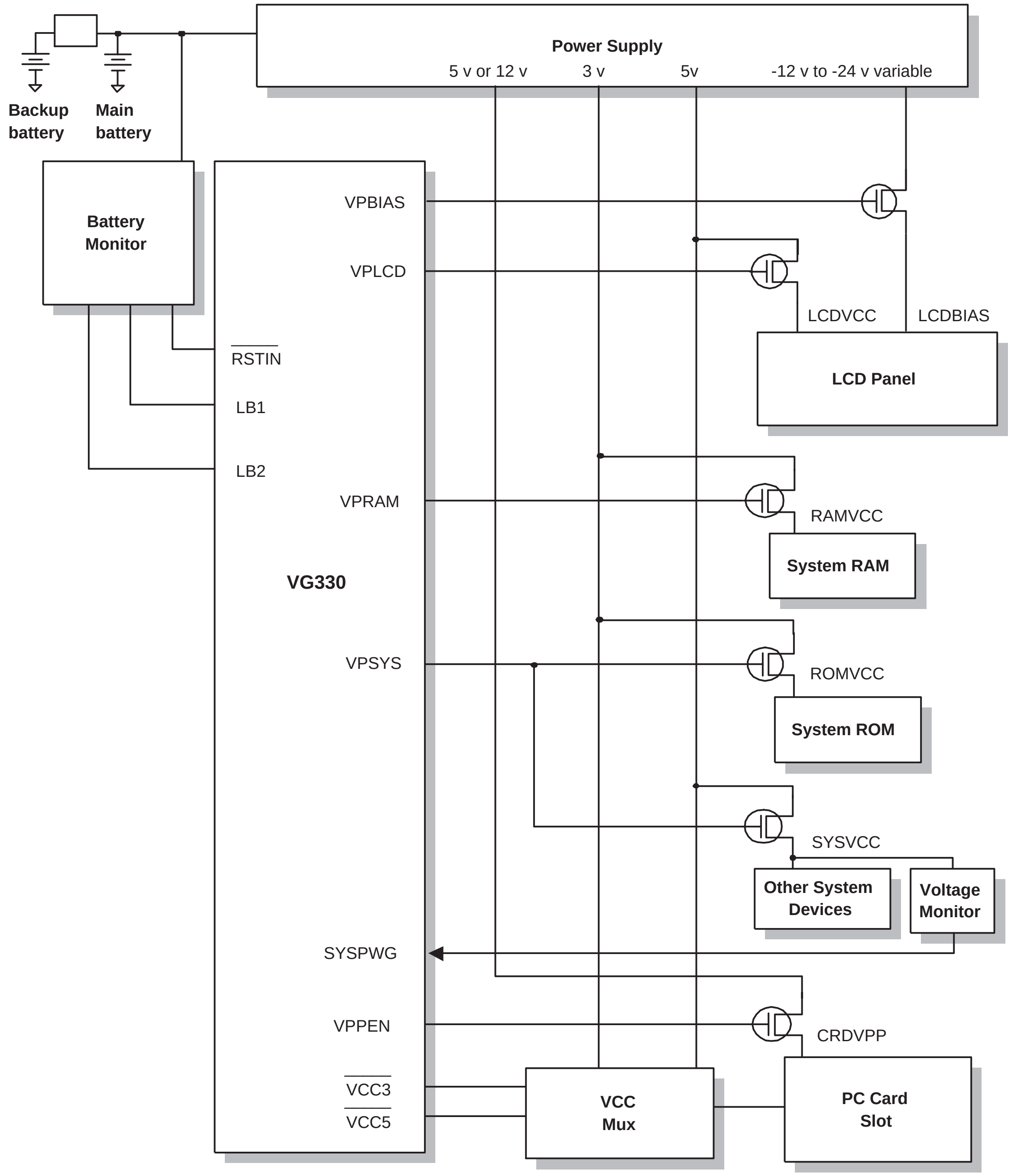

Figure 14-2 Power Control Pin Application

14.5.2 Battery Status Monitoring

$\overline{\text{RSTIN}}$ Pin

$\overline{\text{RSTIN}}$ is the main reset input to the VG330; when this input is driven low it causes the CPU and all registers and peripherals to be initialized to their default state. $\overline{\text{RSTIN}}$ is typically driven by a voltage supervisory circuit which asserts $\overline{\text{RSTIN}}$ when the main battery drops below a minimum operating threshold. $\overline{\text{RSTIN}}$ may also be driven by an external switch to cause a "hard reset" of the system following a system crash.

LB1 Pin and LB2 Signal

In addition to the internal VG330 activities that are monitored, the PMU also monitors inputs intended to be used by the system designer to track battery status.

The Low Battery Warning Input (LB1) is intended to be used to convey a signal from external circuitry monitoring the primary battery source for the approach of critical exhaustion. LB1 must be driven high by the external voltage-supervisory circuit to signal a low battery warning condition.

A second level of battery monitoring may be supported by defining one of the GPIO pins as LB2. LB2 is intended as a cautionary signal showing that power is getting low, but not necessarily that it is nearly exhausted. In this case the LB1 pin might be considered as an input warning of impending battery failure, whereas the GPIO pin defined as LB2 is used to indicate merely the need to replace batteries soon.

Note that use of LB2 depends on the VG330 being 'awake', and therefore it may be used only when the VG330 is not in SUSPEND or OFF modes. Also, since LB2 must be implemented on a GPIO pin, and GPIO pins are driven low during the SUSPEND state and the OFF state, LB2 must only be driven by an open collector driver.

A typical implementation for two levels of battery monitoring would be to signal the system of the low battery condition when LB1 was asserted and to either automatically SUSPEND the system or prompt the user to SUSPEND the system when LB2 was asserted.

Both the LB1 pin and the GPIO pin defined as LB2 can be used by the PMU to generate an NMI informing system software of low battery or very low battery conditions. The status of these pins may be read from bits D[3:2] of the PMU Status Register. Each low battery source has an associated NMI mask bit in the PMU NMI Mask register. NMI is enabled by clearing the appropriate NMI mask bit to 0. Status of NMI for both LB1 and LB2 can be read in the PMU NMI Status register.

For low battery NMI generation, LB1 and LB2 may defined as edge triggered inputs or they may be internally debounced by the VG330. To enable debouncing of the LB1 input and LB2 signal, the LBDBNC bit of the PMU Control register must be set to 1.

In this mode, LB1 or LB2 must remain active for at least 1 ms before they will be recognized by the VG330 and an NMI will be generated. When the LBDBNC bit is reset to 0, LB1 and LB2 are defined as edge triggered inputs and NMI is generated during a low to high transition on one of these pins.

The LB1 input is a standard TTL level input. To use LB1, it must be connected to the output of an external comparator circuit that supplies a low level signal as long as main battery condition is at a 'good' level.

14.5.3 Voltage Control Output Pins

The VG330 provides both a set of output pins and a set of input pins for managing external power sources. There are seven dedicated output pins for controlling the supply voltage of up to 4 external sub-systems. These pins are listed in Table 14-4, and an example of their application is shown in Figure 14-3. Related control registers are discussed in *Power Control Registers* on page 9 of this chapter.

The polarity of each power control bit is high true. Additionally, the polarity of VPLCD may be changed by programming bit D0 of the PMU Polarity register (Index CAH). This is primarily intended to simplify LCD power control logic.

After a hard reset, the VG330 automatically makes the VPLCD and VPBIAS outputs high-impedance so that external pullup or pulldown resistors (depending on polarity) on the VPLCD and VPBIAS controls can force the power control devices to their off state. This allows the BIOS to set power control bit polarity to low true if appropriate.

Table 14-4. VG330 Dedicated Outputs for Device Power Supply Control

Pin Name	Source	Sub-System Controlled
VPRAM	PMU	System RAM
VPSYS	PMU	System ROM All system logic/peripherals PC Card Address/Data Buffers
VPLCD	LCD Ctlr from PMU request	LCD
VPBIAS	LCD Ctlr from PMU request	LCD
$\overline{\text{VCC3}}$	PC Card Ctlr	PC Card
$\overline{\text{VCC5}}$	PC Card Ctlr	PC Card
VPPEN	PC Card Ctlr	PC Card

Note: $\overline{\text{VCC3}}$, $\overline{\text{VCC5}}$, and VPPEN are power controls generated by the PC Card Controller. For details of their operation, refer to Chapter 13, *PC Card/ExCA Controller*.

VPSYS and VPRAM

The VPSYS signal controls the main power to the system. It is typically used to control power to the peripherals and ROM. VPSYS can be used to control a switching power supply or enable power via a MOSFET switch.

The VPRAM signal can be used to control memory power.

VPSYS and VPRAM are controlled directly by the Power Management Unit (PMU). When one of these pins are driven high, the associated devices and/or sub-systems controlled by that pin are powered on. The value output on these pins is determined by the current power management state, ON, DOZE, SLEEP, SUSPEND, and OFF, and the corresponding register bit of the appropriate Power ON, Power DOZE, Power SLEEP, or Power SUSPEND PMU registers.

For example, when the system is in the ON state, VPRAM is driven by bit D7 and VPSYS is driven by D2 of the Power ON register. In DOZE mode, VPRAM is driven by bit D7 and VPSYS is driven by D2 of the Power DOZE register. During OFF mode both VPRAM and VPSYS are driven low to cause devices and/or sub-systems controlled by these pins to be powered off.

SYSPWG and VPSYS Relationship

As shown in Figure 14-2, VPSYS controls the supply voltage of the system ROM and all other system peripherals. This supply voltage is turned off during SUSPEND and OFF modes.

During a resume from one of these events or from an initial power on of the entire system, the VG330 relies on the SYSPWG input pin to signal that the supply voltage controlled by VPSYS is active and stable and program execution can begin. Until the SYSPWG input is asserted, the VG330 drives all system related output pins to a high-impedance state. This protects system devices connected to VG330 output pins from latchup during power cycling.

The default assumption by the VG330 is that the SYSPWG input is driven by a simple R/C network connected to the supply voltage of the system peripherals. Because of this assumption, the VG330 delays the start of program execution from assertion of SYSPWG in order to guarantee that the system supply voltage is stable. The default delay from SYSPWG active to program execution begins is 250 ms. Following a hard reset of the VG330, program execution will always be delayed by this value.

However, for SUSPEND/RESUME or OFF/RESUME sequences, the delay between SYSPWG and program execution can be programmed via the RSMDLY[1:0] bits of the PMU RESUME Control register. The VG330 supports delays of 250 ms, 125 ms, 62.5 ms, or 0 ms.

For systems implementing external voltage supervisory circuits connected to the supply voltage of the system peripherals, one can set the RSMDLY[1:0] bits to select 0 ms of delay. That is because these types of supervisory circuits introduce their own delay between the time the minimum VCC threshold is detected and when their reset outputs are asserted. Care should still be exercised when using the 0 ms delay mode to prevent program execution from resuming before the supply voltage of the BIOS ROM has stabilized.

The VG330 assumes that the following behaviors of devices connected to VPSYS and VPRAM will occur:

Table 14-5. Design Assumptions for VPSYS and VPRAM

VPSYS	Devices and / or sub-systems are powered on in ON, DOZE, and SLEEP modes. Devices and/or sub-systems are powered off in SUSPEND and OFF modes.
VPRAM	Devices and/or sub-systems are powered on in ON, DOZE, SLEEP, and SUSPEND modes. Devices and/or sub-systems are powered off in OFF mode. VPRAM must remain active (on) in ON, DOZE, SLEEP, and SUSPEND modes. If the supply voltage to the RAM sub-system must be turned off to conserve power, OFF mode support should be implemented by the system.

14.5.4 Power Control Registers

For each power management state there is an associated power control register used to set the behavior of the power control pins (VP pins) when that state is entered.

For example, by clearing the LCD_DOZE bit of the PMU Power DOZE Register, the VPLCD output pin can be turned off (made low or high, depending on chosen polarity) when the VG330 enters the DOZE state.

The pins that can be controlled in this way are:

- VPLCD
- VPSYS
- VPRAM

The PMU Power Control Registers are:

- PMU Power ON Register at index C6H
- PMU Power DOZE Register at index C7H
- PMU Power SLEEP Register at index C8H
- PMU Power SUSPEND Register at index C9H
- PMU Polarity Register at index CAH
- PMU Output Register at index CBH

Register use is described in Chapter 16.

14.5.5 LCD Panel Power Sequencing

The LCU supports independent power up and power down sequencing of the LCD panel. Power sequencing is a process by which logic voltage, clocks/data, and bias voltage to the LCD panel are enabled/disabled in a particular order.

VPLCD and VPBIAS Control Pins

LCDs are typically powered by two power sources, a main VCC and a negative BIAS voltage. Proper sequencing of the power sources and the control signal are required to prevent damage to the LCD panel.

VPLCD and VPBIAS are indirectly controlled by the PMU, which issues requests to the LCU to power on or power off the LCD panel.

Unlike VPRAM and VPSYS which have fixed active high polarity, the polarity of VPLCD and VPBIAS are independently controlled through the LCD_POL and BIAS_POL bits of the PMU Polarity register. These bits will cause VPLCD and/or VPBIAS to be defined as active high (1 = On) when set high or active low (0 = On) when reset low.

The LCU actively drives VPLCD and VPBIAS only when the LCD panel is powered on. To power off the LCD panel, the LCU sets VPLCD and VPBIAS to a high-impedance state and relies on external pull-up or pull-down resistors to disable the external power FET supplying voltage to the LCD panel.

14.5.6 LCD Power-On Sequencing

Power-on sequencing is enabled by setting the SEQUP_EN bit of the LCD Mode Register to 1. In this mode, the LCU asserts VPLCD after a request to turn on the LCD panel has been received from the PMU. The LCU then waits until the sequence delay specified by the DLY[1:0] bits of the LCD Mode Register has been met and enables the LCD interface signals,SHCLK, LOCLK, FRAME, and LCD[3:0] which begin clocking data into the panel. Finally, the LCU again waits until the sequence delay has been met, then asserts VPBIAS and the power-on sequence is complete.

When power-on sequencing is disabled, assertion of VPLCD, enabling of clocks and data, and assertion of VPBIAS all occur simultaneously.

Care should be exercised when selecting a sequencing delay value or disabling power on sequencing. Most LCD panels specify minimum power on sequence timing to prevent the possibility of latchup. This information is normally available in the timing section of the LCD panel data sheet and should be referenced prior to selecting a power on sequencing method.

14.5.7 LCD Power-Down Sequencing

Power-down sequencing is enabled by setting the SEQDN_EN bit of the LCD Mode Register to 1. An LCD panel power-off sequence is identical to a power-on sequence except that the order of events is reversed. First, after receiving a request to turn panel power off from the PMU, VPBIAS is disabled, next clocks and data are clamped low, and finally VPLCD is disabled.

Most LCD panels do not require power down sequencing since the possibility of latchup occurs only when applying power. Therefore the SEQDN_EN bit should normally be written to 0. This is especially true for systems where critical SUSPEND mode entry is a requirement.

Examples of critical SUSPEND are: battery failure or battery removal. In these cases, the system must SUSPEND very quickly in order to prevent loss of data or excessive drain on the backup battery source. Furthermore, a SUSPEND sequence cannot be completed until the LCU has completed a power down of the LCD panel. With power down sequencing enabled, the LCU could require from 20 to 180 milliseconds to complete a power down of the LCD panel.

14.6 PMU Modes

14.6.1 The Five PMU Power Management Modes

The VG330 operates under conditions set by the current state of the PMU. The PMU has five operating modes: ON, DOZE, SLEEP, SUSPEND, and OFF.

ON is the full power operating mode, and is the default operating state. In this state the PMU allows all system operations to run at full speed and it enables all activities.

The remaining modes provide various degrees of power-managed activity. These modes are typically entered after a certain amount of inactivity of peripherals or I/O signals in the system that allows a timer to time out and cause a state change.

DOZE, SLEEP and SUSPEND each have a timer and a timer register associated with them. The application of the timer and its granularity are shown in Table 14-1, “Power Management Mode Usage”. Each timer register is user programmable and is used to either disable the timer or set the amount of time required for a time-out.

For most applications, either SUSPEND or OFF mode will be used, but not both.

The DOZE, SLEEP and SUSPEND timers all get reset when activity is detected. The activity which the PMU monitors is controlled by the PMU Activity Mask register (Index C3H). Any unmasked activity will reset the active timer and return the system to ON mode.

For example, while in ON mode, the Doze timer will be active. Any unmasked activity will reset the Doze timer and the system will remain in ON mode.

Once DOZE mode is active, the Sleep timer will be enabled. If any unmasked activity is detected, the system will transition back to ON mode.

14.7 ON Mode Operating Description

This is the (normally) full speed operating mode. The ON state is the full power, full performance state of the VG330 system.

During the ON state, all I/O peripherals are powered up with clocks supplied and the system runs with clocks at their maximum speed capabilities.

To conserve maximum power it is desirable to remain in the ON state only during computational intensive periods.

In ON mode:

- All function blocks are free to operate unless otherwise qualified (for example, SIO may be powered down)
- RTC operates
- CMOS RAM contents are accessible
- 32.768 KHz oscillator is on
- High-frequency clock is on
- CPU operates
- Pins are free to transition

Entering ON State

The VG330 can enter the ON state:

- Immediately after a hard reset
- Under programmatic control by a write of the appropriate value to the STATE bits of the PMU Status Register
- From the DOZE state if activity that is not masked is detected by the PMU
- From the SLEEP state if activity is that is not masked is detected by the PMU
- From the OFF state or the SUSPEND state, through an interrupt handler triggered by the $\overline{\text{EXT}}$ or the $\overline{\text{RI}}$ inputs, or the VG330 internal $\overline{\text{RIO}}$ signal, or by the RTC alarm

The VG330 provides a great amount of control over which activities are detected to cause awakenings from DOZE or SLEEP. These activities, and the control mechanisms, were previously described earlier in this chapter.

Exiting ON State

The VG330 will leave the ON state if the DOZE timer (controlled by PMU DOZE Timer Register at Index CCH) times out, or the VG330 is programmatically sent into another PMU state.

14.8 DOZE Mode Operating Description

This is the first level of power-saving, power-managed operation and is where the system spends the majority of its time.

During DOZE mode, the processor clock may be slowed, which reduces CPU power needs and conserves power.

In DOZE mode:

- All function blocks are free to operate unless otherwise qualified (for example, SIO may be powered down)
- RTC operates
- CMOS RAM contents are accessible
- 32.768 KHz oscillator is on
- High-frequency clock is on but CPUCLK may be slowed to reduce power
- CPU operates
- Pins are free to transition

Entering DOZE Mode

DOZE mode can be entered as a result of an activity time-out or by a software command.

Exiting DOZE Mode

The VG330 can exit from the DOZE state in any of three ways:

- It will enter the ON state when non-masked activity is detected.
- It will automatically enter the SLEEP state if the PMU SLEEP Timer (controlled by the PMU SLEEP Timer register at Index CDH) times out and the MSK_SLP bit of the PMU NMI Mask Register (Index C4H) is 1.
- It can be programmatically sent, via an interrupt, to the SLEEP state if the PMU SLEEP Timer (controlled by the PMU SLEEP Timer register at Index CDH) times out and the MSK_SLP bit of the PMU NMI Mask Register (Index C4H) is 0.

The VG330 allows creative power management strategies to be implemented, by providing a great deal of programmer control over which activities are detected and which are masked.

14.9 SLEEP Mode Operating Description

In SLEEP Mode the processor clock is slowed and power typically is removed from selected peripherals, such as the LCD panel and possibly the PC Card slot.

In SLEEP mode:

- All function blocks are free to operate unless otherwise qualified (SIO may be powered down, LCD may be powered down, etc.)
- RTC operates
- CMOS RAM contents are accessible
- 32.768 KHz oscillator is on
- High-frequency clock is on but CPUCLK is slowed to reduce power
- CPU operates
- Pins are free to transition

Entering SLEEP Mode

As with DOZE Mode, SLEEP Mode may also be entered as a result of an activity time-out, or by a software command.

Exiting SLEEP Mode

Non-masked activity may be used to cause a return to the ON mode.

Alternatively, the VG330 can be programmed to generate an NMI upon such activity. When an NMI is generated in this case, the VG330 remains in SLEEP mode until software commands the VG330 to ON mode.

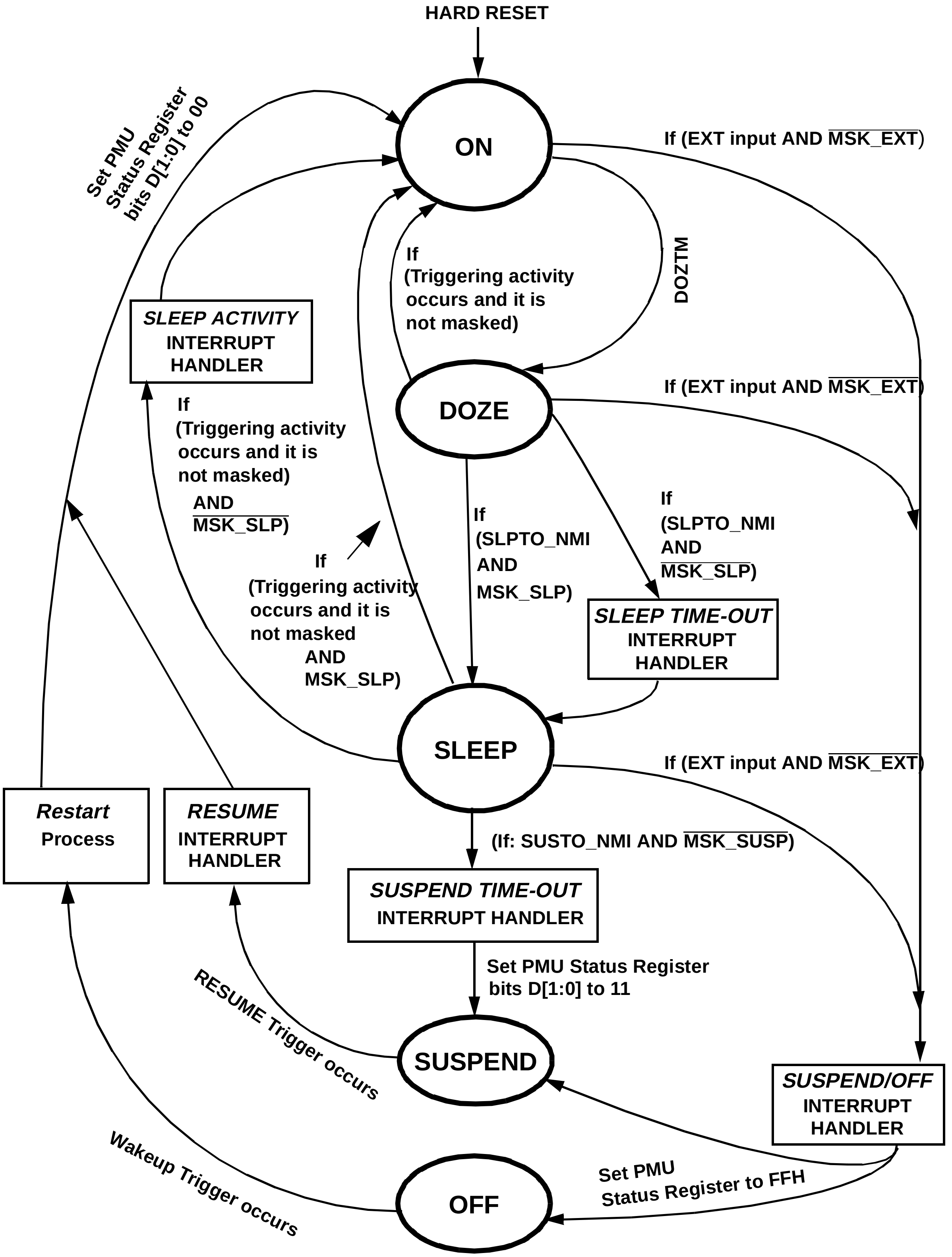
HARD RESET
ON
DOZE
SLEEP
SUSPEND
OFF
Set PMU Status Register bits D[1:0] to 00
If (EXT input AND $\overline{\text{MSK\_EXT}}$)
DOZTM
If (Triggering activity occurs and it is not masked)
SLEEP ACTIVITY INTERRUPT HANDLER
If (Triggering activity occurs and it is not masked) AND $\overline{\text{MSK\_SLP}}$)
If (EXT input AND $\overline{\text{MSK\_EXT}}$)
If (SLPTO_NMI AND MSK_SLP)
If (SLPTO_NMI AND $\overline{\text{MSK\_SLP}}$)
If (Triggering activity occurs and it is not masked AND MSK_SLP)
SLEEP TIME-OUT INTERRUPT HANDLER
If (EXT input AND $\overline{\text{MSK\_EXT}}$)
Restart Process
RESUME INTERRUPT HANDLER
(If: SUSTO_NMI AND $\overline{\text{MSK\_SUSP}}$)
SUSPEND TIME-OUT INTERRUPT HANDLER
Set PMU Status Register bits D[1:0] to 11
RESUME Trigger occurs
SUSPEND/OFF INTERRUPT HANDLER
Wakeup Trigger occurs
Set PMU Status Register to FFH

Figure 14-3 PMU States

14.10 SUSPEND Mode Operating Description

SUSPEND mode is the lowest power state which may be RESUMED without loss of system state. During SUSPEND mode all internal and external clock sources are stopped and all I/O pins are driven either to a high-impedance state or driven low, with the exception of the memory interface signals and the 32 KHz oscillator. The memory interface remains enabled and provides refresh for system RAM. The 32 KHz oscillator continues to run to operate the RTC and provide the time base for refreshing system RAM. In this mode, it is assumed that only the VG330 and system RAM and additional external logic such as PC Card buffers and SIO translators remain powered.

On SUSPEND mode:

- Clocks are stopped and function blocks except for MCU are thus disabled.
- RTC operates
- CMOS RAM contents are accessible
- 32.768 KHz oscillator is on
- 32 MHz high-frequency clock is off
- CPU stops, since its clock is stopped
- pins are either high-Z or low (Note that the states of all pins during SUSPEND are defined in Table 2-1 on page 3 of Chapter 2.)

If other external peripherals or memory devices remain powered, it is the responsibility of the system designer to terminate VG330 signals which are driven three-state. This should be done to eliminate excessive power consumption caused by floating inputs to these devices.

Entering SUSPEND Mode

SUSPEND mode requests are issued in the form of an NMI and can be made by the external EXT switch or the SUSPEND timer. Once a SUSPEND request has been issued, the power management BIOS prepares the system for SUSPEND mode, then issues a SUSPEND command to the VG330. The VG330 always requires software support to enter SUSPEND if the processor state is to be preserved.

After receiving a SUSPEND request, either from an NMI generated by EXT, Suspend timeout, or Low battery condition, the BIOS prepares the system for SUSPEND. This involves the following steps:

1. A check that the system is stable and can be reliably RESUMED, for example if it is not communicating with a peripheral whose state will be lost during SUSPEND.
2. Masking all interrupts at both PICs and at the CPU (executing CLI instruction).
3. Setting the stop on HALT bit of the Clock Control Register.
4. Disabling memory Refresh.
5. Writing a SUSPEND command to the PMU Status register.

   Once the SUSPEND command has been written, the PMU begins the following SUSPEND sequence. The PMU simultaneously:

   - Forces SUSPEND state in the PMU Status register.
   - Applies the values in the PMU Power SUSPEND register to the internal VP signals and the VP pins.
   - Begins a burst of 8 RAM refresh cycles if system RAM has been identified as DRAM.
   - Deasserts the internal Power Good signal causing the $\overline{\text{RESOUT}}$ pin to go active and the other I/O pins to be set to a high-impedance state.
6. Executing a HALT instruction.
7. The PMU then begins monitoring the burst refresh and LCD power down status. As soon as the burst refresh is complete the PMU switches to refresh timed from the 32 Khz clock. When both the burst refresh and LCD power down sequence have completed, the PMU disables the main oscillator.
8. Approximately 1 second after the $\overline{\text{RESOUT}}$ pin is asserted, all VG330 input and bi-directional pins are clamped causing these pins to become low driven outputs.
9. Immediately after the VG330 input and I/O pins are clamped, RESUME triggers are enabled and monitoring of unmasked triggers begins.

Note: RESUME trigger events during the SUSPEND sequence are not lost. These events are postponed until after the VG330 I/O pins have been clamped and are then serviced.

Exiting SUSPEND

After entry into SUSPEND has completed, the VG330 begins to monitor unmasked RESUME triggers. The VG330 will attempt to return the system to the ON state when any one of these triggers is activated unless a low battery condition exists and low battery inhibit is enabled. Low battery inhibit is explained in the RESUME Triggers section. Upon detecting an unmasked RESUME trigger, the PMU executes the following:

1. The PMU simultaneously
   - Applies the values in the PMU Power ON register to the internal VP signals and the VP pins.
   - Deasserts the internal CLAMP signal causing all bi-directional and input pins to be driven three-state.
   - Enables the main oscillator.
2. The PMU then begins monitoring the SYSPWG and LB1 inputs to determine whether to continue the RESUME or abort the sequence and return to SUSPEND.
3. Upon detecting SYSPWG active, starts the Resume Delay timer.
4. Once the Resume Delay timer expires, the PMU causes the $\overline{\text{RESOUT}}$ pin to go high and pulses the processor INTR signal. This forced the CPU to exit the HALT state and continue executing from the BIOS.
5. Immediately following the HALT exit, the BIOS sets the STATE 1:0 bits of the PMU Status Register to 00 (ON mode).
6. The BIOS polls the D4 bit, REFDONE, of the SUSPEND/REFRESH Control Register (Index E4H) to detect when control of RAM can be returned to the MCU. At that time, the BIOS re-enables MCU memory refresh
7. At this point the RESUME sequence is complete and the BIOS can reinitialize the PICs, sequence up the LCD panel, and return control to the system.

Suspend Mode Support of DRAM Refresh

Refresh pulses for DRAM are generated automatically in the SUSPEND state when the design uses DRAM and the BIOS has selected the appropriate refresh method in the SUSPEND/ REFRESH Control Register.

14.11 OFF Mode Operating Description

This is the lowest power state for the system.

OFF mode is intended for systems which require the RTC to operate but which do not require memory contents or processor state to be maintained.

In the OFF state, the VG330's RTC and internal CMOS RAM are maintained. Transition from the OFF state to the ON state results in resetting the CPU but does not affect the RTC or CMOS RAM.

The OFF state is similar to the SUSPEND state, except that the DRAM refresh feature is disabled. The OFF state is used when the contents of the system RAM are not required. This transition is treated by the BIOS as a cold boot.

While in OFF mode all clock sources except the 32.768 KHz oscillator, are stopped and all I/O pins, including the memory interface, are either high-impedance or driven low. It is assumed that only the VG330, of all the components in the system, remains powered during OFF mode.

In OFF mode:

- RTC is maintained
- CMOS RAM contents are retained
- 32.768 KHz oscillator is on
- High-frequency clock is off
- CPU is reset
- pins are either high-Z or low

Entering OFF Mode

The VG330 can be sent to the OFF state programmatically. Designers should, of course, ensure that all critical data is first saved by whatever means is applicable.

Exiting OFF Mode

See the following heading.

14.12 Resumption of Operation

This section describes how the VG330 resumes operation from the SUSPEND or the OFF states.

14.12.1 RESUME Triggers

The system can resume operation from the SUSPEND and the OFF states if a RESUME trigger occurs.

RESUME triggers are the same for SUSPEND and OFF states. Any of four sources may generate a RESUME trigger as follows:

1. A low to high transition on the EXT pin
2. A high to low transition on the internal PC Card controller $\overline{\text{RIO}}$ signal
3. An RTC alarm
4. Trigger generated after a preprogrammed number of pulses on the $\overline{\text{RI}}$ input. Only the $\overline{\text{RI}}$ source can be masked at the power management unit and may be prevented from RESUMEing the system. All other RESUME triggers must be masked at their source.

Aborting a RESUME

Conditions may be specified that allow aborting a RESUME sequence if the battery source is not capable of supplying enough power to complete the power up.

1. RESUME triggers can be qualified with the LB1 input. If LB1 is active, indicating a low battery condition, the RESUME triggers may be ignored. Alternatively, if LB1 goes active prior to SYSPWG being asserted, the RESUME sequence is aborted and the system re-enters SUSPEND.

2. Alternatively, the VG330 may be programmed to time the SYSPWG signal relative to the application of power (VPSYS activated). If SYSPWG does not go active within 1 second, the RESUME sequence is aborted and the system re-enters SUSPEND.

When a RESUME sequence has been ignored or aborted, the VG330 provides two options for signaling the system of this condition. In the first case the VG330 may be programmed to generate a one-second tone on the speaker to signal a low battery condition caused the RESUME to be ignored.

In the second case, the VG330 may generate two one-second tones, separated by one second, to indicated a RESUME sequence was aborted due to LB1 active prior to SYSPWG or because of SYSPWG time-out.

Status Reporting

The power management unit provides status for a number of conditions. Activity status is provided by an activity bit in the main PMU status register. This register also provides status on the current power management state, and the cause of RESUME and whether the RESUME is from normal SUSPEND or Automatic SUSPEND. Detailed activity status, namely which activity source(s) were recently detected, is available in the Activity status register. Both the Activity status register and the activity bit of the PMU status register are automatically cleared following a read.

Other status information provided by the PMU remains valid following a read. Some status bits require specific clearing by software, and others can only be set by external events as is the case with the RESUME wakeup cause.

NMI Generation

The PMU may generate an NMI to signal the system of an activity time-out, or an activity trigger, or low battery status, or to request entry into SUSPEND mode.

All NMI sources may be enabled or disabled and a global mask bit is provided to temporarily mask NMI without losing pending NMIs or preventing the occurrence of new NMIs. NMI reporting is provided by the NMI Status Register.

Both the SLEEP timer and the SUSPEND timer may be programmed to generate NMI.

NMI and SLEEP Timer

When the SLEEP NMI is enabled, the PMU will generate an NMI and remain in DOZE mode when the SLEEP timer expires. It is then the responsibility of the software to program the PMU into SLEEP mode. Once in SLEEP mode, the PMU will not automatically return to ON when unmasked activity is detected. Instead the PMU will generate an NMI and remain in SLEEP mode waiting for software to program it back to ON.

When the SLEEP NMI is disabled, the PMU automatically transitions from DOZE to SLEEP mode when the SLEEP timer expires and automatically returns to ON mode when unmasked activity is detected.

NMI and SUSPEND Timer

When SUSPEND NMI is enabled, the PMU will generate an NMI and remain in SLEEP mode when the SUSPEND timer expires. It is then the responsibility of the software to program the PMU into SUSPEND mode. The PMU never automatically enters SUSPEND mode as a result of a SUSPEND timeout.

NMI and the LB1, LB2, and EXT Signals

The PMU also generates NMI as a result of Low Battery1, or LB1, and Low Battery2, or LB2, status. Each of these sources are provided with an enable bit to allow NMI to be generated. The LB1 NMI enable bit will not prevent LB1 from aborting a RESUME operation if the LB RESUME abort capability is enabled.

Both LB1 and LB2 may be defined as edge triggered inputs or may be debounced by the PMU. When Low battery debounce is enabled, the LB1 or LB2 pins must remain active for 1 ms before NMI will be asserted. When Low battery debounce is disabled, LB1 and LB2 are defined as edge triggered. In both cases a rising edge on the sampled LB1 or LB2 is latched to generate NMI. The LB1 or LB2 NMI can then be cleared by clearing the LB1 or LB2 NMI status bit. The final NMI source is the EXT pin. EXT is typically driven by a push-button switch and asserted to request that the system SUSPEND, OFF, or RESUME. An enable/disable bit is provided to prevent NMI from EXT. However, this bit does not prevent EXT from RESUME’ing the system.

EXT is defined as a rising edge triggered input but is also debounced by a low frequency clock. In order for a rising edge on EXT to be recognized, EXT must first be sampled low for a minimum of 62.5 ms. This debounce is provided to prevent spurious NMIs during SUSPEND requests or SUSPEND request NMIs during RESUME.

14.13 SmartClock

14.13.1 SmartClock and DOZE/ SLEEP Clock Control

During DOZE or SLEEP power management states, the processor clock can be slowed by one of two programmable divisors. A global power management clock enable bit is provided to force the processor to run at full speed regardless of the power management or SmartClock state.

SmartClock operates in conjunction with the DOZE/SLEEP clock control logic to prevent degradation of system performance. SmartClock continuously monitors system activity and attempts to quickly slow down or speed up the processor clock in response to changing system requirements. Typically, DOZE and SLEEP modes attempt to keep the processor clock running slow.

14.13.2 Activity Monitoring

The PMU Activity Mask Register determines which activities will transition the VG330 to ON mode.

The SmartClock Activity Mask Register determines which activities will affect the SmartClock.

Note that when an activity transitions the VG330 to the ON state, the activity mask setting in the SmartClock Activity Mask Register becomes non-significant to system operation.

DOZE and SLEEP modes are defined in terms of absolute activity and inactivity. For these states, a single activity trigger will force an exit back to the ON state. And, once this has occurred, a complete lack of activity, typically for several seconds, will be required before DOZE can be re-entered.

For certain activity sources, such as keyboard input, display updates, touch panel input, etc., it may not be necessary or desirable to exit DOZE mode and return to full speed operation. In these situations SmartClock can temporarily restore the clock to full speed, then return to a slow clocking mode in milliseconds or even microseconds.

SmartClock contains hysteresis which acts to hold the processor clock at either full speed or slow speed.

- When the SmartClock activity level reaches the upper threshold, the processor clock is forced into a fast clocking mode.
- When the SmartClock activity level reaches the lower threshold, the processor clock is forced into a slow clocking mode.

The upper and low thresholds are fixed at FFH and 00H respectively.

How SmartClock Works

SmartClock monitors both activity and inactivity within a programmable timeslice measured in the microseconds to milliseconds range. Separate programmable registers allow an Active Step Value or alternatively an Inactive Step Value to be added to the current activity level during each timeslice. The Active Step Value is always a positive number and may be set from 0 to 255. The Inactive Step Value may be either a negative or positive number and ranges from -128 to +127. Only a single Active Step Value may be added to the current activity level within a particular timeslice.

When activity is detected, the current activity level is immediately updated and further activity monitoring is disabled for that timeslice. This operation allows the system to respond quickly to activity triggers but also acts to prevent additional activity from unnecessarily holding the activity level at the high threshold.

Inactive Step Values are always sampled at the end of each timeslice and the current activity level adjusted at that time.

For default BIOS power management, the Active Step Value might be set to the maximum, 255, and the Inactive Step Value would be set to a relatively small negative number, for instance -64. In this way any activity would immediately cause the activity level to cross the high threshold and return the processor clock to full speed. Inactivity, on the other hand, would cause the activity level to slowly approach the lower threshold, preventing the system from returning to a slow clocking mode until the system was truly idle.

SmartClock and APM

The SmartClock logic can be most effective when used with an APM driver. In this case, the Active Step Value might be set very high, or even to the maximum, and the Inactive Step Value would be set to a positive number, for instance 64 or 128.

In this situation, the SmartClock logic is always attempting to restore the processor clock to full speed and the APM driver, when it gets called, is trying to reset the activity level back to the low threshold. When the system becomes busy because of a compute-intensive application, the APM driver will not be called, and therefore the activity level will eventually cross the high threshold and the processor clock will be returned to full speed.

Clock Control and Interrupts

The SmartClock samples activity sources defined by the SmartClock Activity Mask Register. It also samples interrupts from INTR, interrupt requests on IRQ0 through IRQ15, or NMI.

However, activity on these sources does not make use of the SmartClock Active Step Register. Instead, when one of INTR, IRQ0, IRQ1, or NMI is asserted, the activity level will immediately be set to the high threshold, causing the processor clock to run at full speed. The activity level will remain fixed at the high threshold until the interrupt is terminated.

For INTR, IRQ0, and IRQ1, the interrupt is terminated when an End Of Interrupt (EOI) command is written to the interrupt controller. For NMI, the interrupt is terminated when the NMI is deasserted.

Clock Control and Hold Request

SmartClock does not monitor HRQ to the processor. Other logic returns the processor clock to full speed when HRQ is asserted. The clock remains at full speed until HLDAK is returned by the processor. Once HLDAK has been asserted, the processor clock is allowed to return to slow speed.

Static Clock Modes

The processor clock can also be optionally stopped under the following conditions:

- Following a HALT command.
- While the CPU is not the bus master.
- During Expansion bus cycles.

Each of the above sources can be independently enabled. For stop clock on HALT, the processor clock is stopped after a HALT cycle has been detected on the bus and restarted when a bus master request, interrupt, or NMI is generated.

When other bus masters such as memory Refresh or the display controller are granted the bus, the processor clock may also be stopped. The clock is first stopped after the processor acknowledges the hold request by asserting HLDAK. The clock remains stopped until the requesting device releases HRQ.

In the other cases, the processor clock is stopped once the cycle is under way and remains stopped until the ready signal, RDY, is asserted.

14.13.3 Power Management Status

The BIOS can interrogate the state of power management by checking the value of the STATE bits located in the PMU Status Register (Index C0H). Bits D0 and D1 reflect the current power management state.

Power Down Considerations

During Suspend mode, the VG330 and the RAM array remain powered. This keeps the real time clock operating and system setup configuration stored. During this state the VG330 will consume less than 100uA. Care must be taken in the design to prevent any current leakage paths between the powered up sections of the system and powered down. The VG330 leakage control circuitry drives certain inputs to prevent excessive current consumption. Also certain outputs are driven low or to high-impedance to terminate inputs outside of the VG330.

14.14 Serial Port Power Management

For information about SIO function block power management, see *Power Management of SIO* on page 11-7. SIO power is managed separately from the PMU activity.

14.15 Related Registers

The PMU control registers are summarized in Table 14-6 on this page and the next one.

Table 14-6. PMU Controller-Related Registers

Register	I/O Address	Function Summary
PMU Status Register	C0H	Shows various operating status conditions
Reserved	C1H	
PMU Control Register	C2H	Provides control of certain operating characteristics
PMU Activity Mask Register	C3H	Determines which activities in the system are allowed to trigger the PMU’s state transitions
PMU NMI Mask Register	C4H	Controls behavior related to generation of NMIs
PMU I/O Range Register	C5H	Sets I/O range for activity detection controlled by PMU Activity Mask Register (Index C3H) bit D7
PMU Power On Register	C6H	Sets the values applied to VPRAM output, VPSYS output, and VPLCD output when PMU enters ON State
PMU Power Doze Register	C7H	Sets the values applied to VPRAM output, VPSYS output, and VPLCD output when PMU enters DOZE State
PMU Power Sleep Register	C8H	Sets the values applied to VPRAM output, VPSYS output, and VPLCD output when PMU enters SLEEP State
PMU Power Suspend Register	C9H	Sets the values applied to VPRAM output, VPSYS output, and VPLCD output when PMU enters SUSPEND State
PMU Polarity Register	CAH	Sets polarity of VPLCD and VPBIAS outputs
PMU Output Register	CBH	Shows status of VPRAM, VPSYS, and VPLCD outputs
PMU Doze Timer Register	CCH	The PMU DOZE Timer Register sets the DOZE Timer countdown value.
PMU Sleep Timer Register	CDH	The PMU SLEEP Timer Register sets the SLEEP Timer countdown value.
PMU Suspend Timer Register	CEH	Sets the SUSPEND Timer countdown value.
Reserved	CFH - DAH	

Table 14-6. PMU Controller-Related Registers

Register	I/O Address	Function Summary
PMU Activity Status Register	DBH	Shows status of activity detectors
PMU NMI Status Register	DCH	Shows status of pending NMIs
PMU Resume Control Register	DDH	Provides control of various operating characteristics related to the RESUME State
Clock Control Register	DEH	Provides control over processor stop clock activity
SmartClock Activity Mask Register	DFH	Determines which activities in the system are allowed to activate the SmartClock counter in the Activity direction
SmartClock Inactive Step Register	E0H	Sets the sampling period for detection of activity, based on units of time set by the SmartClock Control Register
SmartClock Active Step Register	E1H	Sets the value added to the current SmartClock activity count when activity has been detected during one sampling period
SmartClock Activity Level Register	E2H	Shows the value of the SmartClock Activity Counter
SmartClock Control Register	E3H	Enables SmartClock; allows setting the SmartClock sampling rate
SUSPEND/REFRESH Control Register	E4H	Sets RAM memory type for refresh controller used during SUSPEND refresh operations

15 RTC, Timer, and Interrupt Controller

15.1 Introduction

The VG330 contains several standard PC peripherals. These include a Real Time Clock (RTC), a PC-compatible Timer, and a dual Intel 8259-compatible Interrupt Controller (ICU).

This chapter discusses these items and also discusses Non Maskable Interrupts in the VG330.

15.1.1 Capabilities

RTC

- Vadem-designed low-power real time clock with 64 bytes of low-power CMOS static RAM
- Programmatically supported through BIOS

Timer

- Intel 8254-compatible timer

Interrupt Controller Unit

- Dual Intel 8259-compatible Programmable Interrupt Controllers
- Two dedicated IRQ pins, IRQA and IRQB, can be routed to any one of IRQ1 through IRQ7, excluding IRQ 2.

15.2 Real Time Clock

The VG330 RTC is a VADEM design and requires BIOS support. The RTC contains three main elements:

- a series of counters used to keep time
- an alarm function
- 64 bytes of CMOS RAM for storage of system set-up information.

The input clock for the RTC is the 32 KHz Low Frequency Clock, which runs continually during all power management states.

The Real Time Clock is not related to the Smart-Clock (which is a feature of the Power Management Unit.)

15.2.1 Architecture

Figure 15-1 shows the main components of the RTC.

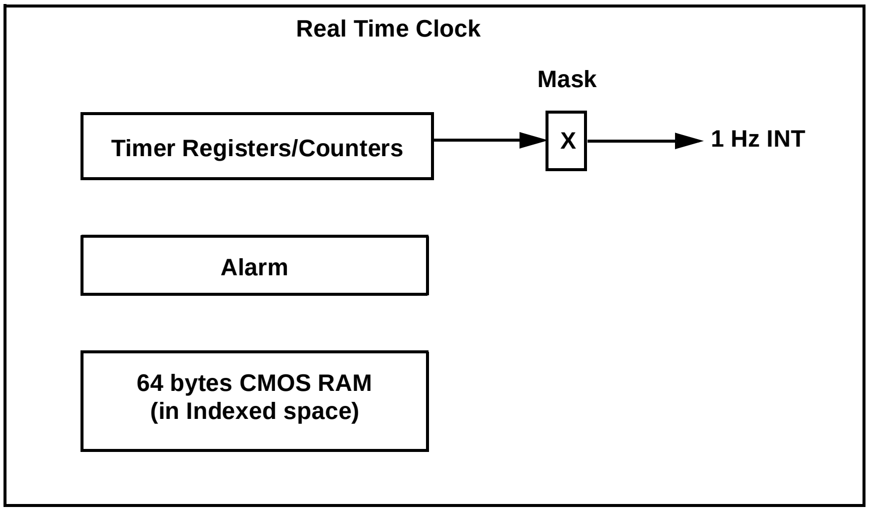

Figure 15-1 RTC Block Diagram

15.2.2 RTC Timers/Counters

The RTC registers consist of the timer/counter registers, a Mode register that sets operating state, and a Status register that reports status of operation. These registers are described in Chapter 16, *Registers*.

15.2.3 RTC RAM

The RTC also provides 64 bytes of CMOS static RAM. This can be used to store system set-up information. The RTC contains CMOS static RAM from index 80H to BFH. This RAM is accessed through the VG330's indexed registers addressing space. The RAM is valid as long as power is applied to the VG330.

15.2.4 RTC Alarm

The RTC includes an alarm that can be programmed to generate a time-of-day alarm or a 32 day alarm interrupt. The alarm can be used to place the VG330 into the ON Power Management State from either the OFF state or the SUSPEND state. To do this requires enabling the alarm for this action, using the RTC Mode Register at 79H.

While in time-of-day operation, an alarm interrupt is triggered at the same time every day until the alarm is disabled. In 32 day mode, an alarm may be set for a specific day up to 32 days in advance.

The cause of a RESUME from SUSPEND or OFF can be read in the PMU Status Register at index C0H. Bits D[6:5] indicate the source, including whether the RTC caused wakeup.

15.2.5 Related Registers

Register	Address
RTC Seconds Register	Index 70H
RTC Minutes Register	Index 71H
RTC Hours Register	Index 72H
RTC Day Low Register	Index 73H
RTC Day High Register	Index 74H
RTC Alarm Seconds Register	Index 75H
RTC Alarm Minutes Register	Index 76H
RTC Alarm Hours Register	Index 77H
RTC Alarm Day Register	Index 78H
RTC Mode Register	Index 79H
RTC Status Register	Index 7AH
RTC CMOS RAM	Index range 80H - BFH
PMU Status Register	Index C0H

15.3 Interrupt Controller Unit

The VG330 includes dual 8259-compatible Programmable Interrupt Controllers integrated into the architecture.

15.3.1 IRQA and IRQB

The VG330 provides two dedicated interrupt pins, IRQA and IRQB. System software may configure these pins to drive IRQs in the range of IRQ1 through IRQ7. This assignment is performed using the ICU Mode Register.

15.3.2 IRQ and GPIO Pins

In addition to the two dedicated interrupt input pins, additional interrupts can be supported using the GPIO pins. Up to 7 additional interrupt inputs are supported. Refer to the Chapter 12 description of GPIO functions for details, and also the GPIO Group Mode Register descriptions in Chapter 16.

15.3.3 Interrupt Gating

When IRQs are assigned to devices, the assigned IRQ signals are OR'd together internally. For example, if the SIO is assigned IRQ3 and the PC Card Controller is assigned IRQ3, the VG330 ORs together the assigned signals to drive IRQ3.

The VG330 does not internally resolve interrupt conflicts. It is the responsibility of the system software to assure that interrupt assignments do not conflict with each other.

15.3.4 Architecture

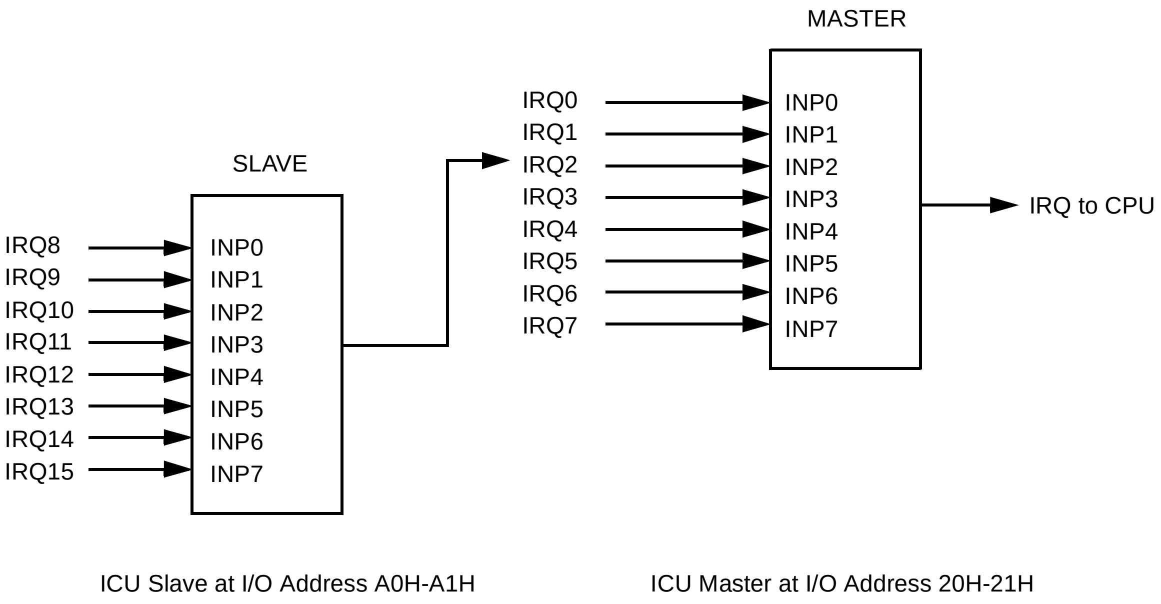

Figure 15-2 ICU Block Diagram

Table 15-1 lists interrupts for which dedicated use is made within the VG330 or for which or assignable use is available:

Table 15-1. IRQ Usage

IRQ	Internal Devices
0	Dedicated - timer channel 0
1	Assignable to: IRQA pin, IRQB pin, KCU, GPIO (pin assignable/mappable - see GPIO Group Mode registers)
2	Dedicated to cascaded slave-master interrupt controller use
3	Assignable to: IRQA pin, IRQB pin; SIO; GPIO; PC Card
4	Assignable to: IRQA pin, IRQB pin; SIO; GPIO; PC Card
5	Assignable to: IRQA pin, IRQB pin; GPIO; PC Card
6	Assignable to: IRQA pin, IRQB pin, GPIO
7	Assignable to: IRQA pin, IRQB pin; SIO; GPIO (pin assignable/mappable - see GPIO Group Mode registers) ; PC Card
8	Reserved
9	RTC; GPIO (pin assignable/mappable - see GPIO Group Mode registers)
10	GPIO (pin assignable/mappable - see GPIO Group Mode registers); PC Card
11	GPIO (pin assignable/mappable - see GPIO Group Mode registers); PC Card
12	GPIO (pin assignable/mappable - see GPIO Group Mode registers); PC Card
13	GPIO (pin assignable/mappable - see GPIO Group Mode registers)
14	GPIO (pin assignable/mappable - see GPIO Group Mode registers); PC Card
15	GPIO (pin assignable/mappable - see GPIO Group Mode registers); PC Card

15.4 NMI in the VG330

A variety of interrupt sources in the VG330 are routed to the NMI input of the V30MX CPU. Each of these sources can be masked. The nature of the masks depends on the functional area providing the source. For example, various actions within the PMU can generate an NMI request coming out of the PMU. Similarly, various actions within the KCU can generate an NMI request. All NMI requests coming from subsystems are OR'd together to drive the CPU NMI input. The source of an NMI request can be read in the Main NMI Status Register at index 19H.

The method of clearing an NMI depends on the source of the NMI request.

Sources that can generate NMI requests are:

- PMU
- KCU
- PCS (see PCS Mode registers) in GPIO

See also:

- Discussion of keyboard interfacing in Chapter 10.
- *Programmable Chip Selects* on page 12-4 of Chapter 12, *GPIO*.
- *NMI Generation* on page 14-17 of Chapter 14, *Power Management Unit*.

15.4.1 Related Registers

Register	Address
For IRQs, relevant registers are:	
ICU Mode Register	Index 0DH
ICU Shadow Register - Primary Interrupt Controller	Index 40H
ICU Shadow Register - Secondary Interrupt Controller	Index 41H
See also related registers used for programming GPIO to configure IRQs on GPIO pins. (GPIO Group Mode registers)	
For NMI, relevant registers are:	
Main NMI Status Register	Index 19H
PCS 0 Mode Register	Index 20H
PCS 1 Mode Register	Index 24H
PCS 2 Mode Register	Index 28H

15.5 Timer

The Timer is a PC/XT-compatible Intel 8254 equivalent.

- Channel 0 of the Timer is reserved for the System Timer (18 Hz periodic interrupt).
- Channel 1 is unused
- Channel 2 is used to control the System Speaker.

For register descriptions, refer to the Intel 8254 documentation

16 Registers

16.1 Organization of This Chapter

This chapter is organized as follows:

- Description of register organization
- Listing and description of VG330 I/O-Mapped registers
- Listing of VG330 Indexed registers:
  - General registers
  - LCU registers
  - PC Card Controller registers
- Description of VG330 indexed registers:
  - General Registers
  - LCD Controller Unit registers.
  - PC Card Controller registers

16.2 Register Organization and Mapping

There are two main ways to access registers in the VG330.

The first category is comprised of those registers accessed using *I/O addressing*. The second category is *indexed* registers, that is, registers assigned an index number. These registers are reached only by first writing an index value to an Index Register, and then accessing data through a Register Data register.

Most of the IBM PC-compatible registers and peripherals are accessed using I/O addressing. Most of the Vadem-specific registers are reached using indexing, through the VG330 Index Register and the VG330 Data Register. However, the LCD Controller Unit and the PC Card Controller are accessed through their own separate sets of index and data registers, as shown in Figure 16-1.

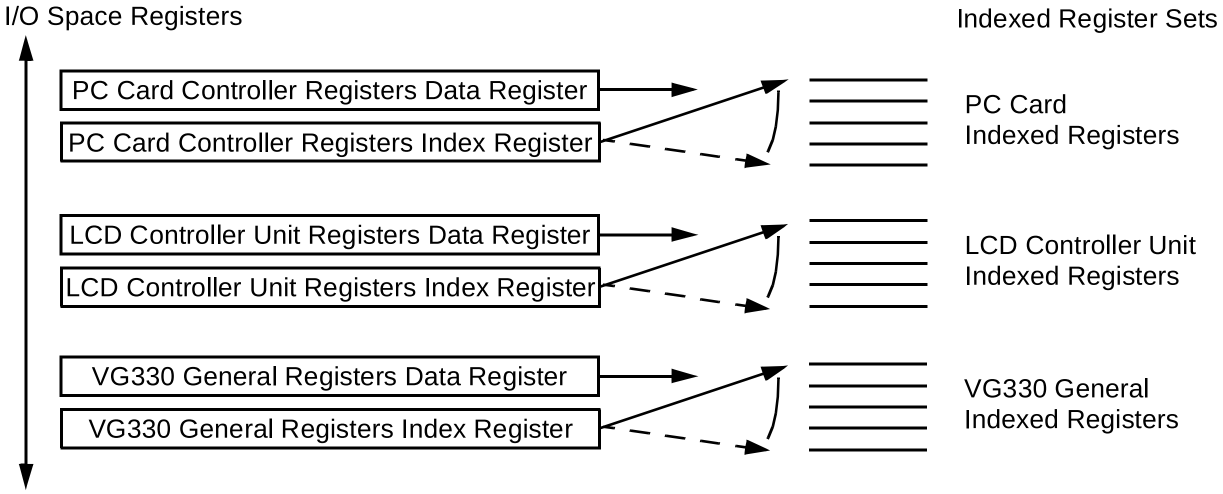
I/O Space Registers
Indexed Register Sets
PC Card Controller Registers Data Register
PC Card Controller Registers Index Register
PC Card
Indexed Registers
LCD Controller Unit Registers Data Register
LCD Controller Unit Registers Index Register
LCD Controller Unit
Indexed Registers
VG330 General Registers Data Register
VG330 General Registers Index Register
VG330 General
Indexed Registers

Figure 16-1 Register Organization in the VG330

16.3 I/O Mapped Registers Listed

Table 16-1 lists the addresses or address ranges for all I/O-mapped VG330 registers.

Table 16-1. VG330 Registers in the I/O Address Space

Register/Peripheral	I/O Address
8259-Compatible Interrupt Controller (Primary)	020H - 021H
VG330 Index Register	026H
VG330 Data Register	027H
8254-CompatibleTimer	040H - 043H
PC/XT-Compatible PPIA Keyboard Data Register	060H
PC/XT Compatible PPIB Keyboard Control Register	061H
PC/XT Compatible PPIC System Status Register	062H
Memory Mapper Address Register	06CH
Mapper Low Byte Data Register	06EH
Mapper High Byte Data Register	06FH
8259-Compatible Interrupt Controller (Secondary)	0A0H-0A1H
Serial Port	2E8H - 2EFH, or 2F8H - 2FFH, or 3F8H - 3FFH
LCU - LCD Controller Unit	3D4H - 3D5H, and 3D8H - 3DEH
PC CARD/ExCA Controller	3E0H - 3E1H

16.4 I/O Register Reference

VG330 I/O-mapped registers are described on the following pages.

Name	8259-Compatible Interrupt Controller Registers
Type	Read/Write
I/O Address	020H - 021H (Primary) and 0A0H - 0A1H (Secondary)

Description

These registers are compatible with the equivalent registers in the Intel 8259 Interrupt Controller.

Name VG330 Index Register

Type Read/Write

I/O Address 026H

Description Use this register to select VG330 General registers by writing a register's index number to this register. The selected register is accessed through the Data Register at I/O Address 027H.

Note that the LCU registers and PC Card registers are accessed through their own separate index and data registers as described in the corresponding sections of this manual.

Bits

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

D[7:0] **DA**

To access a register in the indexed general register group, write its index to this register.

Name VG330 Data Register

Type Read/Write

I/O Address 027H

Description Use this register to access a VG330 General register after it has been selected using VG330 Index register at I/O address 026H.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

D[7:0] **DD**

This contains data in the register selected by the VG330 Index Register.

Name	8254-Compatible Counter/Timer Registers
Type	Read/Write
I/O Address	040H - 043H
Description	PC/XT-compatible Counter/Timer. Its registers are compatible with the equivalent registers in the Intel 8254 Counter/Timer.

Name	PC/XT Compatible PPIA Keyboard Data Register
Type	Read only
I/O Address	060H
Description	Contains Keyboard Scan Code.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
KSC7	KSC6	KSC5	KSC4	KSC3	KSC2	KSC1	KSC0

D[7:0] **KSC**

Keyboard Scan Code

The function of this register changes depending upon the state of the ENASCAN bit of the Keyboard Scan Enable register located at VG330 Index 66H.

Normally, the PC/XT keyboard data register is read only.
When keyboard scanning is enabled, the BIOS writes the translated keyboard scan code to this register. Default value is 00H.

Name	PC/XT Compatible PPIB Keyboard Control Register
Type	Read/Write
I/O Address	061H
Description	Keyboard and other control functions.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
RSTKBD	KCLKEN	Reserved	Reserved	HISWS	Reserved	SPKDAT	TGATE

D7 **RSTKBD**

Enable and reset keyboard

0 = Enable Keyboard (default).
1 = Clear Keyboard Data Port and IRQ1

D6 **KCLKEN**

Enable Keyboard Clock

0 = Force Keyboard Clock Low (default).
1 = Enable Keyboard Clock.

KCLKEN is pulsed low by software to request that the keyboard perform diagnostics.

When the Keyboard Controller is configured for matrix keyboard scan mode, KCLKEN may be used to generate an NMI. Following a write to the PPIB port with the KCLKEN bit reset low, an NMI will be generated on the next write to the PPIB port with the KCLKEN bit set high. At this time the BIOS will perform a keyboard scan operation and return the results to the PPIA port.

D[5:4] **Reserved.**

Default = 00H

D3 **HISWS**

Switch Enable

0 = Enable System Switches SW1 - SW4 (default)
1 = Enable System Switches SW5 - SW8

D2 **Reserved**

Default = 0

D1 **SPKDAT**

Enable Speaker Output

0 = Disable Speaker Output (default)
1 = Enable Speaker Output

D0 **TGATE**

Enable Timer Channel 2

0 = Disable Timer Channel 2 (Speaker Clock) (Default)
1 = Enable Timer Channel 2

Name PC/XT Compatible PPIC System Status Register
Type Read/Write
I/O Address 062H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	TOUT2	$\overline{\text{SPKR}}$	SW4_8	SW3_7	SW2_6	SW1_5

D[7:6] **Reserved**

Reserved bits. Default = 00H.

Always read back as zero.

D5 **TOUT2**

State of 8254 TOUT2 (Speaker Clock).

D4 **SPKR**

Inverted state of the SPKR output pin

0 = Speaker is ON
1 = Speaker is OFF (default)

D3 **SW4_8**

SW4 - Always set high
SW8 - Set by bit D7 of the Keyboard Scan Enable Register

D2 **SW3_7**

SW3 - Always set high
SW7 - Set by bit D6 of the Keyboard Scan Enable Register

D1 **SW2_6**

SW2 - Always reset low
SW6 - Set by bit D5 of the Keyboard Scan Enable Register

D0 **SW1_5**

SW1 - Always reset low
SW5 - Set by bit D4 of the Keyboard Scan Enable Register

Name	Mapper Address Register
Type	Read/Write
I/O Address	06CH
Description	Used this register to select memory mapping registers by writing corresponding page address to this register.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
PA19	PA18	PA17	PA16	PA15	PA14	Reserved	Reserved

D[7:2] **Page Address**

Page address of the Memory Mapping register to access through the Map Data registers. Default = 000000B.

For systems operating in 640 x 200 or 640 x 400 video mode, valid entries are:

A0, A4, A8, and AC
C0, C4, C8, and CC
D0, D4, D8, and DC
E0, E4, E8, and EC

For systems operating in 640 x 480 graphics mode, valid entries include the above list plus

B0, B4, B8, and BC
C0, C4, C8, and CC
D0, D4, D8, and DC
E0, E4, E8, and EC

See discussion in Chapter 8, MCU.

D[1:0] **Reserved**

Reserved bits. Default = 00H

Always clear to zero.

Name Mapper Low Byte Data Register

Type Read/Write

I/O Address 06EH

Description For the address currently specified in register 06CH, this register contains the translated mapped address for A[21:14]

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MAPA21	MAPA20	MAPA19	MAPA18	MAPA17	MAPA16	MAPA15	MAPA14

D[7:0] **MAPA LOW**

Least significant byte of memory map address in the selected memory device.

Name	Mapper High Byte Data Register
Type	Read/Write
I/O Address	06FH
Description	For the address currently specified in register 06CH, this register contains the translated mapped address for A[23:22]. It also defines memory type and sets page enable for this page.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
PEN	Reserved	DTYP1	DTYP0	Reserved	Reserved	MAPA23	MAPA22

D7 **PEN**

0 = Disable mapping for this page (default)
1 = Enable mapping for this page

D6 **Reserved**

Reserved bit. Default = 0H.

Always clear this bit to zero.

D[5:4] **DTYP**

Memory Type.

These bits select the type of memory device assigned to this memory page, according to the following table:

DTYP1	DTYP0	Page Memory Device Type
0	0	None. (Default) VG330 performs an expansion memory cycle (ISA) with accesses to this mapped address.
0	1	RAM (defined by the setting of the RAM Type Select bits D[3:0] bits of the Memory Control 1 Register, Index 04H)
1	0	ROM #0
1	1	ROM #1

D[3:2] **Reserved**

Reserved bits. Default = 00B

Always clear this bit to zero.

D[1:0] **MAPA HIGH**

Most significant bits of memory map address in the selected memory device.

Name 16450 Serial Port Registers

Type Read/Write

I/O Address 2E8H - 2EFH, or 2F8H - 2FFH, or 3F8H - 3FFH, depending on the setting of the SPSEL bits of the SIO Mode Register

Description Refer to 16450 Data Manual for register definitions.

16.5 Indexed Registers

Many Vadem extension registers are in sets reached only through indirect addressing (indexing).

There are three sets of indexed registers in the VG330. These groups are listed in Table 16-2:

Table 16-2. Sets of VG330 Indexed Registers

Register Set	**Index and data registers for this set**		**For more information, see:**
	Index Reg	**Data Reg**	
LCU - LCD Controller Unit[a]	I/O Address 3D4H	I/O Address 3D5H	Chapter 9, and descriptions in LCU registers section of this chapter.
PC Card Controller	I/O Address 3E0H	I/O Address 3E1H	Chapter 13, and descriptions in the PC Card Controller registers section of this chapter.
All remaining VG330-specific registers not in the above two sets	I/O Address 026H	I/O Address 027H	Refer to relevant chapters.

[a] Of all the LCU registers, only the LCD Configuration Control Register is accessed through the VG330 Index Register at 26H and VG330 Data Register at 27H. The remainder are accessed as shown.

The following table lists all indexed registers in the VG330. Register descriptions follow.

Table 16-3. VG330 Indexed Registers - Primary Group

Register	**Index**
Revision Register	00H
BCG Mode Register	01H
Reserved	02H - 03H
Memory Control 1 Register	04H
Memory Control 2 Register	05H
Alt. Display Buffer Start Address Register	06H
LCD Configuration Control Register	07H
Reserved	08H - 0CH
ICU Mode Register	0DH
Reserved	0EH
SIO Clock Control Register	0FH
SIO Mode Register	10H
SIO Power Control Register	11H
Timer Clock Control Register 1	12H
Timer Clock Control Register 2	13H

Table 16-3. VG330 Indexed Registers - Primary Group

Register	Index
Address Pin Configuration Register 1	14H
Address Pin Configuration Register 2	15H
Address and Data Pin Control Register	16H
Reserved	17H - 18H
Main NMI Status Register	19H
Reserved	1AH - 1FH
PCS 0 Mode Register	20H
PCS 0 Address Start Register	21H
PCS 0 Address Stop Register	22H
PCS 0 Address High Register	23H
PCS 1 Mode Register	24H
PCS 1 Address Start Register	25H
PCS 1 Address Stop Register	26H
PCS 1 Address High Register	27H
PCS 2 Mode Register	28H
PCS 2 Address Start Register	29H
PCS 2 Address Stop Register	2AH
PCS 2 Address High Register	2BH
Alternate PCS Mode Register	2CH
Alternate PCS Address Start Register	2DH
Alternate PCS Address Stop Register	2EH
Alternate PCS Address High Register	2FH
BIOS Time Base Low Register	30H
BIOS Time Base High Register	31H
Reserved	32H - 33H
Expansion Bus Mode Register	34H
Expansion Bus I/O Wait State Control Register	35H
Expansion Bus Memory Wait State Control Register	36H
Reserved	37H
Top of Memory Register	38H
Reserved	39H - 3FH
ICU Shadow Register 1	40H
ICU Shadow Register 2	41H

Table 16-3. VG330 Indexed Registers - Primary Group

Register	Index
Reserved	42H - 4FH
GPIO Group A Mode Register 1	50H
GPIO Group A Mode Register 2	51H
GPIO Group A Mode Register 3	52H
GPIO Group A Mode Register 4	53H
GPIO Group B Mode Register 1	54H
GPIO Group B Mode Register 2	55H
GPIO Group B Mode Register 3	56H
GPIO Group B Mode Register 4	57H
GPIO Group C Mode Register 1	58H
GPIO Group C Mode Register 2	59H
GPIO Group C Mode Register 3	5AH
GPIO Group C Mode Register 4	5BH
GPIO Group A Data Register	5CH
GPIO Group B Data Register	5DH
GPIO Group C Data Register	5EH
Reserved	5FH
Scan Control A Register	60H
Scan Control B Register	61H
Scan Control C Register	62H
Return Status A Register	63H
Return Status B Register	64H
Return Status C Register	65H
Keyboard Scan Enable Register	66H
Scan NMI Control and Status Register	67H
XT Shadow Serial Shift Register	68H
Reserved	69H - 6FH
RTC Seconds Register	70H
RTC Minutes Register	71H
RTC Hours Register	72H
RTC Day Low Register	73H
RTC Day High Register	74H
RTC Alarm Seconds Register	75H

Table 16-3. VG330 Indexed Registers - Primary Group

Register	Index
RTC Alarm Minutes Register	76H
RTC Alarm Hours Register	77H
RTC Alarm Day Register	78H
RTC Mode Register	79H
RTC Status Register	7AH
Reserved - Write only test register	7BH
ROM Wait State Control Register	7CH
RAM Wait State Control Register	7DH
Refresh Timer Register	7EH
Refresh Control Register	7FH
RTC CMOS RAM	80H - BFH
PMU Status Register	C0H
Reserved	C1H
PMU Control Register	C2H
PMU Activity Mask Register	C3H
PMU NMI Mask Register	C4H
PMU I/O Range Register	C5H
PMU Power On Register	C6H
PMU Power Doze Register	C7H
PMU Power Sleep Register	C8H
PMU Power Suspend Register	C9H
PMU Polarity Register	CAH
PMU Output Register	CBH
PMU Doze Timer Register	CCH
PMU Sleep Timer Register	CDH
PMU Suspend Timer Register	CEH
Reserved	CFH - D9H
Reserved	DAH
PMU Activity Status Register	DBH
PMU NMI Status Register	DCH
PMU Resume Control Register	DDH
Clock Control Register	DEH
SmartClock Activity Mask Register	DFH

Table 16-3. VG330 Indexed Registers - Primary Group

Register	Index
SmartClock Inactive Step Register	E0H
SmartClock Active Step Register	E1H
SmartClock Activity Level Register	E2H
SmartClock Control Register	E3H
Suspend/Refresh Control register	E4H
Reserved	E5H - E7H
BIOS Shadow RAM Address Register	E8H
BIOS Shadow RAM and EMS Control Register	E9H
Reserved	EAH - FFH

For listing and description of VG330 LCD Controller Unit - Registers, refer to that section in this chapter.

For listing and description of VG330 PC Card Controller Unit Registers, refer to that section in this chapter.

Name	Revision Register
Type	Read only
Index	00H
Description	This register identifies the revision level of the VG330 silicon.
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
REVD							

D[7:0] **REVD**

VG330 Silicon revision number 02

Name BCG Mode Register

Type Read/Write

Index 01H

Description This register controls system clock divisors and bus management modes.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OSCDIV1	OSCDIV0	Reserved	LTCHADR	BINH	SDIV1	SDIV0

D7 **Reserved**

Default = 0.

D[6:5] **OSCDIV[1:0]**

Divisor for generating CPUCLK and Video Clock from input oscillator. These bits select the divisor applied to the input clock frequency generated by either the crystal on pins X1/X2 or external oscillator on X1:

OSCDIV1	OSCDIV0	CPUCLK and Video Clock Divisor
0	0	X1 frequency
0	1	X1 frequency divided by 2 (default)
1	0	X1 frequency divided by 3
1	1	X1 frequency divided by 4

D4 **Reserved**

Default = 0.

D3 **LTCHADR**

Enable Address Latch Mode. Default = 0. In order to enable Address Latch mode, both bits D3 and D2 must be set to ‘1’.

D2 **BINH**

Enable Bus Inhibit Mode.
0 = Disable Bus Inhibit Mode (default)
1 = Enable Bus Inhibit Mode

D[1:0] **SDIV[1:0]**

ISA bus clock divisor select. These bits select the divisor applied to the CPUCLK frequency for generating the ISA bus clock, SYSCLK.

SDIV1	SDIV0	SYSCLK Divisor
0	0	CPUCLK / 4
0	1	CPUCLK / 3
1	0	CPUCLK / 2 (default)
1	1	Reserved setting

Name Memory Control 1 Register

Type Read/Write

Index 04H

Description This register defines the configuration of memory by setting the type of RAM memory used.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MAPEN	BANK2	BANK1	BANK0	MTYP3	MTYP2	MTYP1	MTYP0

D7 **MAPEN**

Enable Global Memory Mapping. Default = 0.

0 = Disable all of the Memory Mapping registers.
1 = Enable the Memory Mapping registers.

D[6:4] **BANK**

RAM bank select bits. Default = 111.

These bits specify the number of RAM banks installed, as follows. A bank is defined as a set of memory devices that are a total of 16 bits wide. Thus, either one x16 device, or two 8-bit devices, or four x4 devices can constitute a bank.

Set BANK as follows:

Number of Banks	BANK
1	000
2	001
3	010
4	011
5	100
6	101

Note 1: The default value is a reserved setting which is used during system initialization only; for normal operation, the system programmer must set it to match the system memory configuration. This register must be initialized in order for the to work, because RAM usage depends on its settings. Values of 7 or 8 are not valid values.

Note 2: If SRAM or PSRAM is selected, any memory above the last bank in the RAM addressing space is treated as Flash memory, is automatically accessed using Flash cycle types, and is controlled using the MCx Chip Select lines.

Note 3: The BANK bits also determine the physical location of the Display Buffer Area.

D[3:0] **MTYP**

RAM Type Select bits. Default = 0000.

These bits specify the type and density of RAM and are decoded as follows:

MTYP3	MTYP2	MTYP1	MTYP0	Density	Type
0	0	0	0	Reserved	
SRAM					
0	0	0	1	128K x 8	SRAM
0	0	1	0	512K x 8	SRAM
0	0	1	1	Reserved	
PSRAM[a]					
0	1	0	0	128K x 8	PSRAM[a]
0	1	0	1	512K x 8	PSRAM
0	1	1	0	Reserved	
DRAM[b]					
0	1	1	1	512K x 8	DRAM
1	0	0	0	1M x 4	DRAM
1	0	0	1	4M x 4	DRAM
1	0	1	0	256K x 16	DRAM
1	0	1	1	1M x 16	DRAM
1	1	0	0	2M x 8	DRAM
Reserved					
1	1	0	1	Reserved	
1	1	1	X	Reserved	

[a] The VG330 automatically refreshes DRAM and PSRAM when system is ON. However, PSRAM will be placed in self-refresh mode when suspended.

[b] Note that this RAM is refreshed by page mode cycles during LCD refresh.

Name	Memory Control 2 Register
Type	Read/Write
Index	05H
Description	This register defines the size of ROM used.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	ROM0SIZ	ROM1SIZ	Reserved	Reserved	Reserved	Reserved	Reserved

D7 **Reserved**

Reserved bit. Default = 0.

D6 **ROM0SIZ**

ROM 0 Size bit.

This bit is read only; it reflects the state of the ROM8/$\overline{16}$ pin.

0 = ROM 0 data is 16 bits.
1 = ROM 0 data is 8 bits.

D5 **ROM1SIZ**

ROM 1 Size bit. Default = 0.

This bit defines the ROM 1 data width.

0 = ROM 1 data is 16 bits. (Default)
1 = ROM 1 data is 8 bits.

D[4:0] **Reserved**

Reserved bits. Default = 00000.

Name Alternate Display Buffer Start Address Register
Type Read/Write
Index 06H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
ALTDBREN	DBA21	DBA20	DBA19	DBA18	DBA17	DBA16	DBA15

D7 **ALTDBREN**

Enable Alternate Display Buffer.

0 = Disable the Alternate Display Buffer. (Default)
1 = Enable the Alternate Display Buffer.

When the alternate buffer is enabled, the LCD is refreshed from the memory location in the upper-most RAM memory bank pointed to by bits D[6:0] of this register.

When the VG330 is in 640x200 or 640x400 video mode, CPU accesses to B8000H-BFFFFH memory will still access the last Kilobyte block in the last RAM bank.

When in 640x480 video mode, CPU access to A0000H-AFFFFH memory will still access the last 64 Kilobyte block in the last RAM bank.

D[6:0] **DBA**

Alternate Display Buffer Start Address bits. Default = 0000000B.

These bits determine the starting address in the upper-most RAM memory bank where the alternate display buffer will reside.

Name LCD Configuration Control Register
Type Read/Write
Index 07H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{ENALCD}}$	VIDSPD1	VIDSPD0	Reserved	Reserved	Reserved	Reserved	Reserved

D7 **$\overline{\text{ENALCD}}$**

Enable LCD Controller. Default = 0

0 = Enable the VG330 LCD Controller.
1 = Disable the LCD Controller and free the memory address range from B8000H - BFFFFH for use by devices on the Expansion bus.

D[6:5] **VIDSPD**

Select video access speed. Default = 00.

These bits determine the number of clocks cycles required to complete one video refresh memory access.

Value		Fast Page Mode RAM (All values expressed in number of CPUCLK cycles)			
D6	**D5**	**$\overline{\text{RAS}}$ Precharge**	**$\overline{\text{RAS}}$**	**$\overline{\text{CAS}}$ Precharge**	**$\overline{\text{CAS}}$**
0	0	2[a]	2[a]	0.5	1.5
0	1	3	3	0.5	1.5
1	0	3	4	1.0	2
1	1	N/A			

[a] A first DRAM/fast Page Mode access is actually RAS/ CAS, followed by CAS precharge and CAS cycles.

Value		PSRAM/SRAM	
D6	**D5**	**Precharge**	**CS**
0	0	1.5	2.5
0	1	2	3
1	0	2	4
1	1	2.5	5.5

D[4:0] **Reserved**

Reserved bits. Default = 00000.

Name	ICU Mode Register
Type	Read/Write
Index	0DH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
IRAS2	IRAS1	IRAS0	Reserved	IRBS2	IRBS1	IRBS0	Reserved

D[7:5] **IRAS**

Select IRQA assignment. These bits assign an interrupt to IRQA.

IRAS2	IRAS1	IRAS0	IRQ
0	0	0	IRQA input disabled. (Default)
0	0	1	1
0	1	0	reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

D4 **Reserved**

Reserved bit. Default = 0.

D[3:1] **IRBS**

Select IRQB assignment. These bits assign an interrupt to IRQB.

IRBS2	IRBS1	IRBS0	IRQ
0	0	0	IRQB input disabled. (Default)
0	0	1	1
0	1	0	reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

D0 **Reserved**

Reserved bit. Default = 0.

Name SIO Clock Control Register

Type Read/Write

Index 0FH

Description Bits D[3:0] control the time that the SIO clock is low, and bits D[7:4] control the time that the SIO clock is high.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SHCNT3	SHCNT2	SHCNT1	SHCNT0	SLCNT3	SLCNT2	SLCNT1	SLCNT0

D[7:4] **SHCNT**

SIO clock high count. Default = 1000B.

These bits are used to control the SIO clock high pulse width. SIO clock high may be set from 1 to 16 times (X1 input) clock cycles.

D[3:0] **SLCNT**

SIO clock low count. Default = 1000B.

These bits are used to control the SIO clock low pulse width. SIO clock low may be set from 1 to 16 times (X1 input) clock cycles.

The shortest clock period that can be programmed is 2 times the X1 clock input. (Nominally that input is 32 MHz.) The longest period that can be programmed is 32 times the X1 clock.

If:

L is the count programmed into bits D3 - D0.

H is the count programmed into bits D7 - D4.

F is the frequency of the X1 clock.

Then the output frequency = F / ((L+H+2)

For example, if the X1 clock input is 32 MHZ, and
L = 7 and H = 7, then the output frequency is 2 MHZ.

Name	SIO Mode Register
Type	Read/Write
Index	10H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
SIOENA	IRCLKSGL	HPIREN	TXDSEL	SPSEL1	SPSEL0	SIRQS1	SIRQS0

D7 **SIOENA**

Enable SIO. Enables or disables the serial port.

If the serial port is enabled, the selected interrupt will be generated when interrupt enabled at the serial controller.

If the serial port is disabled, the clock to the UART is gated off, and the selected interrupt can be used for some other function.

0 = Disable internal Serial Port
1 = Enable internal Serial Port (Default)

D6 **IRCLKSGL**

Select IR clock source.

0 = IR Clock operates at 1.8432mhz (Default)
1 = IR Clock is driven at UART baudout

D5 **HPIREN**

Enable HP SIR operation of serial lines.

0 = TXD and RXD signals operate as normal serial signals.(Default)
1 = TXD and RXD signals operate as HP SIR compatible interface signals.

D4 **TXDSEL**

Select TXD/RXD destination.

0 = TXD/RXD enabled on TXD/RXD pins. (Default)
1 = TXD/RXD enabled on GPIO pins. Programmer must then assign TXD/RXD to appropriate GPIO pins by programming GPIO configuration.

HPIREN	TXDSEL	Data format and Pin selection
0	0	Serial input/output on TXD/RXD pins
0	1	Serial I/O on selected GPIO pins
1	0	Serial I/O on TXD/RXD pins formatted HPSIR
1	1	Serial I/O on selected GPIO pins formatted HPSIR

D[3:2] **SPSEL**

Serial Port I/O address select bits. Default = 00.

These bits determine the I/O address of the serial port as follows:

SPSEL1	SPSEL0	Serial Port I/O Address
0	0	3F8H - 3FFH
0	1	2F8H - 2FFH
1	0	Reserved
1	1	2E8H - 2EFH

D[1:0] **SIRQS**

Serial Port interrupt select bits. Default = 10.

These bits assign an IRQ to the internal 16C450's interrupt as follows:

SIRQS1	SIRQS0	Serial Port IRQ
0	0	(reserved)
0	1	IRQ3
1	0	IRQ4 (Default)
1	1	IRQ7

Name	SIO Power Control Register
Type	Read/Write
Index	11H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INPMSK	TXDMSK	Reserved	TCLKSEL	TMO3	TMO2	TMO1	TMO0

D7 **INPMSK**

SIO input mask bit. Default = 0.

This bit enables high to low transitions on any of the SIO inputs, RXD, $\overline{\text{DCD}}$, $\overline{\text{RI}}$, $\overline{\text{DSR}}$, or $\overline{\text{CTS}}$, to retrigger the SIO activity timer. When the SIO activity timer expires, the clock to the internal 16C450 is stopped.

0 = Retrigger Serial Port timer on high to low transition of any SIO inputs.
1 = Mask SIO inputs from retriggering Serial Port timer.

D6 **TXDMSK**

SIO transmit buffer mask bit. Default = 0.

This bit enables writes to the SIO transmit buffer to retrigger the SIO activity timer. When the SIO activity timer expires, the clock to the internal 16C450 is stopped.

0 = Retrigger Serial Port timer on writes to the SIO transmit buffer.
1 = Mask writes to the SIO transmit buffer from retriggering Serial Port timer.

D5 **Reserved**

Reserved bit. Default = 0.

D4 **TCLKSEL**

SIO activity timer resolution. Default = 0.

This bit selects the SIO activity timer range and resolution.

0 = Serial Port activity timer range is from 1 to 15 sec. (1 sec. resolution).
1 = Serial Port activity timer range is from 8 sec. to 2 min. (8 second resolution).

D[3:0] **TMO**

SIO activity timer. Default = 0000B.

Setting this register to zero disables the SIO activity timer.

Name Timer Clock Control 1 Register

Type Read/Write

Index 12H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
THCNT3	THCNT2	THCNT1	THCNT0	TLCNT3	TLCNT2	TLCNT1	TLCNT0

D[7:4] **THCNT**

Timer clock high count. Default = 1000

These bits are used to control the TCLK high pulse width. TCLK high width = THCNT+1 and thmay be set from 1 to 16 times (X1 input) clock cycles.

D[3:0] **TLCNT**

Timer clock low count. Default = 1000

These bits are used to control the TCLK low pulse width. TCLK low width = TLCNT+1 and may be set from 1 to 16 times (X1 input) clock cycles.

Name Timer Clock Control 2 Register

Type Read/Write

Index 13H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
TCNT3	TCNT2	TCNT1	TCNT0	ALTLCNT3	ALTLCNT 2	ALTLCNT 1	ALTLCNT 0

D[7:4] **TCNT**

Timer clock count. Default = 1000.

These bits specify the number of TCLK cycles generated using the primary TCLK high and low pulse widths. Once TCNT+1 cycles have been generated, one TCLK cycle will be generated using the alternate TCLK low pulse specified by the ALTLCNT[3:0] bits of this register.

D[3:0] **ALTLCNT**

Alternate timer clock low count. Default = 1000.

These bits are used to control the TCLK low pulse width when the timer clock count expires. Alternate TCLK low width = ALTLCNT+1 and-may be set from 1 to 16 times (X1 input) clock cycles.

Discussion

The timer clock, TCLK, is derived from the main VG330 high frequency input clock as supplied to the X1 pin by either an external oscillator or a crystal.

In order to support the standard TCLK frequency of 1.19318 MHz from various clock frequencies that can be supplied to the X1 pin, TCLK is generated from a set of programmable dividers specifying a TCLK high pulse width, both primary and alternate TCLK low pulse widths, and a primary TCLK count.

For the number of TCLK cycles specified by bits D[7:4] of the Timer Clock Control 2 Register, the TCLK high pulse width will be controlled by bits D[7:4] and the TCLK low pulse width will be controlled by bits D[3:0] of the Timer Clock Control 1 Register. The minimum TCLK high or low pulse width is one X1 clock period and the maximum TCLK high or low pulse width is 16 times (X1 input) clock periods.

After the number of TCLK cycles specified by bits D[7:4] of the Timer Clock Control 2 Register have been generated, the next TCLK low pulse width will be controlled by bits D[3:0] of the Timer Clock Control 2 Register.

Name Address Pin Configuration Register 1

Type Read/Write

Index 14H

Description This register sets the configuration for address pins A23 and A22. Note that Address pins A23 and A22 are always active for PC Card cycles. If a particular address pin is not enabled for RAM, ROM0, or ROM1, then that pin is defined as a direct connection to the PC Card slot and will be made high impedance when PC Card power is off.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
A23_ RAMEN	A23_ ROM0EN	A23_ ROM1EN	Reserved	A22_ RAMEN	A22_ ROM0EN	A22_ ROM1EN	Reserved

D7 **A23_RAMEN**

Address pin A23 RAM enable. Default = 0.

This bit defines the behavior of the A23 pin during RAM cycles.

0 = A23 driven by mapper address or zero during RAM cycles.
1 = A23 driven with latched value of last address during RAM cycles.

D6 **A23_ROM0EN**

Address pin A23 ROM0 enable. Default = 0.

This bit defines the behavior of the A23 pin during ROM0 cycles.

0 = A23 driven by mapper address during ROM0 cycles.
1 = A23 driven with latched value of last address during ROM0 cycles.

D5 **A23_ROM1EN**

Address pin A23 ROM1 enable. Default = 0.

This bit defines the behavior of the A23 pin during ROM1 cycles.

0 = A23 driven by mapper address during ROM1 cycles.
1 = A23 driven with latched value of last address during ROM1 cycles.

D4 **Reserved**

Reserved bit. Default = 0.

D3 **A22_RAMEN**

Address pin A22 RAM enable. Default = 0.

This bit defines the behavior of the A22 pin during RAM cycles.

0 = A22 driven by mapper address or zero during RAM cycles.
1 = A22 driven with latched value of last address during RAM cycles.

D2 **A22_ROM0EN**

Address pin A22 ROM0 enable. Default = 0.

This bit defines the behavior of the A22 pin during ROM0 cycles.

0 = A22 driven by mapper address or zero during ROM0 cycles.
1 = A22 driven with latched value of last address during ROM0 cycles.

D1 **A22_ROM1EN**

Address pin A22 ROM1 enable. Default = 0.

This bit defines the behavior of the A22 pin during ROM1 cycles.

0 = A22 driven by mapper address during ROM1 cycles.
1 = A22 driven with latched value of last address during ROM1 cycles.

D0 **Reserved**

Reserved bit. Default = 0.

Name Address Pin Configuration Register 2

Type Read/Write

Index 15H

Description This register sets the configuration for address pins A21 and A20. Note that Address pins A21 and A20 are always active for PC Card cycles. If a particular address pin is not enabled for RAM, ROM0, or ROM1, then that pin is defined as a direct connection to the PC Card slot and will be made high impedance when PC Card power is off.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
A21_ RAMEN	A21_ ROM0EN	A21_ ROM1EN	Reserved	A20_ RAMEN	A20_ ROM0EN	A20_ ROM1EN	Reserved

D7 **A21_RAMEN**

Address pin A21 RAM enable. Default = 0.

This bit defines the behavior of the A21 pin during RAM cycles.

0 = A21 driven by mapper address or zero during RAM cycles.
1 = A21 driven with latched value of last address during RAM cycles.

D6 **A21_ROM0EN**

Address pin A21 ROM0 enable. Default = 0.

This bit defines the behavior of the A21 pin during ROM0 cycles.

0 = A21 driven by mapper address during ROM0 cycles.
1 = A21 driven with latched value of last address during ROM0 cycles.

D5 **A21_ROM1EN**

Address pin A21 ROM1 enable. Default = 0.

This bit defines the behavior of the A21 pin during ROM1 cycles.

0 = A21 driven by mapper address during ROM1 cycles.
1 = A21 driven with latched value of last address during ROM1 cycles.

D4 **Reserved**

Reserved bit. Default = 0.

D3 **A20_RAMEN**

Address pin A20 RAM enable. Default = 0.

This bit defines the behavior of the A20 pin during RAM cycles.

0 = A20 driven by mapper address or zero during RAM cycles.
1 = A20 driven with latched value of last address during RAM cycles.

D2 **A20_ROM0EN**

Address pin A20 ROM0 enable. Default = 0.

This bit defines the behavior of the A20 pin during ROM0 cycles.

0 = A20 driven by mapper address or zero during ROM0 cycles.

1 = A20 driven with latched value of last address during ROM0 cycles.

D1 **A20_ROM1EN**

Address pin A20 ROM1 enable. Default = 0.

This bit defines the behavior of the A20 pin during ROM1 cycles.

0 = A20 driven by mapper address during ROM1 cycles.
1 = A20 driven with latched value of last address during ROM1 cycles.

D0 **Reserved**

Reserved bit. Default = 0.

Name Address and Data Pin Control Register 3

Type Read/Write

Index 16H

Description This register sets the configuration for address pins A[19:12] and also controls Data Clamping and Data Hold.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
DRAMEN	EXP_IOEN	Reserved	Reserved	DCLMP_EN	DHLD_EN	Reserved	Reserved

D7 **DRAMEN**

Address pins A[19:12] DRAM enable. Default = 0.

This bit defines the behavior of the A[19:12] pins during DRAM cycles.

0 = A[19:12] driven by mapper address or zero during DRAM cycles.
1 = A[19:12] driven with latched value of last address during DRAM cycles.

D6 **EXP_IOEN**

Address pins A[19:16] I/O enable. Default = 0.

This bit defines the behavior of the A[19:16] pins during I/O cycles.

0 = A[19:16] driven low by CPU during I/O cycles.
1 = A[19:16] driven with latched value of last address during I/O cycles.

D[5:4] **Reserved**

Reserved bits. Default = 0.

D3 **DCLMP_EN**

Enable Data Clamp. Default = 0.

This bit defines the behavior of the D[15:0] pins during processor stop clock modes.

0 = D[15:0] driven to high-impedance state during processor stop clock modes.
1 = D[15:0] driven low during processor stop clock modes.

D2 **DHLD_EN**

Enable Data Hold. Default = 0.

This bit defines the behavior of the D[15:0] pins during idle bus cycles.

0 = D[15:0] driven to high-impedance state during idle cycles.
1 = D[15:0] driven with last value read from or written to bus during idle cycles.

D[1:0] **Reserved**

Reserved bits. Default = 0.

Name Main NMI Status Register
Type Read/Write
Index 19H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	PCS2_ NMI	PCS1_ NMI	PCS0_ NMI	KBD_NMI	PMU_NMI

D[7:5] **Reserved**

Reserved bits. Default = 000.

D4 **PCS2_NMI**

0 = NMI did not occur.
1 = This bit is set to 1 if Programmable Chip Select 2, NMI occurred.

D3 **PCS1_NMI**

0 = NMI did not occur.
1 = This bit is set to 1 if Programmable Chip Select 1, NMI occurred.

D2 **PCS0_NMI**

0 = NMI did not occur.
1 = This bit is set to 1 if Programmable Chip Select 0, NMI occurred.

D1 **KBD_NMI**

0 = NMI did not occur.
1 = This bit is set to 1 if NMI was generated by Keyboard.

D0 **PMU_NMI**

0 = NMI did not occur.
1 = This bit is set to 1 if NMI was generated by PMU.

Name Programmable Chip Select 0 Mode Register

Type Read/Write

Index 20H

Description Control register for PCS0.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
PCS0_ MIOB	Reserved	PCS0_ DSIZE	PCS0_ MON	PCS0_ NMIMD1	PCS0_ NMIMD0	PCS0_ CSMD1	PCS0_ CSMD0

D7 **PCS0_MIOB**

Function select: Memory or I/O Chip Select.

0 = Enable I/O chip select decode. (Default)
1 = Enable Memory chip select decode.

D6 **Reserved**

Reserved bit. Default = 0.

D5 **PCS0_DSIZE**

Programmable Chip Select 0 Data Size.

0 = 8-bit data path. 8-bit cycles are generated unless $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$ is returned from the device. (Default)
1 = 16-bit data path. $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ are ignored and only 16-bit cycles are generated for the device.

D4 **PCS0_MON**

Enable PCS0 Activity Monitor.

0 = Disable activity from retriggering timer. (Default)
1 = Setting this bit to 1 enables allowing activity on this Programmable Chip Select to retrigger the PMU activity timer.

D[3:2] **PCS0_NMIMD**

Enable/Select NMI Mode for PCS0.

These bits may be set to enable NMI during Programmable Chip Select activity and are decoded as follows:

PCS0_ NMIMD1	PCS0_ NMIMD0	NMI Mode
0	0	Disabled. NMI is not generated during Programmable Chip Select 0. (Default)
0	1	NMI enabled for I/O or Memory read cycles.
1	0	NMI enabled for I/O or Memory write cycles.
1	1	NMI enabled for I/O or Memory read and write cycles.

D[1:0] **PCS0_CSMD**

Chip Select 0 Mode.

These bits are set to select the operation of the Programmable Chip Select 0 and are decoded as follows:

PCS0_ CSMD1	PCS0_ CSMD0	Chip Select Mode
0	0	Disabled. Programmable Chip Select 0 is not generated. (Default)
0	1	Chip Select 0 is qualified with I/O or Memory read strobe.
1	0	Chip Select 0 is qualified with I/O or Memory write strobe.
1	1	Chip Select 0 is generated from address decode only.

Name Programmable Chip Select 0 Address Start Register

Type Read/Write

Index 21H

Description This register sets the starting address (the lower bound) for PCS0 activation.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
PCS0_STARTA[7:0]							

D[7:0] **PCS0_STARTA**

I/O or Memory Chip Select 0 Start Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and are set to specify the start of the I/O chip select address. For memory chip selects these bits represent A[15:8] and are set to specify the start of the memory chip select address.

Name	Programmable Chip Select 0 Address Stop Register
Type	Read/Write
Index	22H
Description	This register sets the ending address (the upper bound) for PCS0 activation.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
PCS0_STOPA[7:0]							

D[7:0] **PCS0_STOPA**

I/O or Memory Chip Select 0 Stop Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and are set to specify the end of the I/O chip select address. This provides a minimum I/O chip select range of 1 byte and a maximum range of 256 bytes. For memory chip selects these bits represent A[15:8] and are set to specify the end of the memory chip select address. This provides a minimum memory chip select range of 256 bytes and a maximum range of 64 Kilobytes.

Name	Programmable Chip Select 0 Address High Register
Type	Read/Write
Index	23H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PCS0_HIGHA[7:0]							

D[7:0] **PCS0_HIGHA**

I/O or Memory Chip Select 0 High Address. Default = 0.

For I/O chip selects, these bits are compared with A[15:8] to enable the I/O chip select. For memory chip selects, PCS0_HIGHA[7:4] are ignored and PCS0_HIGHA[3:0] are compared with A[19:16] to enable the memory chip select.

Name	Programmable Chip Select 1 Mode Register
Type	Read/Write
Index	24H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
PCS1_ MIOB	Reserved	PCS1_ DSIZE	PCS1_ MON	PCS1_ NMIMD1	PCS1_ NMIMD0	PCS1_ CSMD1	PCS1_ CSMD0

D7 **PCS1_MIOB**

Function select: Memory or I/O Chip Select.

0 = Enable I/O chip select decode. (Default)
1 = Enable Memory chip select decode.

D6 **Reserved**

Reserved bit. Default = 0.

D5 **PCS1_DSIZE**

Programmable Chip Select 1 Data Size.

0 = 8-bit data path. 8-bit cycles are generated unless $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$ is returned from the device. (Default)
1 = 16-bit data path. $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ are ignored and only 16-bit cycles are generated for the device.

D4 **PCS1_MON**

Enable PCS1 Activity Monitor.

0 = Disable activity from retriggering timer. (Default)
1 = Setting this bit to 1 enables allowing activity on this Programmable Chip Select to retrigger the PMU activity timer.

D[3:2] **PCS1_NMIMD**

Enable/Select NMI Mode for PCS1.

These bits may be set to enable NMI during Programmable Chip Select activity and are decoded as follows:

PCS0_ NMIMD1	PCS0_ NMIMD0	NMI Mode
0	0	Disabled. NMI is not generated during Programmable Chip Select 1. (Default)
0	1	NMI enabled for I/O or Memory read cycles.
1	0	NMI enabled for I/O or Memory write cycles.
1	1	NMI enabled for I/O or Memory read and write cycles.

D[1:0] **PCS1_CSMD**

Chip Select 1 Mode.

These bits are set to select the operation of the Programmable Chip Select 1 and are decoded as follows:

PCS1_ CSMD1	PCS1_ CSMD0	Chip Select Mode
0	0	Disabled. Programmable Chip Select 1 is not generated. (Default)
0	1	Chip Select 1 is qualified with I/O or Memory read strobe.
1	0	Chip Select 1 is qualified with I/O or Memory write strobe.
1	1	Chip Select 1 is generated from address decode only.

Name	Programmable Chip Select 1 Address Start Register
Type	Read/Write
Index	25H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PCS1_STARTA[7:0]							

D[7:0] **PCS1_STARTA**

I/O or Memory Chip Select 1 Start Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and they are set to specify the start of the I/O chip select address.

For memory chip selects these bits represent A[15:8] and they are set to specify the start of the memory chip select address.

Name Programmable Chip Select 1 Address Stop Register

Type Read/Write

Index 26H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
PCS1_STOPA[7:0]							

D[7:0] **PCS1_STOPA**

I/O or Memory Chip Select 1 Stop Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and are set to specify the end of the I/O chip select address. This provides a minimum I/O chip select range of 1 byte and a maximum range of 256 bytes. For memory chip selects these bits represent A[15:8] and are set to specify the end of the memory chip select address. This provides a minimum memory chip select range of 256 bytes and a maximum range of 64 Kilobytes.

Name	Programmable Chip Select 1 Address High Register
Type	Read/Write
Index	27H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PCS1_HIGHA[7:0]							

D[7:0] **PCS1_HIGHA**

I/O or Memory Chip Select 1 High Address. Default = 0.

For I/O chip selects, these bits are compared with A[15:8] to enable the I/O chip select.

For memory chip selects, PCS1_HIGHA[7:4] are ignored and PCS1_HIGHA[3:0] are compared with A[19:16] to enable the memory chip select.

Name	Programmable Chip Select 2 Mode Register
Type	Read/Write
Index	28H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
PCS2_ MIOB	Reserved	PCS2_ DSIZE	PCS2_ MON	PCS2_ NMIMD1	PCS2_ NMIMD0	PCS2_ CSMD1	PCS2_ CSMD0

D7 **PCS2_MIOB**

Function select: Memory or I/O Chip Select.

0 = Enable I/O chip select decode. (Default)
1 = Enable Memory chip select decode.

D6 **Reserved**

Reserved bit. Default = 0.

D5 **PCS2_DSIZE**

Programmable Chip Select 2 Data Size.

0 = 8-bit data path. 8-bit cycles are generated unless $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$ is returned from the device. (Default)
1 = 16-bit data path. $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ are ignored and only 16-bit cycles are generated for the device.

D4 **PCS2_MON**

PCS2 Activity Monitor Enable.

0 = Disable activity from retriggering timer. (Default)
1 = Setting this bit to 1 enables allowing activity on this Programmable Chip Select to retrigger the PMU activity timer.

D[3:2] **PCS2_NMIMD**

Enable/Select NMI Mode for PCS2.

These bits may be set to enable NMI during Programmable Chip Select activity and are decoded as follows:

PCS2_ NMIMD1	PCS2_ NMIMD0	NMI Mode
0	0	Disabled. NMI is not generated during Programmable Chip Select 2. (Default)
0	1	NMI enabled for I/O or Memory read cycles.
1	0	NMI enabled for I/O or Memory write cycles.
1	1	NMI enabled for I/O or Memory read and write cycles.

D[1:0] **PCS2_CSMD**

Chip Select 2 Mode.

These bits are set to select the operation of the Programmable Chip Select 2 and are decoded as follows:

PCS2_ CSMD1	PCS2_ CSMD0	Chip Select Mode
0	0	Disabled. Programmable Chip Select 2 is not generated. (Default)
0	1	Chip Select 2 is qualified with I/O or Memory read strobe.
1	0	Chip Select 2 is qualified with I/O or Memory write strobe.
1	1	Chip Select 2 is generated from address decode only.

Name Programmable Chip Select 2 Address Start Register

Type Read/Write

Index 29H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
PCS2_STARTA[7:0]							

D[7:0] **PCS2_STARTA**

I/O or Memory Chip Select 2 Start Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and are set to specify the start of the I/O chip select address.

For memory chip selects these bits represent A[15:8] and are set to specify the start of the memory chip select address.

Name	Programmable Chip Select 2 Address Stop Register
Type	Read/Write
Index	2AH
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PCS2_STOPA[7:0]							

D[7:0] **PCS2_STOPA**

I/O or Memory Chip Select 2 Stop Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and are set to specify the end of the I/O chip select address. This provides a minimum I/O chip select range of 1 byte and a maximum range of 256 bytes.

For memory chip selects these bits represent A[15:8] and are set to specify the end of the memory chip select address. This provides a minimum memory chip select range of 256 bytes and a maximum range of 64 Kilobytes.

Name	Programmable Chip Select 2 Address High Register
Type	Read/Write
Index	2BH
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PCS2_HIGHA[7:0]							

D[7:0] **PCS2_HIGHA**

I/O or Memory Chip Select 2 High Address. Default = 0.

For I/O chip selects, these bits are compared with A[15:8] to enable the I/O chip select.

For memory chip selects, PCS2_HIGHA[7:4] are ignored and PCS2_HIGHA[3:0] are compared with A[19:16] to enable the memory chip select.

Name	Alternate PCS Mode Register
Type	Read/Write
Index	2CH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
MIOB	Reserved	DSIZE	MONITOR	SELCS1	SELCS0	CSMD1	CSMD0

D7 **MIOB**

Function select: Memory or I/O Chip Select.

0 = Enable I/O chip select decode. (Default)
1 = Enable Memory chip select decode.

D6 **Reserved**

Reserved bit. Default = 0.

D5 **DSIZE**

Programmable Chip Select Data Size.

0 = 8-bit data path. 8-bit cycles are generated unless $\overline{\text{IOCS16}}$ or $\overline{\text{MEMCS16}}$ is returned from the device. (Default)
1 = 16-bit data path. $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ are ignored and only 16-bit cycles are generated for the device.

D4 **MONITOR**

Enable Alternate PCS Activity Monitor.

0 = Disable activity from retriggering timer. (Default)
1 = Setting this bit to 1 enables allowing activity on this Programmable Chip Select to retrigger the PMU activity timer.

D[3:2] **SELCS**

PCS Select.

These bits allow the alternate Programmable Chip Select to be AND'ed with one of PCS[2:0] as follows:

SELCS1	SELCS0	Alternate Programmable Chip Select AND'ed with
0	0	$\overline{\text{PCS0}}$
0	1	Reserved
1	0	$\overline{\text{PCS2}}$
1	1	None. (Default)

D[1:0] **CSMD**

Chip Select Mode.

These bits are set to select the operation of the Programmable Chip Select and are decoded as follows:

CSMD1	CSMD0	Chip Select Mode
0	0	Disabled. Programmable Chip Select is not generated. (Default)
0	1	Chip Select qualified with I/O or Memory read strobe.
1	0	Chip Select qualified with I/O or Memory write strobe.
1	1	Chip Select generated from address decode only.

Name	Alternate PCS Address Start Register
Type	Read/Write
Index	2DH
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
STARTA							

D[7:0] **STARTA**

I/O or Memory Chip Select Start Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and they are set to specify the start of the I/O chip select address.

For memory chip selects these bits represent A[15:8] and they are set to specify the start of the memory chip select address.

Name	Alternate PCS Address Stop Register
Type	Read/Write
Index	2EH
Description	
Bits	

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">STOPA</td></tr>
</table>

D[7:0] **STOPA**

I/O or Memory Chip Select Stop Address. Default = 0.

For I/O chip selects, these bits represent A[7:0] and they are set to specify the end of the I/O chip select address. This provides a minimum I/O chip select range of 1 byte and a maximum range of 256 bytes.

For memory chip selects these bits represent A[15:8] and they are set to specify the end of the memory chip select address. This provides a minimum memory chip select range of 256 bytes and a maximum range of 64 Kilobytes.

Name	Alternate PCS Address High Register
Type	Read/Write
Index	2FH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
HIGHA							

D[7:0] **HIGHA**

I/O or Memory Chip Select High Address. Default = 0.

For I/O chip selects, these bits are compared with A[15:8] to enable the I/O chip select. For memory chip selects, HIGHA[7:4] are ignored and HIGHA[3:0] are compared with A[19:16] to enable the memory chip select.

Name BIOS Time Base Low Register

Type Read/Write

Index 30H

Description The BIOS Time Base Registers allow a free-running timer clocked by TCLK to be read. This timer may be accessed through the BIOS Clock Interface calls.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
TMR[7:0]							

D[7:0] **TMR[7:0]**

Low byte of the BIOS timer count. Default = 0.

Name	BIOS Time Base High Register
Type	Read/Write
Index	31H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
TMR[15:8]							

D[7:0] **TMR[15:8]**

High byte of the BIOS timer count. Default = 0.

Name Expansion Bus Mode Register

Type Read/Write

Index 34H

Description This register controls system clock modes.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SCLK_MD1	SCLK_MD0	LODLY1	LODLY0	OE_INH	Reserved	Reserved	Reserved

D[7:6] **SCLK_MD[1:0]**

SYSCLK mode.

These bits determine the clocking mode of the Expansion bus clock, SYSCLK as follows.

SCLK_MD1	SCLK_MD0	SYSCLK Mode
0	0	**Clock Stop Mode. (default)** SYSCLK is normally stopped and only begins toggling when an Expansion bus cycle is requested.
0	1	**Clock Sync Mode**. SYSCLK is allowed to run continuously. When an Expansion bus cycle is requested, the start of the cycle may be delayed to synchronize the cycle with SYSCLK.
1	0	**Clock Stretch Mode.** SYSCLK is allowed to run continuously. When an Expansion bus cycle is requested, SYSCLK is stretched to synchronize it to the start of the cycle.
1	1	Reserved setting.

D[5:4] **LODLY[1:0]**

Expansion bus lead off delay.

These bits specify the delay applied to the start of all Expansion bus cycles. These bits allow additional address setup time to be provided for slow Expansion bus 16-bit memory devices.

LODLY1	LODLY0	Expansion bus lead off delay
0	0	None (default)
0	1	1 processor clock cycle
1	0	2 processor clock cycles
1	1	3 processor clock cycles

D3 **OE_INH**

ROM OE inhibit.

The $\overline{\text{OE}}$ pins of external ROM devices controlled by either $\overline{\text{ROMCE0}}$ or $\overline{\text{ROMCE1}}$ may be driven by the $\overline{\text{SMRD}}$ output.

0 = The $\overline{\text{SMRD}}$ pin will be asserted during reads from either ROM0 or ROM1. (Default)
1 = The $\overline{\text{SMRD}}$ pin will not be asserted during reads from either ROM0 or ROM1.

D[2:0] **Reserved bits.**

Default = 000.

Name Expansion Bus I/O Wait State Control Register
Type Read/Write
Index 35H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	IO_W2	IO_W1	IO_W0	Reserved	Reserved	Reserved	Reserved

D7 **Reserved**

Reserved bit. Default = 0.

D[6:4] **IO_W**

Expansion Bus I/O Wait State bits. Default = 100.

These bits specify the Expansion bus wait states added to all I/O cycles and are expressed in Expansion bus clock (SYSCLK) cycles. I/O wait states may be programmed to select from zero to 7 additional Expansion bus clock cycles.

The I/O command pulse width for zero wait state cycles is 1.5 Expansion bus clock cycles.

D[3:0] **Reserved**

Reserved bits. Default = 0000.

Name Expansion Bus Memory Wait State Control Register

Type Read/Write

Index 36H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	MEM8_W2	MEM8_W1	MEM8_W0	Reserved	MEM16_W2	MEM16_W1	MEM16_W0

D7 **Reserved**

Reserved bit. Default = 0.

D[6:4] **MEM8_W**

Expansion Bus 8-bit Memory Wait State bits. Default = 100.

These bits specify the Expansion bus wait states added to 8-bit memory cycles and are expressed as number of Expansion bus clock (SYSCLK) cycles. 8-bit memory wait states may be programmed to select from zero to 7 additional Expansion bus clock cycles.

The 8-bit memory command pulse width for zero wait state cycles is 1.5 Expansion bus clock cycles.

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **MEM16_W**

Expansion Bus 16 bit Memory Wait State bits. Default = 100.

These bits specify the Expansion bus wait states added to 16-bit memory cycles and are expressed in Expansion bus clock (SYSCLK) cycles. 16-bit memory wait states may be programmed to select from zero to 7 additional Expansion bus clock cycles.

The 16-bit memory command pulse width for zero wait state cycles is 2 Expansion bus clock cycles.

Name Top of Memory Register
Type Read/Write
Index 38H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
BUF16K	Reserved	BA19	BA18	BA17	BA16	BA15	BA14

D7 **BUF16K**

Display buffer size. Default = 0.

0 = Display buffer is 32 Kilobytes.
1 = Display buffer is 16 Kilobytes.

D6 **Reserved**

Reserved bit. Default = 0.

D[5:0] **BA[19:14]**

Top of memory. Default = 101000.

For systems which provide less than 640 Kilobytes of RAM, this register must be set to indicate the starting address of physical RAM reserved for the display buffer.

Once set, all accesses to memory between this address and 9FFFFH will be inhibited except through the space at B8000H - BFFFFH, or VGA address space at A0000H-AFFFFH, or the memory mapping registers.

Name Primary Interrupt Controller - ICU Shadow Register
Type Read/Write
Index 40H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	PICU_ BUSY	PINIT	PPOLL	ISR

D[7:4] **Reserved**

Reserved bit. Default = 0000.

D3 **PICU_BUSY**

Primary interrupt controller busy status. Default = 0.

This bit is set to ‘1’ while either bit D2 or D1 of this register is high.

D2 **PINIT**

Status: Primary interrupt controller initialization in progress.

0 = This bit is cleared to zero when Initialization Command Word 4 (ICW4) is written to the interrupt controller. (Default)
1 = This bit is set to ‘1’ when an Initialization Command Word 1 (ICW1) is written to the primary interrupt controller.

D1 **PPOLL**

Interrupt controller programmed into POLL’ed mode.

0 = This bit is cleared to zero when port 20H of the interrupt controller has been read. (Default)
1 = Indicates the interrupt controller is programmed into polled mode.

D0 **ISR**

Interrupt IRR/ISR status.

This bit tracks the state of the interrupt controller’s In Service Register and Interrupt Request Register.

0 = Interrupt Request Register (IRR) is available from Interrupt Controller.(Default)
1 = In Service Register (ISR) is available from Interrupt Controller.

Name Secondary Interrupt Controller - ICU Shadow Register

Type Read/Write

Index 41H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SICU_ BUSY	SINIT	SPOLL	ISR

D[7:4] **Reserved**

Reserved bit. Default = 0000.

D3 **SICU_BUSY**

Secondary interrupt controller busy status. Default = 0.

This bit is set to ‘1’ while either bit D2 or D1 of this register is high.

D2 **SINIT**

Interrupt controller initialization in progress.

0 = This bit is cleared to zero when Initialization Command Word 4 (ICW4) is written to the interrupt controller. (Default)
1 = This bit is set to ‘1’ when an Initialization Command Word 1 (ICW1) is written to the primary interrupt controller.

D1 **SPOLL**

Secondary interrupt controller programmed into POLL’ed mode.

0 = This bit is cleared to zero when port 20H of the interrupt controller has been read. (Default)
1 = Indicates the interrupt controller is programmed into polled mode.

D0 **ISR**

Interrupt IRR/ISR status.

This bit tracks the state of the interrupt controller’s In Service Register and Interrupt Request Register.

0 = Interrupt Request Register (IRR) is available from Interrupt Controller. (Default)
1 = In Service Register (ISR) is available from Interrupt Controller.

Name	GPIO Group A Mode Register 1
Type	Read/Write
Index	50H
Description	This register determines GPIO pin functions.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	GPA7_MD2	GPA7_MD1	GPA7_MD0	GPA6_IRS	GPA6_MD2	GPA6_MD1	GPA6_MD0

D7 **Reserved**

Reserved bit. Default = 0.

D[6:4] **GPA7_MD**

GPIO_A7 function select. Default = 000

The function mapped to the GPIO_A7 pin is as follows:

GPA7_MD[2:0]			GPIO_A7 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input - IRQ10
0	1	0	Input - Keyboard Clock
0	1	1	Input - RET7
1	0	0	Output - General Purpose
1	0	1	Output - SYSCLK through
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN7

D3 **GPA6_IRS**

GPIO_A6 IRQ select bit. Used together with GPA6_MD selection of bit function to allow GPIO_A6 to be used as an IRQ source.

If GPA6_MD = 001 and this bit
= 0 then GPIO_A6 is routed to IRQ11. (Default)
= 1 then GPIO_A6 is routed to IRQ3.

D[2:0] **GPA6_MD**

GPIO_A6 function select. Default = 000.

The function mapped to the GPIO_A6 pin is as follows:

GPA6_MD[2:0]			GPIO_A6 Pin Function
0	0	0	Input - General Purpose (Default)
0	0	1	Input: if GPA6_IRS = 1, this is IRQ11; IF GPA6_IRS = 0, this is IRQ3.
0	1	0	Input - Keyboard Data
0	1	1	Input - RET6
1	0	0	Output - General Purpose
1	0	1	Output - $\overline{BHE}$
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN6

Name GPIO Group A Mode Register 2

Type Read/Write

Index 51H

Description This register determines GPIO pin functions.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPA5_IRS	GPA5_MD2	GPA5_MD1	GPA5_MD0	GPA4_IRS	GPA4_MD2	GPA4_MD1	GPA4_MD0

D7 **GPA5_IRS**

GPIO_A5 IRQ select bit.

Used together with GPA5_MD selection of bit function to allow GPIO_A5 to be used as an IRQ source.

If GPA5_MD = 001 and this bit
= 0 then GPIO_A5 is routed to IRQ12. (Default)
= 1 then GPIO_A5 is routed to IRQ4.

D[6:4] **GPA5_MD**

GPIO_A5 function select. Default = 000

The function mapped to the GPIO_A5 pin is as follows:

GPA5_MD[2:0]			GPIO_A5 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPA5_IRS = 1, this is IRQ4; IF GPA6_IRS = 0, this is IRQ12.
0	1	0	Input - $\overline{\text{IOCS16}}$ through GPIO A5
0	1	1	Input - RET5
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 0 through GPIO A5
1	1	1	Output - SCAN5

D3 **GPA4_IRS**

GPIO_A4 IRQ select bit. Used together with GPA4_MD selection of bit function to allow GPIO_A4 to be used as an IRQ source.

If GPA4_MD = 001 and this bit

= 0 then GPIO_A4 is routed to IRQ13. (Default)
= 1 then GPIO_A4 is routed to IRQ5.

D[2:0] **GPA4_MD**

GPIO_A4 function select. Default = 000.

The function mapped to the GPIO_A4 pin is as follows:

GPA4_MD[2:0]			GPIO_A4 Pin Function
0	0	0	Input - General Purpose (Default)
0	0	1	Input: if GPA4_IRS = 1, this is IRQ5; IF GPA4_IRS = 0, this is IRQ13.
0	1	0	Input - $\overline{\text{MEMCS16}}$
0	1	1	Input - RET4
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - LCD M
1	1	1	Output - SCAN4

Name GPIO Group A Mode Register 3

Type Read/Write

Index 52H

Description This register determines GPIO pin functions.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPA3_IRS	GPA3_MD2	GPA3_MD1	GPA3_MD0	GPA2_IRS	GPA2_MD2	GPA2_MD1	GPA2_MD0

D7 **GPA3_IRS**

GPIO_A3 IRQ select bit.

Used together with GPA3_MD selection of bit function to allow GPIO_A3 to be used as an IRQ source.

If GPA3_MD = 001 and this bit
= 0 then GPIO_A3 is routed to IRQ14. (Default)
= 1 then GPIO_A3 is routed to IRQ6.

D[6:4] **GPA3_MD**

GPIO_A3 function select. Default = 000

The function mapped to the GPIO_A3 pin is as follows:

GPA3_MD[2:0]			GPIO_A3 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPA3_IRS = 1, this is IRQ6; IF GPA6_IRS = 0, this is IRQ14.
0	1	0	Input - LB2
0	1	1	Input - RET3
1	0	0	Output - General Purpose
1	0	1	Output - SYSCLK
1	1	0	Reserved
1	1	1	Output - SCAN3

D3 **GPA2_IRS**

GPIO_A2 IRQ select bit. Used together with GPA2_MD selection of bit function to allow GPIO_A2 to be used as an IRQ source.

If GPA2_MD = 001 and this bit

= 0 then GPIO_A2 is routed to IRQ15. (Default)
= 1 then GPIO_A2 is routed to IRQ7.

D[2:0] **GPA2_MD**

GPIO_A2 function select. Default = 000.

The function mapped to the GPIO_A2 pin is as follows:

GPA2_MD[2:0]			GPIO_A2 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPA2_IRS = 1, this is IRQ7; IF GPA6_IRS = 0, this is IRQ15.
0	1	0	Input - GP_RXD
0	1	1	Input - RET2
1	0	0	Output - General Purpose
1	0	1	Output - $\overline{BHE}$
1	1	0	Output - LCD M
1	1	1	Output - SCAN2

Name	GPIO Group A Mode Register 4
Type	Read/Write
Index	53H
Description	This register determines GPIO pin functions.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	GPA1_MD2	GPA1_MD1	GPA1_MD0	Reserved	GPA0_MD2	GPA0_MD1	GPA0_MD0

D7 **Reserved**

Reserved bit. Default = 0.

D[6:4] **GPA1_MD**

GPIO_A1 function select. The function mapped to the GPIO_A1 pin is as follows:

GPA1_MD[2:0]			GPIO_A1 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input - $\overline{\text{IOCS16}}$
0	1	0	Input - Keyboard Data
0	1	1	Input - RET1
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN1

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **GPA0_MD**

GPIO_A0 function select, mapped as follows:

GPA0_MD[2:0]			GPIO_A0 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input - $\overline{\text{MEMCS16}}$
0	1	0	Input - Keyboard Clock
0	1	1	Input - RET0
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN0

Name GPIO Group B Mode Register 1
Type Read/Write
Index 54H
Description This register determines GPIO pin functions.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPB7_IRS	GPB7_MD2	GPB7_MD1	GPB7_MD0	Reserved	GPB6_MD2	GPB6_MD1	GPB6_MD0

D7 **GPB7_IRS**

GPIO_B7 IRQ select bit.

Used together with GPB7_MD[6:4] selection of bit function to allow GPIO_B7 to be used as an IRQ source.

If GPB7_MD = 001 and this bit
= 0 then GPIO_B7 is routed to IRQ9. (Default = 0)
= 1 then GPIO_B7 is routed to IRQ1

D[6:4] **GPB7_MD[2:0]**

GPIO_B7 function select. The function mapped to the GPIO_B7 pin is as follows:

GPB7_MD[2:0]			GPIO_B7 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB7_IRS = 1, this is IRQ1; IF GPB7_IRS = 0, this is IRQ9.
0	1	0	Input - GP_RXD
0	1	1	Input - RET15
1	0	0	Output - General Purpose
1	0	1	Output - SYSCLK
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN15

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **GPB6_MD[2:0]**

GPIO_B6 function select. The function mapped to the GPIO_B6 pin is as follows:

GPB6_MD[2:0]			GPIO_B6 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input - IRQ10
0	1	0	Input - LB2
0	1	1	Input - RET14
1	0	0	Output - General Purpose
1	0	1	Output - $\overline{\text{BHE}}$
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN14

Name GPIO Group B Mode Register 2
Type Read/Write
Index 55H
Description This register determines GPIO pin functions.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPB5_IRS	GPB5_MD2	GPB5_MD1	GPB5_MD0	GPB4_IRS	GPB4_MD2	GPB4_MD1	GPB4_MD0

D7 **GPB5_IRS**

GPIO_B5 IRQ select bit.

Used together with GPB5_MD[6:4] selection of bit function to allow GPIO_B5 to be used as an IRQ source.

If GPB5_MD = 001 and this bit
= 0 then GPIO_B5 is routed to IRQ11. (Default)
= 1 then GPIO_B5 is routed to IRQ3

D[6:4] **GPB5_MD[2:0]**

GPIO_B5 function select. The function mapped to the GPIO_B5 pin is as follows:

GPB5_MD[2:0]			GPIO_B5 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB5_IRS = 1, this is IRQ3; IF GPB5_IRS = 0, this is IRQ11.
0	1	0	Input - GP_RXD
0	1	1	Input - RET13
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 0
1	1	1	Output - SCAN13

D3 **GPB4_IRS**

GPIO_B4 IRQ select bit.

Used together with GPB4_MD[2:0] selection of bit function to allow GPIO_B4 to be used as an IRQ source.

If GPB4_MD = 001 and this bit
= 0 then GPIO_B4 is routed to IRQ12. (Default)
= 1 then GPIO_B4 is routed to IRQ4

D[2:0] **GPB4_MD[2:0]**

GPIO_B4 function select. The function mapped to the GPIO_B4 pin is as follows:

GPB4_MD[2:0]			GPIO_B4 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB4_IRS = 1, this is IRQ4; IF GPB4_IRS = 0, this is IRQ12.
0	1	0	Input - LB2
0	1	1	Input - RET12
1	0	0	Output - General Purpose
1	0	1	Output - GP_TXD through GPIO B4
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN12

Name GPIO Group B Mode Register 3

Type Read/Write

Index 56H

Description This register determines GPIO pin functions.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPB3_IRS	GPB3_MD2	GPB3_MD1	GPB3_MD0	GPB2_IRS	GPB2_MD2	GPB2_MD1	GPB2_MD0

D7 **GPB3_IRS**

GPIO_B3 IRQ select bit.

Used together with GPB3_MD[6:4] selection of bit function to allow GPIO_B3 to be used as an IRQ source.

If GPB3_MD = 001 and this bit
= 0 then GPIO_B3 is routed to IRQ13. (Default)
= 1 then GPIO_B3 is routed to IRQ5

D[6:4] **GPB3_MD[2:0]**

GPIO_B3 function select. The function mapped to the GPIO_B3 pin is as follows:

GPB3_MD[2:0]			GPIO_B3 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB3_IRS = 1, this is IRQ5; IF GPB3_IRS = 0, this is IRQ13.
0	1	0	Input - GP_RXD
0	1	1	Input - RET11
1	0	0	Output - General Purpose
1	0	1	Output - General Purpose
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN11

D3 **GPB2_IRS**

GPIO_B2 IRQ select bit.

Used together with GPB2_MD[2:0] selection of bit function to allow GPIO_B2 to be used as an IRQ source.

If GPB2_MD = 001 and this bit
= 0 then GPIO_B2 is routed to IRQ14. (Default)
= 1 then GPIO_B2 is routed to IRQ6

D[2:0] **GPB2_MD[2:0]**

GPIO_B2 function select. The function mapped to the GPIO_B2 pin is as follows:

GPB2_MD2			GPIO_B2 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB2_IRS = 1, this is IRQ6; IF GPB26_IRS = 0, this is IRQ14.
0	1	0	Input - LB2
0	1	1	Input - RET10
1	0	0	Output - General Purpose
1	0	1	Output - GP_TXD
1	1	0	Output - Programmable Chip Select 0
1	1	1	Output - SCAN10

Name GPIO Group B Mode Register 4

Type Read/Write

Index 57H

Description This register determines GPIO pin functions.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPB1_IRS	GPB1_MD2	GPB1_MD1	GPB1_MD0	Reserved	GPB0_MD2	GPB0_MD1	GPB0_MD0

D7 **GPB1_IRS**

GPIO_B1 IRQ select bit.

Used together with GPB1_MD[6:4] selection of bit function to allow GPIO_B1 to be used as an IRQ source.

If GPB1_MD = 001 and this bit
= 0 then GPIO_B1 is routed to IRQ15. (Default)
= 1 then GPIO_B1 is routed to IRQ7

D[6:4] **GPB1_MD[2:0]**

GPIO_B1 function select.

The function mapped to the GPIO_B1 pin is as follows:

GPB1_MD[2:0]			GPIO_B1 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPB1_IRS = 1, this is IRQ7; IF GPB1_IRS = 0, this is IRQ15.
0	1	0	Input - $\overline{\text{IOCS16}}$
0	1	1	Input - RET9
1	0	0	Output - General Purpose
1	0	1	Output - General Purpose
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN9

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **GPB0_MD[2:0]**

GPIO_B0 function select. The function mapped to the GPIO_B0 pin is as follows:

GPB0_MD[2:0]			**GPIO_B0 Pin Function**
0	0	0	Input - General Purpose (default)
0	0	1	Input - LB2
0	1	0	Input - $\overline{\text{MEMCS16}}$
0	1	1	Input - RET8
1	0	0	Output - General Purpose
1	0	1	Output - GP_TXD
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN8

Name GPIO Group C Mode Register 1
Type Read/Write
Index 58H
Description This register determines GPIO pin functions.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPC7_IRS	GPC7_MD2	GPC7_MD1	GPC7_MD0	Reserved	GPC6_MD2	GPC6_MD1	GPC6_MD0

D7 **GPC7_IRS**

GPIO_C7 IRQ select bit.

Used together with GPC7_MD[6:4] selection of bit function to allow GPIO_C7 to be used as an IRQ source.

If GPC7_MD = 001 and this bit
= 0 then GPIO_C7 is routed to IRQ9. (Default)
= 1 then GPIO_C7 is routed to IRQ1

D[6:4] **GPC7_MD[2:0]**

GPIO_C7 function select. The function mapped to the GPIO_C7 pin is as follows:

GPC7_MD[2:0]			GPIO_C7 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPC7_IRS = 1, this is IRQ1; IF GPC7_IRS = 0, this is IRQ9.
0	1	0	Input - LB2
0	1	1	Input - RET23
1	0	0	Output - General Purpose
1	0	1	Output - SYSCLK
1	1	0	Output - PC Card Memory Read
1	1	1	Output - SCAN23

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **GPC6_MD[2:0]**

GPIO_C6 function select. The function mapped to the GPIO_C6 pin is as follows:

GPC6_MD[2:0]			**GPIO_C6 Pin Function**
0	0	0	Input - General Purpose (default)
0	0	1	Input - IRQ10
0	1	0	Input - GP_RXD
0	1	1	Input - RET22
1	0	0	Output - General Purpose
1	0	1	Output - $\overline{BHE}$
1	1	0	Output - PC Card Memory Write
1	1	1	Output - SCAN22

Name	GPIO Group C Mode Register 2
Type	Read/Write
Index	59H
Description	This register determines GPIO pin functions.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
GPC5_IRS	GPC5_MD2	GPC5_MD1	GPC5_MD0	GPC4_IRS	GPC4_MD2	GPC4_MD1	GPC4_MD0

D7 **GPC5_IRS**

GPIO_C5 IRQ select bit.

Used together with GPC5_MD[6:4] selection of bit function to allow GPIO_C5 to be used as an IRQ source.

If GPC5_MD = 001 and this bit
= 0 then GPIO_C5 is routed to IRQ11. (Default)
= 1 then GPIO_C5 is routed to IRQ3

D[6:4] **GPC5_MD[2:0]**

GPIO_C5 function select. The function mapped to the GPIO_C5 pin is as follows:

GPC5_MD[2:0]			GPIO_C5 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPC5_IRS = 1,this is IRQ3; if GPC5_IRS =0, this is IRQ11.
0	1	0	Reserved
0	1	1	Input - RET21
1	0	0	Output - General Purpose
1	0	1	Output - GP_TXD
1	1	0	Output - PC Card A22
1	1	1	Output - SCAN21

D3 **GPC4_IRS**

GPIO_C4 IRQ select bit.

Used together with GPC4_MD[2:0] selection of bit function to allow GPIO_C4 to be used as an IRQ source.

If GPC4_MD = 001 and this bit
= 0 then GPIO_C4 is routed to IRQ12. (Default)
= 1 then GPIO_C4 is routed to IRQ4

D[2:0] **GPC4_MD[2:0]**

GPIO_C4 function select. The function mapped to the GPIO_C4 pin is as follows:

GPC4_MD[2:0]			GPIO_C4 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPC4_IRS = 1,this is IRQ4; if GPC4_IRS =0, this is IRQ12.
0	1	0	Input - $\overline{\text{IOCS16}}$
0	1	1	Input - RET20
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - PC Card A21
1	1	1	Output - SCAN20

Name GPIO Group C Mode Register 3

Type Read/Write

Index 5AH

Description This register determines GPIO pin functions.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPC3_IRS	GPC3_MD2	GPC3_MD1	GPC3_MD0	GPC2_IRS	GPC2_MD2	GPC2_MD1	GPC2_MD0

D7 **GPC3_IRS**

GPIO_C3 IRQ select bit.

Used together with GPC3_MD[6:4] selection of bit function to allow GPIO_C3 to be used as an IRQ source.

If GPC3_MD = 001 and this bit
= 0 then GPIO_C3 is routed to IRQ13. (Default)
= 1 then GPIO_C3 is routed to IRQ5

D[6:4] **GPC3_MD[2:0]**

GPIO_C3 function select. The function mapped to the GPIO_C3 pin is as follows:

GPC3_MD[2:0]			GPIO_C3 Pin Function
0	0	0	Input - General Purpose (default)

0	0	1	Input: if GPC3_IRS = 1,this is IRQ5;
			if GPC3_IRS =0, this is IRQ13.

0	1	0	Input - $\overline{\text{MEMCS16}}$
0	1	1	Input - RET19
1	0	0	Output - General Purpose
1	0	1	Output - PC Card A20
1	1	0	Output - Programmable Chip Select 2
1	1	1	Output - SCAN19

D3 **GPC2_IRS**

GPIO_C2 IRQ select bit.

Used together with GPC2_MD[2:0] selection of bit function to allow GPIO_C2 to be used as an IRQ source.

If GPC2_MD = 001 and this bit
= 0 then GPIO_C2 is routed to IRQ14. (Default)
= 1 then GPIO_C2 is routed to IRQ6

D[2:0] **GPC2_MD[2:0]**

GPIO_C2 function select. The function mapped to the GPIO_C2 pin is as follows:

GPC2_MD[2:0]			GPIO_C2 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Input: if GPC2_IRS = 1,this is IRQ6; if GPC2_IRS =0, this is IRQ14.
0	1	0	Input - LB2
0	1	1	Input - RET18
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 1
1	1	1	Output - SCAN18

Name	GPIO Group C Mode Register 4
Type	Read/Write
Index	5BH
Description	This register determines GPIO pin functions.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
GPC1_IRS	GPC1_MD2	GPC1_MD1	GPC1_MD0	GPC0_IRS	GPC0_MD2	GPC0_MD1	GPC0_MD0

D7 **GPC1_IRS**

GPIO_C1 IRQ select bit.

Used together with GPC1_MD[6:4] selection of bit function to allow GPIO_C1 to be used as an IRQ source.

If GPC1_MD = 001 and this bit
= 0 then GPIO_C1 is routed to IRQ15. (Default)
= 1 then GPIO_C1 is routed to IRQ7

D[6:4] **GPC1_MD[2:0]**

GPIO_C1 function select. The function mapped to the GPIO_C1 pin is as follows:

GPC1_MD[2:0]			GPIO_C1 Pin Function
0	0	0	Input - General Purpose (default)

0	0	1	Input: if GPC1_IRS = 1,this is IRQ7;
			if GPC1_IRS =0, this is IRQ15.

0	1	0	Input - GP_RXD
0	1	1	Input - RET17
1	0	0	Output - General Purpose
1	0	1	Reserved
1	1	0	Output - Programmable Chip Select 0
1	1	1	Output - SCAN17

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **GPC0_MD[2:0]**

GPIO_C0 function select. The function mapped to the GPIO_C0 pin is as follows:

GPC0_MD[2:0]			GPIO_C0 Pin Function
0	0	0	Input - General Purpose (default)
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Input - RET16
1	0	0	Output - General Purpose
1	0	1	Output - LCD M
1	1	0	Output - PC Card Address Latch Enable
1	1	1	Output - SCAN16

Name GPIO Group A Data Register

Type Read/Write

Index 5CH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPA_D7	GPA_D6	GPA_D5	GPA_D4	GPA_D3	GPA_D2	GPA_D1	GPA_D0

D[7:0] **GPA_D**

GPIO_A[7:0] data bits.

When a particular GPIO_A[7:0] pin is configured as General Purpose Output, data written to this register is output on the corresponding GPIO_A[7:0] pin. When configured for General Purpose Output, reads to this register will return the last data written.

When a particular GPIO_A[7:0] pin is configured as General Purpose Input, data inputs on the GPIO_A[7:0] pins may be read from this register. When configured for General Purpose input, writes to bits in this register are ignored.

Note: Bits not assigned as general purpose input or output are ignored when written to, and are cleared to ‘0’ when read.

Name GPIO Group B Data Register

Type Read/Write

Index 5DH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPB_D7	GPB_D6	GPB_D5	GPB_D4	GPB_D3	GPB_D2	GPB_D1	GPB_D0

D[7:0] **GPB_D**

GPIO_B[7:0] data bits.

When a particular GPIO_B[7:0] pin is configured as General Purpose Output, data written to this register is output on the corresponding GPIO_B[7:0] pin. When configured for General Purpose Output, reads to this register will return the last data written.

When a particular GPIO_B[7:0] pin is configured as General Purpose Input, data inputs on the GPIO_B[7:0] pins may be read from this register. When configured for General Purpose input, writes to bits in this register are ignored.

Note: Bits not assigned as general purpose input or output are ignored when written to, and are cleared to ‘0’ when read.

Name GPIO Group C Data Register

Type Read/Write

Index 5EH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
GPC_D7	GPC_D6	GPC_D5	GPC_D4	GPC_D3	GPC_D2	GPC_D1	GPC_D0

D[7:0] **GPC_D**

GPIO_C[7:0] data bits.

When a particular GPIO_C[7:0] pin is configured as General Purpose Output, data written to this register is output on the corresponding GPIO_C[7:0] pin. When configured for General Purpose Output, reads to this register will return the last data written.

When a particular GPIO_C[7:0] pin is configured as General Purpose Input, data inputs on the GPIO_C[7:0] pins may be read from this register. When configured for General Purpose input, writes to bits in this register are ignored.

Note: Bits not assigned as general purpose input or output are ignored when written to, and are cleared to ‘0’ when read.

Name	SCAN Control A Register
Type	Read/Write
Index	60H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
SCAN7	SCAN6	SCAN5	SCAN4	SCAN3	SCAN2	SCAN1	SCAN0

D[7:0] **SCAN[7:0]**

SCAN control bits for GPIO pin group A. Default = 0.
When any GPIO_A[7:0] pin is assigned as one of SCAN[7:0], that pin will be controlled by its associated SCAN bit of this register as follows:

0 = GPIO_A pin driven to high-impedance state.
1 = GPIO_A pin driven low.

Name SCAN Control B Register

Type Read/Write

Index 61H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SCAN15	SCAN14	SCAN13	SCAN12	SCAN11	SCAN10	SCAN9	SCAN8

D[7:0] **SCAN[15:8]**

SCAN control bits for GPIO pin group B. Default = 0.
When any GPIO_B[7:0] pin is assigned as one of SCAN[15:8], that pin will be controlled by its associated SCAN bit of this register as follows:

0 = GPIO_B pin driven to high-impedance state.
1 = GPIO_B pin driven low.

Name SCAN Control C Register
Type Read/Write
Index 62H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
SCAN23	SCAN22	SCAN21	SCAN20	SCAN19	SCAN18	SCAN17	SCAN16

D[7:0] **SCAN[23:16]**

SCAN control bits for GPIO pin group C. Default = 0.
When any GPIO_C[7:0] pin is assigned as one of SCAN[24:16], that pin will be controlled by its associated SCAN bit of this register as follows:

0 = GPIO_C pin driven to high-impedance state.
1 = GPIO_C pin driven low.

Name Return Status A Register
Type Read/Write
Index 63H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
RET[7:0]							

D[7:0] **RET[7:0]**

Return status bits 7:0 for GPIO pin group A. Default = FFH.

When any of the GPIO_A[7:0] pins are assigned as RET[7:0], that GPIO pin state will be available on the associated bit in this register. Bits in this register not assigned by the GPIO Group A Mode register as one of RET[7:0] will return ‘1’ when read.

Name	Return Status B Register
Type	Read/Write
Index	64H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
RET[15:8]							

D[7:0] **RET[15:8]**

Return status bits 15:8 for GPIO pin group B. Default = FFH.

When any of the GPIO_B[7:0] pins are assigned as RET[15:8], that GPIO pin state will be available on the associated bit in this register. Bits in this register not assigned by the GPIO Group B Mode register as one of RET[15:8] will return ‘1’ when read.

Name Return Status C Register

Type Read/Write

Index 65H

Description

Bits

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RET[23:16]							

D[7:0] **RET[23:16]**

Return status bits 23:16 for GPIO pin group B. Default = FFH.

When any of the GPIO_C[7:0] pins are assigned as RET[23:16], that GPIO pin state will be available on the associated bit in this register. Bits in this register not assigned by the GPIO Group B Mode register as one of RET[23:16] will return ‘1’ when read.

Name Keyboard Scan Enable Register

Type Read/Write

Index 66H

Description The keyboard controller interface configuration is programmed through this register. Certain other PC functions are also controlled, as described.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SW8	SW7	SW6	SW5	ENASCAN	SCANMD	SCANCLK1	SCANCLK0

D[7:4] **SW[8:5]**

Default = 0000.

These bits represent system switches 8 through 5 in a PC/XT compatible system. The value written to these bits may be read by PC/XT software or OS in the PC/XT compatible PPIC System Status Register. These bits represent the number of disks in the system and the default display mode, and are decoded as follows:

SW8	SW7	Number of Floppy Drives		SW6	SW5	Default Display Mode
0	0	1		0	0	EGA/VGA
0	1	2		0	1	CGA 40 x 25
1	0	3		1	0	CGA 80 x 25
1	1	4		1	1	MDA

These bits are provided for compatibility purposes only. They do not physically control any VG330 hardware. In a PC/XT system, the floppy count determines the logical address of the first hard disk, such as C:, D:, or E:. The default display mode is read by a standard PC/XT BIOS to determine the location and format of the display BIOS

D3 **ENASCAN**

Enable Keyboard Scan.

This bit determines the source driving the PC/XT-compatible PPIA Keyboard Data Register accessed at I/O address 060h and IRQ1. ENASCAN selects the primary keyboard interface and also selects how keyboard scan codes are passed to system software. (See also: Shadow XT Shift Register at Index 68H.)

0 = Selects the PC/XT serial keyboard interface as the primary keyboard interface. (default)
1 = Select scanned keyboard matrix as the primary keyboard interface.

Case ENASCAN=0

When the serial interface is selected, the PPIA Keyboard Data Register is defined as Read Only and keyboard scan codes read from this register are generated by the PC/XT serial keyboard interface shift register. The shift register also generates an IRQ1 when one character has been received to signal the standard keyboard handler that keyboard data is available.

Keyboard scanning can still be performed while the ENASCAN bit is set, but in this case the BIOS must use another mechanism to pass scan codes to the system. An example of such an implementation would be an icon based touch pad where primary keyboard input is handled by the PC/XT serial keyboard interface and the touch pad is handled by the keyboard scanner.

Case ENASCAN=1

When this bit is 1, the VG330 uses a scanned keyboard matrix as the primary keyboard interface.

In this mode the PPIA Keyboard Data Register is defined as Read/Write. The BIOS scanned keyboard handler translates the keyboard matrix data into an PC/XT compatible scan code and writes this value to the PPIA Keyboard Data Register. IRQ1 is generated during this write to the PPIA Keyboard Data Register to signal the standard keyboard handler that keyboard data is available.

Just as keyboard scanning is permitted while the PC/XT serial keyboard interface is defined as the primary keyboard interface, so does the serial keyboard interface remain enabled when keyboard scanning is selected as the primary interface. However, access to data received through the serial keyboard interface shift register is handled differently for this case. Under this mode of operation, data transmitted through the PC/XT serial keyboard interface may be read in the Shadow XT Shift Register at VG330 index 068H. In this mode, the serial keyboard interface cannot generate an interrupt when a character has been received, so the interface must be polled.

D2 **SCANMD**

Keyboard Scan Mode Select.

This bit selects the type of keyboard matrix scanning:

0 = Enables a full scan interface to the keyboard matrix and keydown events are sampled on the RETURN signal lines. (default)
1 = Enables a partial scan interface to the keyboard matrix and keydown events are sampled on the SCAN signal lines.

D[1:0] **SCANCLK[1:0]**

Keyboard Scanner NMI Rate.

Bits D[1:0], SCANCLK[1:0], are used to select a periodic NMI rate as shown in the following table. These bits have effect only when Bit D2 of the Scan NMI Control and Status Register (Index 67H) is set as follows:

SCANCLK1	SCANCLK0	NMI Rate in Hz
0	0	51
0	1	64
1	0	85
1	1	128

Typically, this NMI is used to perform keyboard scanning once a key-down event has been detected. However, the NMI generated from this logic is independent of the keyboard scan mode and therefore could be used as a simple periodic NMI. Enabling and status reporting of the periodic NMI are controlled in the Scan NMI Control and Status Register at Index 67H.

Name Scan NMI Control and Status Register

Type Read/Write

Index 67H

Description NMI sources are enabled or disabled and NMI status is reported through this register.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
KEY_NMI	SCAN_NMI	PPIB_NMI	Reserved	KYNMI_EN	SNMI_EN	PNMI_EN	Reserved

D7 **KEY_NMI**

This is a status bit that is set high while the Keydown NMI is active.

This bit is set to 1 under these conditions:

If bit D3 of this register is set to 1 and an NMI is generated due to a high to low transition being detected on any of the RET[23:0] signals (through GPIO pins) from a keyboard matrix, or

if a low to high transition is detected on any SCAN[23:0] line (through GPIO pins).

To clear both the Keydown NMI and the KEY_NMI status bit, perform an I/O write to this register with bit D7 set high.

D6 **SCAN_NMI**

This status bit is set high while the periodic scan NMI is active.

To clear both the periodic scan NMI and the SCAN_NMI status bit, perform an I/O write to this register with bit D6 set high.

D5 **PPIB_NMI**

This status bit is set high while the PPBI NMI is active.

To clear both the PPBI NMI and the PPIB_NMI status bit, perform an I/O write to this register with bit D5 set high.

D4 **Reserved**

D3 **KYNMI_EN**

This bit enables the Keydown NMI, KEY_NMI, bit D7 of this register. Default = 0.

0 = Disable Keydown NMIs.
1 = Enable Keydown NMIs.

When Keydown NMIs are enabled, the NMI source, SCAN = 1 or RETURN = 0, is determined by the SCANMD bit of the Keyboard Scan Enable Register.

Both SCAN and RETURN are defined as levels, not transitions, for the purposes of Keydown NMI generation. Therefore, while a keydown condition exists, NMI will be asserted if KYNMI_EN is set high. An attempt to clear a Keydown NMI by writing to this register with bit D7 set high will have no effect on either the Keydown NMI or the KEY_NMI status bit if the keydown condition exists during this write.

Once a Keydown NMI has been generated, the recommended way of clearing the NMI is to first disable further NMIs by resetting the KYNMI_EN bit low and then clear the NMI by writing the KEY_NMI bit high.

D2 **SNMI_EN**

This bit enables the periodic scan NMI typically used to scan the external keyboard matrix. Default = 0.

0 = Disable periodic scan NMIs.
1 = Enable periodic scan NMIs. The periodic scan NMI rate is determined by the SCLK[1:0] bits of the Keyboard Scan Enable Register.

Periodic scan NMIs are essentially asynchronous events which could result in the immediate generation of an NMI when enabled. To prevent this behavior, software should first write the SCAN_NMI bit high before setting the SNMI_EN bit high.

D1 **PNMI_EN**

This bit enables the PPIB I/O write NMI. Default = 0.

0 = Disable generating an NMI in response to a write to PPIB I/O.
1 = Enable generating an NMI upon an I/O write to PC/XT compatible PPIB Keyboard Control Register that causes bit D6 of that register to change from low to high.

In a PC/XT system, bit D6 of the PPIB is defined as KCLKEN. When this bit is reset low, the keyboard clock line is driven low by the keyboard interface logic causing a reset to the keyboard microcontroller. When bit D6 is then set back high, the keyboard microcontroller exits reset and performs its power-up diagnostics, such as stuck key testing, and sends a diagnostics result code the keyboard interface logic.

Since in keyboard scan mode an external microcontroller is not used, the VG330 performs NMI I/O trapping during writes to the PPIB register. When a PPIB NMI is generated, the BIOS keyboard scan handler writes the appropriate result code to the PPIA Keyboard Data Register.

D0 **Reserved**

Name Shadow XT Shift Register

Type Read/Write

Index 68H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
KBVALUE[7:0]							

D[7:0] **KBVALUE[7:0]**

Keyboard data shifted in over the serial keyboard interface can be read in different ways depending on whether serial keyboard interface is enabled and upon the setting of the ENASCAN bit of the Keyboard Scan Enable Register at Index 66H.

The table below shows the operating configuration for this register that results from the setting of ENASCAN:

Value of ENASCAN	Resulting Configuration Supported	
	I/O port 60H	**KBVALUE**
0	A read of Port 60H returns the value shifted into the VG330 on the GPIO pins configured for KBCLK and KBDATA.	KBVALUE contains the last value written to Port 60H.
1	A read of Port 60H returns the last value written to I/O port 60H.	KBVALUE contains the value shifted into the VG330 on the GPIO pins configured for KBCLK and KBDATA.

Name RTC Seconds Register
Type Read/Write
Index 70H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0

D[7:6] **Reserved**

Reserved bits.

D[5:0] **SEC[5:0]**

Binary value representing the seconds count. Default = 000000.
Valid settings are from 00H to 3BH.

Name RTC Minutes Register
Type Read/Write
Index 71H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0

D[7:6] **Reserved**

Reserved bits. Default = 0.

D[5:0] **MIN[5:0]**

Binary value representing the minutes count. Default = 000000.
Valid settings are from 00H to 3BH.

Name RTC Hours Register
Type Read/Write
Index 72H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	HR4	HR3	HR2	HR1	HR0

D[7:5] **Reserved**

Reserved bits. Default = 0.

D[4:0] **HR[4:0]**

Binary value representing the hours count, in 24 hour mode.
Default = 00000.
Valid settings are from 00H to 17H.

Name RTC Day Low Register
Type Read/Write
Index 73H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
DAY[7:0]							

D[7:0] **DAY[7:0]**

Binary value representing the low day count. Default = 00H.
Valid settings are from 00H to FFH.

Name RTC Day High Register
Type Read/Write
Index 74H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	DAY11	DAY10	DAY9	DAY8

D[7:4] **Reserved**

Reserved bits. Default = 0H

D[3:0] **DAY[11:8]**

Binary value representing the high day count. Default = 0H.
Valid settings are from 00H to 0FH.

Name RTC Alarm Seconds Register
Type Read/Write
Index 75H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	ALRS5	ALRS4	ALRS3	ALRS2	ALRS1	ALRS0

D[7:6] **Reserved**

Reserved bits. Default = 00.

D[5:0] **ALRS[5:0]**

Binary value representing the Alarm seconds count. Default = 000000.
Valid settings are from 00H to 3BH.

Name RTC Alarm Minutes Register
Type Read/Write
Index 76H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	ALRM5	ALRM4	ALRM3	ALRM2	ALRM1	ALRM0

D[7:6] **Reserved**

Reserved bits. Default = 00.

D[5:0] **ALRM[5:0]**

Binary value representing the Alarm minutes count. Default = 0000000. Valid settings are from 00H to 3BH.

Name RTC Alarm Hours Register
Type Read/Write
Index 77H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ALRH4	ALRH3	ALRH2	ALRH1	ALRH0

D[7:5] **Reserved**

Reserved bits. Default = 0.

D[4:0] **ALRH[4:0]**

Binary value representing the Alarm hours count in 24 hour mode. Default = 00000. Valid settings are from 00H to 17H.

Name RTC Alarm Day Register
Type Read/Write
Index 78H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ALRD4	ALRD3	ALRD2	ALRD1	ALRD0

D[7:5] **Reserved**

Reserved bits. Default = 0.

D[4:0] **ALRD[4:0]**

Binary value representing the Alarm day count. Default = 00000. Valid settings are from 00H to 1FH. This value is compared with the least significant 5 bits of the RTC Low Day counter.

Name	RTC Mode Register
Type	Read/Write
Index	79H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$\overline{\text{RTCEN}}$	Reserved	UPDATE	Reserved	ALRMD	Reserved	$\overline{\text{MSK\_ALRM}}$	$\overline{\text{MSK\_PER}}$

D7 **$\overline{\textbf{RTCEN}}$**

RTC clock enable bit. Default = 0.

When the RTC clock is disabled, only the RTC mode and RTC status registers will be accessible.

0 = Enable RTC Clock
1 = Disable RTC Clock

D6 **Reserved**

Reserved bit. Default = 0.

D5 **UPDATE**

RTC update enable bit. Default = 0.

Use this bit to pause the RTC clock to set time or alarm values.

0 = No pause (normal operation)
1 = Pause the RTC clock to set time or alarm values.

D4 **Reserved**

Reserved bit. Default = 0.

D3 **ALRMD**

RTC alarm mode bit. Default = 0.

This bit determines the alarm mode.

0 = ALMD[4:0] disabled for alarm comparison (alarm occurs daily)
1 = ALMD[4:0] enabled for alarm comparison (alarm occurs once every 32 days)

D2 **Reserved**

Reserved bit. Default = 0.

D1 **$\overline{\textbf{MSK\_ALRM}}$**

RTC alarm interrupt mask bit. Default = 0.

Used to enable or disable the RTC alarm.

0 = RTC Alarm interrupts masked.
1 = RTC Alarm interrupts unmasked.

D0 **$\overline{\text{MSK\_PER}}$**

RTC periodic interrupt mask bit. Default = 0.

0 = RTC periodic interrupts masked.
1 = RTC periodic interrupts unmasked. An interrupt will be generated once per second.

Name RTC Status Register
Type Read/Write
Index 7AH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
VALID	Reserved	Reserved	Reserved	Reserved	Reserved	ALARM	PERIODIC

D7 **VALID**

RTC valid status bit. Default = 0.

Following a hard reset of the VG330, this bit is cleared to zero. System software sets this bit to 1 after the RTC has been initialized.

0 = RTC Clock data invalid.
1 = Disable RTC Clock data valid.

D[6:2] **Reserved**

Reserved bits. Default = 00000.

D1 **ALARM**

RTC alarm status bit. Default = 0.

0 = No RTC alarm pending.
1 = This bit is set to ‘1’ when an RTC alarm is pending. This bit is unaffected by the RTC alarm interrupt mask bit and may be cleared by writing to this register with bit D1 set high.

D0 **PERIODIC**

RTC periodic status bit. Default = 0.

This bit is set to ‘1’ once per second. This bit is unaffected by the RTC periodic interrupt mask bit and may be cleared by writing to this register with bit D0 set high.

Name	ROM Wait State Control Register
Type	Read/Write
Index	7CH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	ROM1_W2	ROM1_W1	ROM1_W0	Reserved	ROM0_W2	ROM0_W1	ROM0_W0

D7 **Reserved**

D[6:4] **ROM1_W**

ROM 1 Wait State bits. Default = 111.

These bits specify the CPU wait states added to ROM 1 memory cycles and are expressed in processor clock (CPUCLK) cycles. ROM 1 wait states may be programmed to select from zero to 7 additional processor clock cycles.

Value in ROM1_W[2:0]	**Number of ROM cycle wait states in terms of CPUCLKs (depends on value of bit D7 as follows:)** Value of Bit D7 of RAM Wait State Register (Index 7DH)	
	FASTMEM=0	**FASTMEM=1**
000	5	3[a]
001	6	4
010	7	5
011	8	6
100	9	7
101	10	8
110	11	9
111	12	10

[a] Do not use this setting for DRAM

D3 **Reserved**

Reserved bit. Default = 0.

D[2:0] **ROM0_W**

ROM 0 Wait State bits. Default = 111B.

These bits specify the CPU wait states added to ROM 0 memory cycles and are expressed in processor clock (CPUCLK) cycles. ROM 0 wait states may be programmed to select from zero to 7 additional processor clock cycles in the same way as ROM1_W above, and are affected by D7 in register 7DH in the same way.

Name	RAM Wait State Control Register
Type	Read/Write
Index	7DH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
FASTMEM	RAM_W2	RAM_W1	RAM_W1	Reserved	Reserved	Reserved	LODLY

D[7] **FASTMEM**

Changes minimum RAM or ROM cycle time from 5 CPU clocks to 3 CPU clocks.See table below.

D[6:4] **RAM_W**

RAM Wait State bits. Default = 111.

These bits specify the CPU wait states added to RAM memory cycles and are expressed in processor clock (CPUCLK) cycles. RAM wait states may be programmed to select from zero to 7 additional processor clock cycles.The following table shows the numbers of wait states inserted; the value used depends on the setting of bit D7 of the RAM Wait Register at the index 7DH

Value in RAM_W[2:0]	**Number of RAM cycle wait states in terms of CPUCLKs (depends on value of bit D7 as follows:)** Value of Bit D7 of RAM Wait State Register (Index 7DH)	
	D7=0	**D7=1**
000	5	3[a]
001	6	4
010	7	5
011	8	6
100	9	7
101	10	8
110	11	9
111	12	10

[a] Do not use this setting for DRAM

D[3:1] **Reserved**

Reserved bit. Default = 0.

D0 **LODLY**

Lead off delay enable bit. Default = 1.

0 = Cycles not delayed.
1 = When this bit is set to ‘1’, the start of all cycles will be delayed by one clock cycle to provide additional address setup time.

Name	Refresh Timer Register
Type	Read/Write
Index	7EH
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
REFRT7	REFRT6	REFRT5	REFRT4	REFRT3	REFRT2	REFRT1	REFRT0

D[7:0] **REFRT**

Refresh Rate bits. Default = 0.

These bits determine the RAM refresh rate and specify the divisor applied to the 32.768 Khz clock for generating refresh requests. Setting this count to 00H will cause a refresh cycle to be generated on each edge of the 32.768 Khz clock, yielding a 15.26 µS refresh rate.

REFRT[7:0]	**Refresh Rate**	**# of 32.768 KHz clock edges**
00H	15.258 µS	1
01H	3.875 mS	254
02H	3.860 mS	253
03H	3.845 mS	252
. . .	. . .	. . .
. . .	. . .	. . .
. . .	. . .	. . .
FCH	45.776 mS	3
FDH	30.517 mS	2
FEH	15.258 mS	1
FFH	3.906 mS	256

Name Refresh Control Register
Type Read/Write
Index 7FH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
REFEN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

D7 **REFEN**

Refresh Enable. Default = 0.

0 = Disable refresh.
1 = Enable refresh.

D[6:0] **Reserved**

Reserved bits. Default = 0.

Name PMU Status Register

Type Read/Write

Index C0H

Description This register is used to determine the current state of the PMU, and it identifies the cause of a RESUME sequence. It is also used to command the PMU to enter specific operating modes.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	WU1	WU0	ACTIVITY	LB2STAT	LB1STAT	STATE1	STATE0

D7 **Reserved**

D[6:5] **WU**

Read-only Wakeup code bits. These bits identify the cause of a RESUME from SUSPEND or OFF modes.

WU1	WU0	Wakeup Cause
0	0	None (Default)
0	1	EXT input. Note: EXT is highest priority, RI lowest.
1	0	RTC Alarm.
1	1	RI input.

D4 **ACTIVITY**

Activity status bit. Default = 0. This bit is cleared to zero when a zero is written to this bit.
1 = An unmasked activity trigger has occurred.

D3 **LB2STAT**

LB2 signal status. Default = 0.

This bit reflects the state of the Secondary Low Battery input signal. To implement Secondary Low Battery reporting in a system, one of the GPIO pins must be configured to provide LB2, as described in Chapter 12, *GPIO*.

D2 **LB1STAT**

LB1 pin status. This bit reflects the state of the Primary Low Battery input pin.

D[1:0] **STATE[1:0]**

Power management state bits. Default = 0.

These bits reflect the current power management state of the VG330. Software may immediately transition to any power management state by writing to these bits. To enter OFF Mode, write the value 0FFH to this register.

STATE1	STATE0	Power Management State
0	0	ON Mode
0	1	DOZE Mode
1	0	SLEEP Mode
1	1	VG330 is in SUSPEND or RESUME state.

Name PMU Control Register

Type Read/Write

Index C2H

Description This register provides the following functions:
1) It controls the effect SmartClock has on the system clock
2) It defines the number of RI pulses that can trigger a RESUME
3) It enables Low Battery input debouncing

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	RING2	RING1	RING0	Reserved	LBDBNC	DOZ_SPD	FSTCLKO

D7 **Reserved**

Always write to 0.

D[6:4] **RING**

RI count. Default = 001

These bits specify the number of RI input pulses required to RESUME the VG330 from SUSPEND or OFF modes.

RING2	RING1	RING0	RI pulses required to RESUME
0	0	0	RI input can not force RESUME
0	0	1	1 (Default)
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

D3 **Reserved**

Always write to 0.

D2 **LBDBNC**

Low Battery debounce enable bit. Default = 0.

0 = When this bit is cleared to ‘0’ the LB1/LB2 inputs are defined as edge triggered and an NMI may be generated immediately after LB1/LB2 are asserted.
1 = When this bit is set to ‘1’ the LB1 input, and LB2 input if LB2 is enabled, will be debounced at approximately 1 ms. In this mode, the LB1 and/or LB2 pin must remain active for 1 ms before an LB1/LB2 NMI will be generated.

D1 **DOZ_SPD**

DOZE/SLEEP clock divisor select. Default = 0.

This bit selects the divisor applied to the processor clock during DOZE and SLEEP modes. This bit is ignored if DOZE/SLEEP stop clock mode is enabled or if bit D0, the FSTCLKO bit, is set to ‘1’.

0 = Divide by 4
1 = Divide by 8

D0 **FSTCLKO**

Fast clock enable bit. Default = 0.

0 = Allow use of the slow clock divisors or stop clock enable bits of the Clock Control Register.
1 = When this bit is set to ‘1’, the slow clock divisors or stop clock enable bits of the Clock Control Register are ignored. The processor clock will remain operating at full speed during DOZE and SLEEP modes.

Name PMU Activity Mask Register

Type Read/Write

Index C3H

Description This register determines which activities will cause a transition from DOZE or from SLEEP mode, to ON mode.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MSK_IORNG	MSK_VIDM	MSK_HD	Reserved	MSK_SIO	MSK_EXCA	MSK_KBD	MSK_GPIO

D7 **MSK_IORNG**

Programmable I/O range activity mask bit. Default = 1.

0 = Enables triggering of activity detector by I/O accesses within the address range specified by the PMU I/O Range Register.
1 = I/O accesses within the address range specified by the PMU I/O Range Register do not trigger activity detection.

D6 **MSK_VIDM**

Video memory activity mask bit. Default = 0.

0 = Enables triggering of activity detector by memory writes to the VG330 display buffer area mapped at B8000H - BFFFFH or A0000H - AFFFFH.
1 = Memory writes to the VG330 display buffer area mapped at B8000H - BFFFFH or A0000H - AFFFFH do not trigger activity detection.

D5 **MSK_HD**

Hard disk activity mask bit. Default = 0.

0 = Enables triggering of activity detector by I/O accesses to a hard disk at addresses 1F0H-1F7H and 3F6H-3F7H.
1 = I/O accesses to a hard disk at addresses 1F0H-1F7H and 3F6H-3F7H do not trigger activity detection.

D4 **Reserved**

Reserved bit. Default = 0.

D3 **MSK_SIO**

Serial port activity mask bit. Default = 0.

0 = Enables triggering of activity detector by I/O accesses to the serial port at addresses 2E8H - 2EFH, 2F8H - 2FFH, or 3F8H - 3FFH.
1 = I/O accesses to the serial port at addresses 2E8H - 2EFH, 2F8H - 2FFH, or 3F8H - 3FFH do not trigger activity detection.

D2 **MSK_EXCA**

ExCA activity mask bit. Default = 0.

0 = Enables triggering of activity detector by I/O accesses to the registers of the internal ExCA controller or I/O or memory accesses to PC CARD cards.
1 = I/O accesses to the registers of the internal ExCA controller or I/O or memory accesses to PC CARD cards do not trigger activity detection.

D1 **MSK_KBD**

Keyboard activity mask bit. Default = 0.

0 = Enables triggering of activity detector by I/O accesses to the keyboard controller at address 060H.
1 = I/O accesses to the keyboard controller at address 060H do not trigger activity detection.

D0 **MSK_GPIO**

GPIO PCS Activity Mask Bit. Default = 0.

0 = Enables triggering of activity detector by activity on a programmable chip select that was defined in the GPIO Registers.
1 = Activity of a programmable chip select does not trigger activity detection.

Name PMU NMI Mask Register

Type Read/Write

Index C4H

Description The bits of this register control masking for sources of NMI requests.

Note 1: The Global PMU NMI mask bit and the EXT input NMI mask bit do not affect RESUME operation triggered by the EXT input.

Note 2: Pending NMI requests do not take effect unless they are unmasked. Masked sources never generate NMI's.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MSK_PNMI	Reserved	MSK_SUSP	MSK_SLP	MSK_LB2	MSK_LB1	MSK_EXT	Reserved

D7 **MSK_PNMI**

Global PMU NMI mask bit. Default =1.

This bit blocks the PMU NMI request. It does not prevent PMU NMI status bits (using the register at Index DCH) from being set. When this bit is cleared, if any PMU NMI status bits are already set, a PMU NMI will occur.

0 = Allow PMU_NMI to occur
1 = Mask PMU_NMI from occurring.

Note that this bit will neither clear pending PMU NMI sources nor prevent incoming requests from setting status bits in the register at Index DCH.

If an NMI request from any of the sources handled by the other bits in this register is pending when this bit is set to '1', or occurs after this bit is set to '1', and the source's NMI request is not cleared, then an NMI will be generated as soon as this bit is cleared to '0'.

D6 **Reserved**

Reserved bit. Default = 0.

D5 **MSK_SUSP**

SUSPEND time-out NMI mask bit. Default = 1.

The PMU never enters SUSPEND mode automatically. It can only enter SUSPEND through a command written to the register at Index C0H.

0 = Enables generating an NMI when the SUSPEND timer expires.
1 = NMI will not be generated when the SUSPEND timer expires. The PMU will not automatically enter SUSPEND mode when the SUSPEND timer expires and the SUSPEND time-out NMI is masked.

D4 **MSK_SLP**

SLEEP Time-out / SLEEP Activity NMI mask bit. Default = 1.

0 = Enables generating an NMI when the SLEEP timer expires or when activity is detected while the PMU is in SLEEP mode. When this bit is cleared to ‘0’, the PMU will not automatically transition from DOZE to SLEEP when the SLEEP timer expires. Instead, the PMU will generate an NMI and remain in the DOZE mode. Once the PMU is commanded into SLEEP mode, it will not automatically transition back to ON mode when unmasked activity is detected. Instead an NMI will be generated and the PMU will remain in SLEEP

1 = NMI will not be generated when the SLEEP timer expires or when activity is detected while the PMU is in SLEEP mode. Instead, the PMU will automatically transition from DOZE mode to SLEEP mode after the SLEEP timer expires and automatically return to ON mode when activity is detected within SLEEP mode.

D3 **MSK_LB2**

LB2 input NMI mask bit. Default = 1.

Note that use of LB2 requires the system designer to configure a GPIO pin allocated as an input to convey an LB2 signal into the VG330.

0 = Enables generating an NMI if the LB2 input goes active.
1 = Activity on the LB2 input will not generate an NMI.

D2 **MSK_LB1**

LB1 input NMI mask bit. Default = 1.

0 = Enables generating an NMI if the LB1 input pin goes active.
1 = Activity on the LB1 input pin will not generate an NMI.

D1 **MSK_EXT**

EXT input NMI mask bit. Default = 1.

0 = Enables generating an NMI if the EXT input pin goes active.
1 = Activity on the EXT input pin will not generate an NMI.

D0 **Reserved**

Reserved bit. Default = 0.

Name	PMU I/O Range Register
Type	Read/Write
Index	C5H
Description	This register sets the I/O address range used for monitoring I/O activity.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
RNGSIZE	IORNG6	IORNG5	IORNG4	IORNG3	IORNG2	IORNG1	IORNG0

D7 **RNGSIZE**

I/O range size. Sets size of the monitored range. Default = 0.

0 = 16 byte I/O range
1 = 8 byte I/O range

D[6:0] **IORNG[6:0]**

I/O range start. Sets the start address value for monitored I/O activities. Default = 0.

Bits D[6:0] correspond to the SA[9:3] bus address. (The SA bus is shown as *VG330 Internal System Address* in Figure 6-1 in *Bus Architecture* in Chapter 6.) The activity monitor compares D[6:0] to SA[9:3] and uses the result to trigger detection. Bit D0 is ignored when the range size is 16 bytes.

The following table illustrates register usage:

Value in reg	**RNG SIZE**	**IORNG value D[6:0], shown mapped to SA[9:3]**												**Effective range**
	D7	**-**		**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**-**			
	-	SA11	SA10	**SA9**	**SA8**	**SA7**	**SA6**	**SA5**	**SA4**	**SA3**	SA2	SA1	SA0	
00H	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**x**	x	x	x	0000H - 000FH
80H	1	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	x	x	x	0000H - 0007H
55H	0	0	0	**1**	**0**	**1**	**0**	**1**	**0**	**x**	x	x	x	02A0H - 02AFH
D5H	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	x	x	x	02A8H - 02AFH
D4H	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	**0**	x	x	x	02A0H - 02A7H
7FH	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**x**	x	x	x	03F0H - 03FFH
FFH	1	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	x	x	x	03F8H - 03FFH
FEH	1	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**0**	x	x	x	03F0H - 03F7H

Name PMU Power ON Register

Type Read/Write

Index C6H

Description The bits of this register determine the value of the corresponding output pins when the ON state is entered. Default value = 84H.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RAM_ON	Reserved	Reserved	Reserved	Reserved	SYS_ON	Reserved	LCD_ON

D7 **RAM_ON**

VPRAM pin state = RAM_ON value when the ON state is entered.
0 = OFF
1 = ON (Default)

D2 **SYS_ON**

VPSYS pin state = SYS_ON value when the ON state is entered.
0 = OFF
1 = ON (Default)

D0 **LCD_ON**

VPLCD pin state = LCD_ON value when the ON state is entered.
0 = OFF (Default)
1 = ON

Name PMU Power DOZE Register
Type Read/Write
Index C7H
Description The bits of this register determine the value of the corresponding output pins when the DOZE state is entered. Default value = 84H.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
RAM_DOZE	Reserved	Reserved	Reserved	Reserved	SYS_DOZE	Reserved	LCD_DOZE

D7 **RAM_DOZE**

VPRAM pin state = RAM_DOZE value when the DOZE state is entered.
0 = OFF
1 = ON (Default)

D2 **SYS_DOZE**

VPSYS pin state = SYS_DOZE value when the DOZE state is entered.
0 = OFF
1 = ON (Default)

D0 **LCD_DOZE**

VPLCD pin state = LCD_DOZE value when the DOZE state is entered.
0 = OFF (Default)
1 = ON

Name PMU Power SLEEP Register

Type Read/Write

Index C8H

Description The bits of this register determine the value of the corresponding output pins when the SLEEP state is entered. Default value = 84H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RAM_SLP	Reserved	Reserved	Reserved	Reserved	SYS_SLP	Reserved	LCD_SLP

D7 **RAM_SLP**

VPRAM pin state = RAM_SLP value when the SLEEP state is entered.
0 = OFF
1 = ON (Default)

D2 **SYS_SLP**

VPSYS pin state = SYS_SLP value when the SLEEP state is entered.
0 = OFF
1 = ON (Default)

D0 **LCD_SLP**

VPLCD pin state = LCD_SLP value when the SLEEP state is entered.
0 = OFF (Default)
1= ON

Name PMU Power SUSPEND Register

Type Read/Write

Index C9H

Description The bits of this register determine the value of the corresponding output pins when the SUSPEND state is entered. Default value = 80H

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RAM_SUS	Reserved	Reserved	Reserved	Reserved	SYS_SUS	Reserved	LCD_SUS

D7 **RAM_SUS**

VPRAM pin state = RAM_SUS value when the SUSPEND state is entered.
(Default = 1, or ON.)

D2 **SYS_SUS**

VPSYS pin state = SYS_SUS value when the SUSPEND state is entered.
(Default = 0, or OFF.)

D0 **LCD_SUSP**

VPLCD pin state = LCD_SUS value when the SUSPEND state is entered.
(Default = 0, or OFF.)

Name PMU Polarity Register

Type Read/Write

Index CAH

Description The bits of this register determine the polarity of corresponding LCD output pins.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BIAS_POL	LCD_POL

D[7:2] **Reserved**

Reserved bits. Default = 0.

D1 **BIAS_POL**

0 = Active low
1 = Active high

D0 **LCD_POL**

0 = Active low
1 = Active high

Name PMU Output Register

Type Read/Write

Index CBH

Description The bits of this register show the state of the corresponding output pins.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RAM_OUT	Reserved	Reserved	Reserved	Reserved	SYS_OUT	Reserved	LCD_OUT

D7 **RAM_OUT**

RAM_OUT value = VPRAM pin state

D2 **SYS_OUT**

SYS_OUT value = VPSYS pin state

D0 **LCD_OUT**

LCD_OUT value = VPLCD pin state

0 = LCD _OFF

1 = LCD_ON

NOTE: LCD_OUT may be delayed from actual LCD state when LCD power state is changing.

Name PMU DOZE Timer Register

Type Read/Write

Index CCH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	DOZTM3	DOZTM2	DOZTM1	DOZTM0

D[7:4] **Reserved**

Reserved bits. Default = 0.

D[3:0] **DOZTM**

DOZE timer value.

Value	Time
0000	Disabled
0001	1/8 sec.
0010	1/4 sec.
0011	3/8 sec.
0100	1/2 sec.
0101	5/8 sec.
0110	3/4 sec.
0111	7/8 sec.
1000	1 sec.
1001	2 sec.
1010	4 sec.
1011	6 sec.
1100	8 sec.
1101	10 sec.
1110	12 sec.
1111	14 sec.

Name PMU SLEEP Timer Register
Type Read/Write
Index CDH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SLPTM3	SLPTM2	SLPTM1	SLPTM0

D[7:4] **Reserved**

Reserved bits. Default = 0.

D[3:0] **SLPTM**

SLEEP timer value.

Value	Time
0000	Disabled (Default)
0001	1 min
0010	2 min
0011	3 min
0100	4 min
0101	5 min
0110	6 min
0111	7 min
1000	8 min
1001	9 min
1010	10 min
1011	11 min
1100	12 min
1101	13 min
1110	14 min
1111	15 min

Name PMU SUSPEND Timer Register

Type Read/Write

Index CEH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	SUSTM3	SUSTM2	SUSTM1	SUSTM0

D[7:4] **Reserved**

Reserved bits. Default = 0.

D[3:0] **SUSTM**

SUSPEND timer value.

Value	Time
0000	Disabled
0001	1 min
0010	2 min
0011	3 min
0100	4 min
0101	5 min
0110	6 min
0111	7 min
1000	8 min
1001	9 min
1010	10 min
1011	11 min
1100	12 min
1101	13 min
1110	14 min
1111	15 min

Name PMU Activity Status Register
Type Read/Write
Index DBH
Description Shows device activity since inserted. Note that status is shown even if activity is masked off.
Bits

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IORNGACT	VIDACT	HDACT	Reserved	SIOACT	PCCACT	KBDACT	GPIOACT

D7 **IORNGACT**

Programmable I/O range activity status flag. Default = 0.

This bit is set to ‘1’ when programmable I/O range activity is detected. It is cleared to zero after this register is read.

D6 **VIDACT**

Video activity status flag. Default = 0.

This bit is set to ‘1’ when video activity is detected. It is cleared to zero after this register is read.

D5 **HDACT**

Hard disk activity status flag. Default = 0.

This bit is set to ‘1’ when hard disk activity is detected. It is cleared to zero after this register is read.

D4 **Reserved**

Reserved bit. Default = 0.

D3 **SIOACT**

Serial port activity status flag. Default = 0.

This bit is set to ‘1’ when serial port activity is detected. It is cleared to zero after this register is read.

D2 **PCCACT**

PC Card activity status flag. Default = 0.

This bit is set to ‘1’ when I/O accesses to the registers of the internal PC Card controller or I/O or memory accesses to PC CARD cards is detected. It is cleared to ‘0’ after this register is read.

D1 **KBDACT**

Keyboard activity status flag. Default = 0.

This bit is set to ‘1’ when keyboard activity is detected. It is cleared to zero after this register is read.

D0 **GPIOACT**

Status flag for activity in a GPIO programmable chip select. Default = 0.This bit is set to ‘1’ when activity is detected on one of the GPIO’s programmable chip selects. It is cleared to zero after this register is read.

Name PMU NMI Status Register

Type Read/Write

Index DCH

Description Individual NMI Status Register bits are cleared by writing a ‘1’ to that bit position. The NMI signal to the CPU will remain active while the global PMU NMI mask bit (Index C4H, bit D7) is cleared to ‘0’ and any one of these NMI sources are active.

When the mask bits in the PMU NMI Mask register are set, the corresponding inputs will not generate an NMI.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	SLPACT_NMI	SUSTO_NMI	SLPTO_NMI	LB2_NMI	LB1_NMI	EXT_NMI	Reserved

D7 **Reserved**

Reserved bit. Default = 0.

D6 **SLPACT_NMI**

Sleep Activity NMI pending. Default = 0.

This bit is set to ‘1’ when a SLEEP Activity NMI has been generated.

D5 **SUSTO_NMI**

Suspend Time-out NMI pending. Default = 0.

This bit is set to ‘1’ when a SUSPEND time-out NMI has been generated.

D4 **SLPTO_NMI**

Sleep Time-out NMI pending. Default = 0.

This bit is set to ‘1’ when a SLEEP time-out NMI has been generated.

D3 **LB2_NMI**

LB2 NMI pending.Default = 0.

This bit is set to ‘1’ when an LB2 NMI has been generated.

D2 **LB1_NMI**

LB1 NMI pending. Default = 0

This bit is set to ‘1’ when an LB1 NMI has been generated.

D1 **EXT_NMI**

EXT NMI pending. Default = 0.

This bit is set to ‘1’ when an EXT NMI has been generated.

D0 **Reserved**

Reserved bit. Default = 0.

Name PMU RESUME Control Register

Type Read/Write

Index DDH

Description **Note:** If the LB2 option in GPIO is configured for use on a pin, then the LB signal here is redefined as LB2 and any GPIO input assigned to LB2 will become an NMI to the PMU.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RSMDLY1	RSMDLY0	LB_SIGEN	PWG_SIGEN	LB_INH	LB_ABORT	PWG_ABORT	Reserved

D[7:6] **RSMDLY**

RESUME delay from SYSPWRGD. Default = 11.

These bits specify the delay from SYSPWRGD active until the system restarts following a RESUME from SUSPEND or OFF modes.

RSM DLY1	RSM DLY0	RESUME delay from SYSPWRGD active
0	0	None, system RESUMES immediately after SYSPWRGD active
0	1	62.5 ms
1	0	125 ms
1	1	250 ms (Default)

D5 **LB_SIGEN**

Low battery signal enable. Default = 0.

0 = The VG330 will not signal the system when a RESUME request is ignored due to a low battery condition signaled by one speaker beep.
1 = The VG330 will signal the system when a RESUME request is ignored due to a low battery condition.

D4 **PWG_SIGEN**

SYSPWRGD time-out signal enable. Default = 0.

0 = The VG330 will not signal the system when a RESUME request is aborted due to a low battery condition prior to SYSPWRGD, or a SYSPWRGD time-out signaled by two speaker beeps.
1 = The VG330 will signal the system when a RESUME request is aborted due to a low battery condition prior to SYSPWRGD, or a SYSPWRGD time-out.

D3 **LB_INH**

Low battery RESUME inhibit. Default = 0.

0 = The VG330 will accept all requests to RESUME the system while the LB pin is active.
1 = The VG330 will ignore all requests to RESUME the system while the LB pin is active.

D2 **LB_ABORT**

Low battery RESUME abort. Default = 0.

0 = System will ignore LB_ABORT signal.
1 = The VG330 will abort a RESUME sequence and re-enter SUSPEND or OFF mode if the LB1 pin goes active prior to SYSPWRGD.

D1 **PWG_ABORT**

SYSPWRGD RESUME abort. Default = 0.

0 = System will ignore PWG_ABORT signal.
1 = The VG330 will abort the RESUME sequence and re-enter SUSPEND or OFF mode if SYSPWRGD does not go active within 1 second of asserting VPSYS.

D0 **Reserved**

Reserved bit. Default = 0.

Name Clock Control Register
Type Read/Write
Index DEH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
STP_EN	Reserved	Reserved	Reserved	Reserved	STP_ON_HRQ	STP_ON_AT	STP_ON_HLT

D7 **STP_EN**

Global stop clock enable. Default = 0.

0 = Disable STP_ON_HRQ, STP_ON_AT and STP_ON_HLT.
1 = Enables this register.

D[6:3] **Reserved**

Reserved bits. Default = 0.

D2 **STP_ON_HRQ**

Enable Stop Clock while HRQ active. Default = 0.

0 = The processor clock will not stop after releasing control of the bus to either memory refresh or the LCD controller.
1 = The processor clock will stop after releasing control of the bus to either memory refresh or the LCD controller. The processor clock will remain stopped until one of these devices attempts to return control of the bus back to the CPU.

D1 **STP_ON_AT**

Enable Stop Clock during expansion bus cycle. Default = 0.

0 = The processor clock will not stop after the start of an expansion bus cycle.
1 = The processor clock will stop after the start of an expansion bus cycle and will remain stopped until the internal Ready is activated.

D0 **STP_ON_HLT**

Enable Stop Clock during Halt cycle. Default = 0.

0 = The processor clock will not stop following a bus cycle which indicates HALT status.
1 = The processor clock will stop following a bus cycle which indicates HALT status. The processor clock will remain stopped until an interrupt, NMI, or hold request is issued.

Name SmartClock Activity Mask Register
Type Read/Write
Index DFH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
MSK_IORNG	MSK_VIDM	MSK_HD	MSK_IRQ	MSK_SIO	MSK_PCC	MSK_KBD	MSK_PIO

D7 **MSK_IORNG**

Programmable I/O range activity mask bit. Default = 1.

0 = I/O accesses within the address range specified by the PMU I/O Range Register will trigger SmartClock activity.
1 = I/O accesses within the address range specified by the PMU I/O Range Register will not trigger SmartClock activity.

D6 **MSK_VIDM**

Video memory activity mask bit. Default = 1.

0 = Memory writes to the VG330 display buffer mapped at B8000H - BFFFFH or A0000H - AFFFFH will trigger SmartClock activity, depending on video mode.
1 = Memory writes to the VG330 display buffer mapped at B8000H - BFFFFH or A0000H - AFFFFH will not trigger SmartClock activity, depending on video mode.

D5 **MSK_HD**

Hard disk activity mask bit. Default = 1.

0 = I/O accesses to the hard disk at addresses 1F0-1F7H and 3F6-3F7H will trigger SmartClock activity.
1 = I/O accesses to the hard disk at addresses 1F0-1F7H and 3F6-3F7H will not trigger SmartClock activity.

D4 **MSK_IRQ**

IRQ activity mask bit. Default = 0.

0 = Activity on IRQs, as defined by the PMU Activity Mask Register, will trigger SmartClock activity.
1 = Activity on IRQs, as defined by the PMU Activity Mask Register, will not trigger SmartClock activity.

D3 **MSK_SIO**

Serial port activity mask bit. Default = 1.

0 = I/O accesses to the serial port at addresses 2E8H - 2EFH, 2F8H - 2FFH, 3E8H - 3EFH, or 3F8H - 3FFH will trigger SmartClock activity.
1 = I/O accesses to the serial port at addresses 2E8H - 2EFH, 2F8H - 2FFH, 3E8H - 3EFH, or 3F8H - 3FFH will not trigger SmartClock activity.

D2 **MSK_PCC**

PC Card activity mask bit. Default = 1.

0 = I/O accesses to the registers of the internal PC Card controller or I/O or memory accesses to PC CARD cards will trigger SmartClock activity.
1 = I/O accesses to the registers of the internal PC Card controller or I/O or memory accesses to PC CARD cards will not trigger SmartClock activity.

D1 **MSK_KBD**

Keyboard activity mask bit. Default = 1.

0 = I/O accesses to the keyboard controller at address 060H will trigger SmartClock activity.
1 = I/O accesses to the keyboard controller at address 060H will not trigger SmartClock activity.

D0 **MSK_PIO**

Programmable chip select mask bit. Default = 1.

0 = Activity on a programmable chip select that was defined in the GPIO Registers will trigger SmartClock activity.
1 = Activity of a programmable chip select that was defined in the GPIO Registers will not trigger SmartClock activity.

Name SmartClock Inactive Step Register

Type Read/Write

Index E0H

Description Note that the SmartClock Control Register (Index E3H) sets the sampling period for the SmartClock.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
NACTSTP[7:0]							

D[7:0] **NACTSTP**

SmartClock Inactive Step bits. Default = 00.

These bits determine the step size. This value may be programmed to be either a positive or negative number. Supported values are -128 to +127, a 2’s complement value.

Name	SmartClock Active Step Register
Type	Read/Write
Index	E1H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACTSTP[7:0]							

D[7:0] **ACTSTP**

SmartClock Active Step bits. Default = 00.

These bits determine the value added to the current Activity Level count when activity has been detected in one sampling period. This value is a positive number and may be set to 0 to 255.

Name SmartClock Activity Level Register
Type Read/Write
Index E2H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
ACTLVL7	ACTLVL6	ACTLVL5	ACTLVL4	ACTLVL3	ACTLVL2	ACTLVL1	ACTLVL0

D[7:0] **ACTLVL[7:0]**

SmartClock Active Level bits. Default = FFH.

These bits reflect the activity level of the sources specified by the SmartClock Activity Mask register.

When the value of this register reaches 00H, a request will automatically be issued to slow or stop the processor clock. This request will remain active until the value in this register reaches FFH.

Once the value of this register reaches FFH, another request to slow or stop the clock will not be issued until the value returns to 00H.

Software may load any value into this register by first pausing the SmartClock sampling logic by clearing the SMTCLKEN bit of the SmartClock Control register to ‘0’, writing to this register, then re-enabling the SmartClock sampling logic by setting the SMTCLKEN bit back to ‘1’.

Name	SmartClock Control Register
Type	Read/Write
Index	E3H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
SMTCLKEN	Reserved	Reserved	Reserved	Reserved	ACTRES2	ACTRES1	ACTRES0

D7 **SMTCLKEN**

SmartClock enable bit. Default = 0

0 = Pauses the SmartClock so an APM driver may load a value into the Activity Level Register.
1 = Enable the SmartClock logic.

D[6:3] **Reserved.**

Reserved bits. Default = 0.

D[2:0] **ACTRES[2:0]**

SmartClock sampling rate select bits. These bits determine the activity sampling rate of the SmartClock logic as follows:

Bits [2:0]	Sampling Rate
000	61 µs (default)
001	122 µs
010	244 µs
011	488 µs
100	976 µs
101	1.95 ms
110	3.91 ms
111	7.81 ms

Name SUSPEND/REFRESH Control Register

Type Read/Write

Index E4H

Description This register allows setting the type of memory refresh behavior performed during the SUSPEND state.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
RFSHMD	RFSHMD	SLWREF	REFDONE	Reserved	Reserved	Reserved	Reserved

D[7:6] **RFSHMD[1:0]**

Suspend Refresh Mode. Default = 00.

RFSH MD1	RFSH MD0	Memory type	Suspend Refresh Behavior
0	0	SRAM	Suspend refresh disabled.
0	1	PSRAM	REFRSELB asserted then DREFRSELB asserted; RASB and DRASB remain negated.
1	0	Standard DRAM	REFRSELB asserted then DREFRSELB asserted; RASB and DRASB toggle. (Refresh rate controlled by D5, the SLWREF bit field)
1	1	Self-Refresh DRAM	REFRSELB asserted then DREFRSELB asserted; RASB asserted then DRASB asserted.

D5 **SLWREF**

Slow Refresh Enable. Default = 0.

0 = 15 µs Refresh Rate.
1 = 120 µs Refresh Rate.

D[4] **REFDONE**

Refresh Done. Default = 0.

This status flag indicates whether the CPU can access system RAM or whether access is not possible at this time because of access restrictions related to power management state transitions.

0 = PMU is providing RAM refresh cycles and CPU cannot access RAM at this time.
1 = MCU is providing control of memory refresh and CPU can access RAM at this time.

D[3:0] **Reserved**

Reserved bits. Default = 0.

Name BIOS Shadow RAM Address Register

Type Read/Write

Index E8H

Description This register allows the shadow RAM to be located anywhere within the 16 Mbyte RAM memory space.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SRA23	SRA22	SRA21	SRA20	SRA19	SRA18	SRA17	SRA16

D[7:0] **SRA[23:16]**

Starting physical RAM address for BIOS shadow. Default = 0FH.

These bits specify the physical address where the 64 Kbyte BIOS shadow RAM is to be located.

Name BIOS Shadow RAM and EMS Control Register

Type Read/Write

Index E9H

Description Bits D7 and D6 of this register are used to initialize and enable the BIOS shadow RAM. The BIOS first selects the RAM address to be used for shadowing the BIOS and initializes the BIOS Shadow RAM Address Register. The BIOS then write enables the shadow RAM and performs a Block-String-Move to itself to copy the BIOS image into the shadow RAM. Once this has been completed, the BIOS inhibits writes to the shadow RAM and sets the read enable bit SR_RE to ‘1’.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
SR_WE	SR_RE	Reserved	Reserved	Reserved	Reserved	ESEG_WP	DSEG_WP

D7 **SR_WE**

BIOS shadow RAM write enable. Default = 0.

0 = Memory writes to F0000H - FFFFFH are directed to the BIOS ROM.
1 = Memory writes to the BIOS ROM address at F0000H - FFFFFH are redirected to the shadow RAM addressed by bits D[7:0] of the BIOS Shadow RAM Address Register.

D6 **SR_RE**

BIOS shadow RAM read enable. Default = 0.

0 = Memory reads from F0000H - FFFFFH are directed to the BIOS ROM.
1 = Memory reads from the BIOS ROM address at F0000H - FFFFFH are redirected to the shadow RAM addressed by bits D[7:0] of the BIOS Shadow RAM Address Register.

D[5:2] **Reserved**

Reserved bits. Default = 0000

D1 **ESEG_WP**

E0000H memory segment write protect. Default = 0.

0 = Writes to memory addressed by the mapping registers for the D0000H - DFFFFH address range will be enabled.
1 = Writes to memory addressed by the mapping registers for the D0000H - DFFFFH address range will be inhibited.

D0 **DSEG_WP**

D0000H memory segment write protect. Default = 0.

0 = Writes to memory addressed by the mapping registers for the E0000H - EFFFFH address range will be enabled.
1 = Writes to memory addressed by the mapping registers for the E0000H - EFFFFH address range will be inhibited.

16.4.1 LCU Register Reference

This section provides details of the LCD Controller Unit registers.

The VG330 LCD controller supports CGA 640x200, AT&T 640x400, and VGA 640x480 monochrome graphics modes. It incorporates a subset of registers compatible with standard CGA and VGA monochrome graphics adapters.

LCU Registers

The LCD controller registers are located at the following CGA compatible I/O addresses:

Four of the LCU registers are located in the I/O addressing space. They are:

Register	Address
LCU Index Register	I/O Address 3D4H
LCU Data Register	I/O Address 3D5H
LCU Mode Select Register A	I/O Address 3D8H
LCU Mode Select Register B	I/O Address 3DEH

The remaining LCU registers exist within an LCU index space and are all accessed through the LCU Index Register at I/O Address 3D4H and the LCU Data Register at I/O Address 3D5H, as follows:

Register	Address
Display Start Address MSB Register	Index 0CH
Display Start Address LSB Register	Index 0DH
T1 Register	Index C6H
T2 Register	Index C7H
T3 Register	Index C8H
T4 Register	Index C9H
LCD Horizontal Resolution Register	Index CAH
LCD Vertical Resolution Register	Index CBH
LCD Mode Register	Index CCH

LCU Indexed Register Descriptions

Name	CGA Index Register
Type	Read/Write
I/O Address	3D4H
Description	This register is used to identify which of the indexed registers inside the LCU is to be accessed.
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INDXA_7	INDXA_6	INDXA_5	INDXA_4	INDXA_3	INDXA_2	INDXA_1	INDXA_0

D[7:0] **INDXA**

Indexed register address bits.

These bits are used to address one of the LCU's CGA indexed registers.

Name	CGA Data Register
Type	Read/Write
I/O Address	3D5H
Description	This register is used to read or write data from or to the indexed registers inside the LCU.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
INDXD_7	INDXD_6	INDXD_5	INDXD_4	INDXD_3	INDXD_2	INDXD_1	INDXD_0

D[7:0] **INDXD**

Indexed register data value.

These bits are used to move data into or out of one of the LCU's CGA indexed registers.

Name CGA Mode Select Register A

Type Read/Write

I/O Address 3D8H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	VIDE	Reserved	Reserved	Reserved

D[7:4] **Reserved**

Reserved bits. Clear to 0000.

D3 **VIDE**

Enable video. Default = 0.

Following a hard reset, this bit must be set to ‘1’ before the VG330 will power up the LCD.

D[2:0] **Reserved**

Reserved bits. Clear to 0000.

Name CGA Mode Select Register B
Type Read/Write
I/O Address 3DEH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	PAGSEL	Reserved	Reserved	GRES1

D[7:4] **Reserved**

Reserved bits. Clear to 0000.

D3 **PAGSEL**

Display buffer page select bit. Default = 0.

Valid only for CGA 640x200 graphics mode.

0 = Select graphics page at B8000H - BBFFFH for display.
1 = Select graphics page at BC000H - BFFFFH for display.

D[2:1] **Reserved**

Reserved bits. Clear to 0000.

D0 **GRES1**

400 line graphics mode select bit. Default = 0.

0 = Select CGA 640x200 graphics mode
1 = Select AT&T 640x400 graphics mode.

The following LCU registers are addressed through the CGA Index Register and read or written through the CGA Data Register.

Name Display Start Address MSB Register

Type Read/Write

LCU Index 0CH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	DSA14	DSA13	DSA12	DSA11	DSA10	DSA9	DSA8

D7 **Reserved**

Reserved bit. Clear to 0.

D[6:0] **DSA High**

Upper byte of display start address bits. Default value is 0000000.

Together with the bits of the Display Start Address LSB Register, these bits specify the starting address within the Display Buffer Area where the image to be displayed on the LCD panel resides.

Name Display Start Address LSB Register

Type Read/Write

LCU Index 0DH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
DSA7	DSA6	DSA5	DSA4	DSA3	Reserved	Reserved	Reserved

D[7:3] **DSA Low**

Lower byte of display start address bits. Default value is 00000.

Together with the bits of the Display Start Address MSB Register, these bits specify the starting address within the Display Buffer Area where the image to be displayed on the LCD panel resides.

D[2:0] **Reserved**

Reserved bits. Clear to 000.

Name LCD T1 Register
Type Read/Write
LCU Index C6H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
CLKPS2	CLKPS1	CLKPS0	T1D4	T1D3	T1D2	T1D1	T1D0

D[7:5] **CKLPS**

Pixel Clock Prescale divisor. Default = 0.

These bits specify the Pixel Clock Prescale divide factor applied to the divided oscillator clock to generate the internal pixel clock, PCLK. The following identifies values:

CLKPS2	CLKPS1	CLKPS0	Clock Prescale Divisor / PCLK Frequency
0	0	0	1/32 MHz (default) (assuming OSCDIV=00)
0	0	1	2 / 16 MHz
0	1	0	4 / 8 MHz
0	1	1	8 / 4 MHz
1	0	0	16 / 2 MHz
1	0	1	32 / 1 MHz
1	1	0	64 / 500 KHz
1	1	1	128 / 250 KHz

D[4:0] **T1D**

T1 period select. Default = 00000

The SHCLK period is specified as T1 + 1 PCLK periods. The minimum value is 2 PCLK periods. To get as close as possible to the desired frame rate, and to simplify meeting other timing specifications of the chosen LCD, it is best to use the highest PCLK frequency and the largest value of T1 that will produce the desired frame rate.

Name LCD T2 Register

Type Read/Write

LCU Index C7H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	LCDW1	LCDW0	T2D4	T2D3	T2D2	T2D1	T2D0

D7 **Reserved**

This bit is reserved for manufacturing test and must be cleared to ‘0’.

(Setting this bit to ‘1’ will cause unpredictable results)

D[6:5] **LCDW**

LCD Data bus width. Default = 00.

Used to set width of data bus to LCD from VG330.
These bits are decoded as follows:

LCDW1	LCDW0	LCD data width	Active LCD data pins
0	0	4 bits (default)	LCD[3:0]
0	1	2 bits	LCD[1:0]
1	0	1 bit	LCD[0]
1	1	Reserved setting.	Reserved

D[4:0] **T2D**

T2 SHCLK High timer select. Default = 00000.

The SHCLK high time is specified as T2 + 1 PCLK periods. T2D[4:0] must be set less than T1D[4:0].

Name LCD T3 Register
Type Read/Write
LCU Index C8H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	VGA	DBLSCAN	T3D4	T3D3	T3D2	T3D1	T3D0

D7 **Reserved**

Clear to 0.

D6 **VGA**

Enable VGA graphics mode. Default = 0.

0 = The video mode is 640x200, 640x400 double scan, or 640x400 AT&T high resolution graphics, and display memory is located at B8000H - BFFFFH.
1 = The video mode is similar to VGA mode 11H, 640x480 monochrome graphics, and display memory is located at A0000H - AFFFFH with identical memory map.

D5 **DBLSCAN**

Enable double scan. Default = 0.

0 = 640x200 graphics mode displays each line only once on the LCD.
1 = Each 640x200 graphics mode line is sent to the LCD twice to expand the 200 line image for 400 line panels.

D[4:0] **T3D**

T3 LOCLK select. Default = 00000.

LOCLK goes high T3 + 1 PCLK periods after SHCLK goes high.
T3D[4:0] cannot be greater than T1D[4:0].

Name LCD T4 Register

Type Read/Write

LCU Index C9H

Description This register adjusts LCD timing.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
LOCLKTYP1	LOCLKTYP0	T4AMODE	T4D4	T4D3	T4D2	T4D1	T4D0

D[7:6] **LOCLKTYP**

Set LOCLK Mode.

When these bits are cleared to ‘00’, SHCLK runs continuously. Otherwise, 4 SHCLK pulses are suppressed at the end of each line, and the rising edge of LOCLK can be delayed by a programmable number of SHCLK periods, plus the delay specified by the T3 register as shown below:

LOCLK TYP1	LOCLK TYP0	SHCLK / LOCLK Delay
0	0	Continuous: (T3 + 1) * PCLK
0	1	Suppress: 4: (T3 + 1) * PCLK
1	0	Suppress 4: ((T3 + 1) * PCLK) + SHCLK
1	1	Suppress 4: ((T3 + 1) * PCLK) + (2 * SHCLK)

D5 **T4AMODE**

Set T4A characteristics. Default = 0.

0 = LOCLK goes low in the same SHCLK period as it went high. See note for T4D below.
1 = One SHCLK period is added to the delay specified by T4D[4:0]. That is, for LOCLK type ‘00’, LOCLK goes low in the next SHCLK period; however, note that even when TA4MODE is set to ‘1’, the LOCLK pulse width is the same for all values of LOCLKTYP[1:0]).

D[4:0] **T4D**

T4 LOCLK High Timer Select. Default = 00000.

Depending on the setting for LOCLKTYP, LOCLK goes low T4 + 1 PCLK periods after SHCLK goes high, or would have gone high had it not been suppressed.

T4D[4:0] can not be greater than T1D[4:0].

If T4AMODE is cleared to a value of 0, T4D[4:0] must be greater than T3D[4:0].

Name	LCD Horizontal Resolution Register
Type	Read/Write
LCU Index	CAH
Description	This register sets the horizontal resolution of the display.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
LCDX7	LCDX6	LCDX5	LCDX4	LCDX3	LCDX2	LCDX1	LCDX0

D[7:0] **LCDX**

LCD Horizontal Resolution. Default = 00H (32 pixels)

The width of the LCD panel in pixels is defined as:
Width = 4 * (LCDX[7:0] + 1).

Maximum horizontal width is 640 pixels and minimum is 32 pixels.

Name LCD Vertical Resolution Register
Type Read/Write
LCU Index CBH
Description This register sets the vertical resolution of the display.
Bits

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LCDY7	LCDY6	LCDY5	LCDY4	LCDY3	LCDY2	LCDY1	LCDY0

D[7:0] **LCDY**

LCD Vertical Resolution. Default = 00H (2 pixels)

The height of the LCD panel (pixel lines) is defined as:
Height = 2 *(LCDY[7:0] + 1).

Maximum lines is 480 pixels. If either GRES1 or DBLSCAN is set to 1, the number of lines must be evenly divisible by 4.

Name LCD Mode Register
Type Read/Write
LCU Index CCH
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	SEQUP_EN	SEQDN_EN	DLY1	DLY0	CENTER	BLANK	RVVD

D7 **Reserved**

Reserved bit. Clear to 0.

D6 **SEQUP_EN**

LCD power up sequence enable bit. Default = 0.

0 = The VG330 will not sequence power and clocks/data to the LCD panel on a power up cycle.
1 = The VG330 sequences power and clocks/data to the LCD panel on a power up cycle. The sequencing delay is specified by bits D[4:3].

D5 **SEQDN_EN**

LCD power down sequence enable bit. Default = 0.

0 = The VG330 will not sequence power and clocks/data to the LCD panel on a power down cycle.
1 = The VG330 will sequence power and clocks/data to the LCD panel on a power down cycle. The sequencing delay is specified by bits D[4:3].

D[4:3] **DLY**

LCD power sequencing delay bits. Default = 00.

These bits determine the sequencing delay between VPLCD, LCD clocks and data, and VPBIAS on power up and power down cycles. LCD power up or power down sequencing is only performed when the associated sequence enable bit has been set to ‘1’.

DLY1	DLY0	LCD power sequence delay
0	0	7.5 ms (default)
0	1	15 ms
1	0	30 ms
1	1	60 ms

D2 **CENTER**

Enable centering. Default = 0.

0 = No centering
1 = If the video mode is set to 640x200 or 640x400 graphics modes, the display image will be centered for panels greater than 200 or 400 lines respectively.

D1 **BLANK**

Enable blanking. Default = 0.

0 = No blanking of unused lines.
1 = When this bit is set to ‘1’ and the video mode is set to 640x200 or 640x400 graphics modes, unused lines for panels greater than 200 or 400 lines will be blanked respectively.

D0 **RVVD**

Enable reverse video. Default = 0.

0 = No video inversion
1 = The data polarity of the display image is reversed.

16.4.2 PC Card Controller Register Reference

This section provides details of the PC Card Controller registers.

Two of the PC Card Controller registers are located in the I/O address space. They are:

Register	**Address**
PC Card Controller Index Register	I/O Address 3E0H
PC Card Controller Data Register	I/O Address 3E1H

All other PC Card controller registers listed in Table16-4 are accessed through PC Card Controller Data Register after being selected through the PC Card Controller Index register.

Table 16-4. PC Card Controller Register List

REGISTER	INDEX
Identification and Revision Register	00H
Interface Status Register	01H
Power and RESETDRV Control Register	02H
Interrupt and General Control Register	03H
Card Status Change Register	04H
Card Status Change Interrupt Configuration Register	05H
Address Window Enable Register	06H
I/O Control Register	07H
I/O Address 0 Start Low Byte Register	08H
I/O Address 0 Start High Byte Register	09H
I/O Address 0 Stop Low Byte Register	0AH
I/O Address 0 Stop High Byte Register	0BH
I/O Address 1 Start Low Byte Register	0CH
I/O Address 1 Start High Byte Register	0DH
I/O Address 1 Stop Low Byte Register	0EH
I/O Address 1 Stop High Byte Register	0FH
System Memory Address 0 Mapping Start Low Byte Register	10H
System Memory Address 0 Mapping Start High Byte Register	11H
System Memory Address 0 Mapping Stop Low Byte Register	12H
System Memory Address 0 Mapping Stop High Byte Register	13H
Card Memory Offset Address 0 Low Byte Register	14H
Card Memory Offset Address 0 High Byte Register	15H
Card Detect and General Control Register	16H
System Memory Address 1 Mapping Start Low Byte Register	18H
System Memory Address 1 Mapping Start High Byte Register	19H
System Memory Address 1 Mapping Stop Low Byte Register	1AH
System Memory Address 1 Mapping Stop High Byte Register	1BH
Card Memory Offset Address 1 Low Byte Register	1CH
Card Memory Offset Address 1 High Byte Register	1DH
Global Control Register	1EH
Card Voltage Sense Register	1FH
System Memory Address 2 Mapping Start Low Byte Register	20H

Table 16-4. PC Card Controller Register List

System Memory Address 2 Mapping Start High Byte Register	21H
System Memory Address 2 Mapping Stop Low Byte Register	22H
System Memory Address 2 Mapping Stop High Byte Register	23H
Card Memory Offset Address 2 Low Byte Register	24H
Card Memory Offset Address 2 High Byte Register	25H
System Memory Address 3 Mapping Start Low Byte Register	28H
System Memory Address 3 Mapping Start High Byte Register	29H
System Memory Address 3 Mapping Stop Low Byte Register	2AH
System Memory Address 3 Mapping Stop High Byte Register	2BH
Card Memory Offset Address 3 Low Byte Register	2CH
Card Memory Offset Address 3 High Byte Register	2DH
Card Voltage Sense Register	2FH
System Memory Address 4 Mapping Start Low Byte Register	30H
System Memory Address 4 Mapping Start High Byte Register	31H
System Memory Address 4 Mapping Stop Low Byte Register	32H
System Memory Address 4 Mapping Stop High Byte Register	33H
Card Memory Offset Address 4 Low Byte Register	34H
Card Memory Offset Address 4 High Byte Register	35H

Name Identification and Revision Register

Type Read only

PCU Index 00H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
IFTYP1	IFTYP0	Reserved	Reserved	REV3	REV2	REV1	REV0

D[7:6] **IFTYP1**

PCSC interface type bits. Default = 10.

These bits read back as “10” to indicate support for both memory and I/O cards.

D[5:4] **Reserved**

Reserved bits. These bits will be read back as zero.

D[3:0] **REV**

These bits identify the revision level. The revision code is 0011.

Name	Interface Status Register
Type	Read only
PCU Index	Base + 01H
Description	
Bits	

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	PWRON	RDY/$\overline{\text{BSY}}$	WP	CD2	CD1	BVD2	BVD1

D7 **Reserved**

Reserved bit. Default = 1.
This bit always returns a ‘1’ when read.

D6 **PWRON**

PC Card power status. Default = 0.
0 = Power to the socket is off (Vcc, Vpp1 and Vpp2 are all no connects).
1 = Power to the socket is on (Vpp1 and Vpp2 are set according to bit D1 of the Power Control Register at PC Card Register Index 02H.)

D5 **RDY/$\overline{\text{BSY}}$**

Ready/$\overline{\text{Busy}}$.
0 = PC Card is busy.
1 = PC Card is ready.

D4 **WP**

Memory Write Protect switch, signal input.
0 = PC Card write protect switch is off.
1 = PC Card write protect switch is on.

D[3:2] **CD[2:1]**

Card Detect. Default = 0.

Complement of the values of *CD[2:1] on the PC Card interface. Bit is set to ‘1’ if corresponding *CD is active, reset to ‘0’ if inactive.

D[1:0] **BVD[2:1]**

Battery Voltage Detect. Default = 0.

For I/O PC Cards, bit D0 indicates the current status of the $\overline{\text{STSCHG}}$ / $\overline{\text{RI}}$ signal from the PC Card. The following shows the values of BVD[2:1] signals for memory PC Cards

BVD2	**BVD1**	**Battery State**
0	0	Battery Dead
0	1	Warning
1	0	Battery Dead
1	1	Battery Good

Name Power and RESETDRV Control Register
Type Read/Write
PCU Index 02H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
OE	Reserved	Reserved	PWREN	Reserved	Reserved	VPPSEL	Reserved

D7 **OE**

Output enable. Default = 0.

If this bit is cleared to zero, the PC Card outputs from the VG330 are driven to a high impedance state and the $\overline{\text{ENABLE}}$ output is driven high.

Note: this bit should not be set until after this register has been written to set the PC Card Power Enable and power has settled.

D6 **Reserved**

Reserved. Default = 0.

D5 **Reserved**

Reserved. Always reads ‘1’.

D4 **PWREN**

PC Card Power Enable. Default = 0.

0 = Power to the socket is disabled (Vcc, Vpp1, and Vpp2 are all no connects).
1 = Voltage selected according to Card Voltage Select Register (2FH). The power to the socket is turned on when a card is inserted and off when removed.

D[3:2] **Reserved**

Reserved. Default = 00.

D1 **VPPSEL**

PC Card Vpp Power Control. Default = 0.

0 = Vpp = Vcc.
1 = Vpp = Programming Voltage.

D0 **Reserved**

Reserved. Default = 0.

Name	Interrupt and General Control Register
Type	Read/Write
PCU Index	03H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
RI_EN	CRDRST	CRDTYP	Reserved	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0

D7 **RI_EN**

Ring Indicate enable. Default = 0

0 = For I/O PC Cards, the *STSCHG/*RI signal from the I/O PC Card is used as the status change signal *STSCHG. The current status of the signal is then available to be read from the Interface Status Register and this signal can be configured as a source for the card status change interrupt.

1 = For I/O PC Cards, the *STSCHG/*RI signal from the I/O PC Card is used as a ring indicator signal and is OR'd to the Power Management Unit and may be used to cause a RESUME from SUSPEND.

For memory PC Cards, this bit has no function.

D6 **CRDRST**

PC Card Reset. Default = 0.

This is a software reset to the PC Card.

0 = Activates the RESET signal to the PC Card. The RESET signal will be active until this bit is set to '1'.
1 = Deactivates the RESET signal to the PC Card.

D5 **CRDTYP**

PC Card Type. Default = 0.

0 = Memory PC Card.
1 = I/O PC Card.

D4 **Reserved**

Reserved bit. Default = 0.

(continued)

D[3:0] **IRQSEL**

IRQ Level Selection (I/O Cards Only). Default = 0011.

IRQSEL[3:0]	IRQ
0000	IRQ not selected.
0001	Reserved.
0010	Reserved.
0011	IRQ3 Enabled.
0100	IRQ4 Enabled.
0101	IRQ5 Enabled.
0110	Reserved.
0111	IRQ7 Enabled.
1000	Reserved.
1001	IRQ9 Enabled.
1010	IRQ10 Enabled.
1011	IRQ11 Enabled.
1100	IRQ12 Enabled.
1101	Reserved.
1110	IRQ14 Enabled.
1111	IRQ15 Enabled.

Name Card Status Change Register

Type Read/Write

PCU Index 04H

Description

This register provides the source of the card status change interrupt. Each source can be enabled to generate this interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register. The bits in this register will read back as zero if their corresponding enable bits are reset to zero.

Note:1: If the Explicit Write Back bit is set to ‘1’ in the Global Control Register, the acknowledgment of sources for the card status change interrupt will be done by writing back ‘1’ to the appropriate bit in the Card Status Change Register that was read as a ‘1’. Once acknowledged, that particular bit in the Card Status Change Register will be read back as zero. The interrupt signal caused by the card status change, if enabled on a system IRQ line, will be active until all of the bits in this register are zero.

Note:2: If the Explicit Write Back bit is not set to ‘1’, the card status change interrupt, when enabled on an IRQ line, will remain active until this register is read. In this mode, reading this register resets to zero all status bits which had been set to ‘1’.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	CD_CHG	RDY_CHG	BAT_WARN	BAT_DEAD

D[7:4] **Reserved**

Reserved bits, always zero.

D3 **CD_CHG**

Card Detect Change. Default = 0.

0 = No change detected on either of $\overline{\text{CD}}$[2:1].
1 = A change has been detected on $\overline{\text{CD}}$[2:1].

D2 **RDY_CHG**

Ready Change. Default = 0.

0 = No change detected on RDY/$\overline{\text{BSY}}$, or I/O PC Card installed.
1 = A low to high change has been detected on RDY/$\overline{\text{BSY}}$ indicating that the memory PC Card is ready to accept a new data transfer.

D1 **BAT_WARN**

Battery Warning. Default = 0.

0 = No battery warning condition, or I/O PC Card installed.
1 = A battery warning condition has been detected.

D0 **BAT_DEAD**

Battery Dead / $\overline{\text{STSCHG}}$. Default = 0.

0 = For memory PC Cards, battery is good. For I/O PC Cards, the Ring Indicate Enable bit of the Interrupt and General Control Register is set to ‘1’, or $\overline{\text{STSCHG}}/\overline{\text{RI}}$ is high.
1 = For memory PC Cards, a battery dead condition has been detected. For I/O PC Cards, the Ring Indicate Enable bit of the Interrupt and General Control Register is reset to ‘0’ and the $\overline{\text{STSCHG}}/\overline{\text{RI}}$ signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of $\overline{\text{STSCHG.}}$

Name Card Status Change Interrupt Configuration Register
Type Read/Write
PCU Index 05H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
SIRQS3	SIRQS2	SIRQS1	SIRQS0	CD_EN	RDY_EN	BWARN_EN	BDEAD_EN

D[7:4] **SIRQ[3:0]**

Interrupt steering for the Card Status Change Interrupt. Default = 000.

These bits select the redirection of the card status change interrupt.

SIRQS[3:0]	IRQ
0000	IRQ not selected
0001	Reserved
0010	Reserved
0011	IRQ3 Enabled
0100	IRQ4 Enabled
0101	IRQ5 Enabled
0110	Reserved
0111	IRQ7 Enabled
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

D3 **CD_EN**

Card Detect Enable. Default = 0.

0 = Disables the generation of a card status change interrupt when the card detect signals change state.
1 = Enables a card status change interrupt when a change has been detected on the *CD1 or *CD2 signals.

D2 **RDY_EN**

Ready Enable. Default = 0.

0 = Disables the generation of a card status change interrupt when a low to high transition has been detected on the Ready/$\overline{\text{Busy}}$ signal.
1 = Enables a card status change interrupt when a low to high transition has been detected on the Ready/$\overline{\text{Busy}}$ signal.

D1 **BWARN_EN**

Battery Warning Enable (memory PC Cards only).

0 = Disables the generation of a card status change interrupt when a battery warning condition has been detected.
1 = Enables a card status change interrupt when a battery warning condition has been detected.

D0 **BDEAD_EN**

Battery Dead Enable /$\overline{\text{STSCHG}}$.

0 = Disables the generation of a card status change interrupt when either a battery dead condition (memory PC card) or an active $\overline{\text{STSCHG}}$ (I/O PC card) is detected.
1 = For memory PC Cards, enables a card status change interrupt when a battery dead condition has been detected. For I/O PC Cards, enables a card status change interrupt if the $\overline{\text{STSCHG}}$/$\overline{\text{RI}}$ signal has been pulled low by the I/O PC Card, assuming the Ring Indicate Enable bit of the Interrupt and General Control Register is cleared to ‘0’.

Name Address Window Enable Register
Type Read/Write
PCU Index 06H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
IOWEN1	IOWEN0	Reserved	MWEN4	MWEN3	MWEN2	MWEN1	MWEN0

D[7:6] **IOWEN[1:0]**

I/O Window Enables. Default = 00.

0 = Inhibit the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window.
1 = Generate the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card.

The start and stop register pairs must all be set to the desired window values before setting these bits to ‘1’.

D5 **Reserved**

Reserved bit.

D[4:0] **MWEN[4:0]**

Memory Window Enables. Default = 0 for all.

0 = Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding memory address window.
1 = Generate the card enable signals to the PC Card when a memory access occurs within the corresponding memory address window. When the system address is within the window, the computed address will be generated to the PC Card.

The start, stop, and offset register pairs must all be set to the desired window values before setting these bits to ‘1’.

Name I/O Control Register
Type Read/Write
PCU Index 07H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
IO1WT	Reserved	IO1_CS16MD	IO1DSZ	IO0WT	Reserved	IO0_CS16MD	IO0DSZ

D7 **IO1WT**

I/O Window 1 Wait State. Default = 0.

0 = 16-bit system accesses occur without additional wait state.
1 = 16-bit system accesses occur with 1 additional wait state.

D6 **Reserved**

Reserved bit.

D5 **IO1_CS16MD**

I/O Window 1 $\overline{\text{IOCS16}}$ Source. Default = 0.

0 = $\overline{\text{IOCS16}}$ is generated based on the value of the data size bit.
1 = $\overline{\text{IOCS16}}$ is generated based on the $\overline{\text{IOIS16}}$ signal returned from the PC Card.

D4 **IO1DSZ**

I/O Window 1 Data Size.Default = 0.

0 = 8-bit I/O data path.
1 = 16-bit I/O data path.

D3 **IO0WT**

I/O Window 0 Wait State.Default = 0.

0 = 16-bit system accesses occur without additional wait state.
1 = 16-bit system accesses occur with 1 additional wait state.

D2 **Reserved**

Reserved bit.

D1 **IO0_CS16MD**

I/O Window 0 $\overline{\text{IOCS16}}$ Source.Default = 0.

0 = $\overline{\text{IOCS16}}$ is generated based on the value of the data size bit.
1 = $\overline{\text{IOCS16}}$ is generated based on the $\overline{\text{IOIS16}}$ signal returned from the PC Card.

D0 **IO0DSZ**

I/O Window 0 Data Size.Default = 0.

0 = 8-bit I/O data path.
1 = 16-bit I/O data path.

Name I/O Address Start Low Byte Register
Type Read/Write
PCU Index Window 0 - 08H
Window 1 - 0CH
Description Low order address bits used to determine the start address of the corresponding I/O address window. This provides a minimum 1 byte window for the I/O address window.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
STARTAL7	STARTAL6	STARTAL5	STARTAL4	STARTAL3	STARTAL2	STARTAL1	STARTAL0

D[7:0] **STARTAL**

I/O Window Start Low Address A[7:0].

Default = 00.

Name I/O Address Start High Byte Register
Type Read/Write
PCU Index Window 0 - 09H
Window 1 - 0DH
Description High order address bits used to determine the start address of the corresponding I/O address window.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
STARTAH 15	STARTAH 14	STARTAH 13	STARTAH 12	STARTAH 11	STARTAH 10	STARTAH 9	STARTAH 8

D[7:0] **STARTAH**

I/O Window Start High Address A[15:8].

Default = 00.

Name	I/O Address Stop Low Byte Register
Type	Read/Write
PCU Index	Window 0 - 0AH Window 1 - 0EH
Description	Low order address bits used to determine the stop address of the corresponding I/O address window.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
STOPAL7	STOPAL6	STOPAL5	STOPAL4	STOPAL3	STOPAL2	STOPAL1	STOPAL0

D[7:0] **STOPAL**

I/O Window Stop Low Address A[7:0].

Default = 00.

Name	I/O Address Stop High Byte Register
Type	Read/Write
PCU Index	Window 0 - 0BH Window 1 - 0FH
Description	High order address bits used to determine the start address of the corresponding I/O address window.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
STOPAH 15	STOPAH 14	STOPAH 13	STOPAH 12	STOPAH 11	STOPAH 10	STOPAH 9	STOPAH 8

D[7:0] **STOPAH**

I/O Window Stop High Address A[15:8].

Default = 00.

Name	System Memory Address Mapping Start Low Byte Register
Type	Read/Write
PCU Index	Window 0 - 10H Window 1 - 18H Window 2 - 20H Window 3 - 28H Window 4 - 30H
Description	Low order address bits used to determine the start address of the corresponding memory address window.
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
MWSTARTA A7	MWSTARTA A6	MWSTARTA A5	MWSTARTA A4	MWSTARTA A3	MWSTARTA A2	MWSTARTA A1	MWSTARTA A0

D[7:0] **MWSTARTA**

Memory Window Start Address A[19:12]. This provides a minimum memory mapping window of 4 Kilobytes.

Default = 00.

Name PC Card Memory Data Width Register
Type Read/Write
PCU Index Window 0 - 11H
Window 1 - 19H
Window 2 - 21H
Window 3 - 29H
Window 4 - 31H
Description This register defines the PC Card memory data width.
Bits

D7	D6	D5	D4	D3	D2	D1	D0
DWIDTH	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

D7 **DWIDTH**

PC Card Memory Data Width. Default = 0.

0 = 8-bit memory data path.
1 = 16-bit memory data path.

D[6:0] **Reserved**

Reserved. Default = 0.

Name System Memory Address Mapping Stop Low Byte Register

Type Read/Write

PCU Index Window 0 - 12H
Window 1 - 1AH
Window 2 - 22H
Window 3 - 2AH
Window 4 - 32H

Description Low order address bits used to determine the start address of the corresponding memory address window.

Bits

D7	D6	D5	D4	D3	D2	D1	D0
MWSTOPA A19	**MWSTOPA A18**	**MWSTOPA A17**	**MWSTOPA A16**	**MWSTOPA A15**	**MWSTOPA A14**	**MWSTOPA A13**	**MWSTOPA A12**

D[7:0] **MWSTOPA**

Memory Window Stop Address A[19:12].

Default = 00.

Name PC Card Memory Wait State Selection Register

Type Read/Write

PCU Index Window 0 - 13H
Window 1 - 1BH
Window 2 - 23H
Window 3 - 2BH
Window 4 - 33H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
M16W1	M16W0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

D[7:0] **M16W[1:0]**

Wait State Select for 16-bit Memory Accesses. Default = 00.

These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the $\overline{\text{WAIT}}$ signal, wait states will be generated when the PC Card asserts the $\overline{\text{WAIT}}$ signal.

M16W1	M16W0	16-bit Memory Wait States
0	0	Standard 16-bit cycle.
0	1	1 additional wait state.
1	0	2 additional wait states.
1	1	3 additional wait states.

D[6:0] **Reserved**

Reserved bits. Default = 0.

Name	Card Memory Offset Address Low Byte Register
Type	Read/Write
PCU Index	Window 0 - 14H Window 1 - 1CH Window 2 - 24H Window 3 - 2CH Window 4 - 34H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
OFFSET A19	OFFSET A18	OFFSET A17	OFFSET A16	OFFSET A15	OFFSET A14	OFFSET A13	OFFSET A12

D[7:0] **OFFSETA[19:12]**

Low order address bits which are added to the system address bits A[19:12] to generate the memory address for the PC Card.

Default = 0.

Name Card Memory Offset Address High Byte Register

Type Read/Write

PCU Index Window 0 - 15H
Window 1 - 1DH
Window 2 - 25H
Window 3 - 2DH
Window 4 - 35H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
WP	REG	OFFSET A25	OFFSET A24	OFFSET A23	OFFSET A22	OFFSET A21	OFFSET A20

D7 **WP**

Write Protect. Default = 0.

0 = Write operations to the PC Card through the corresponding system memory window are allowed.
1 = Write operations to the PC Card through the corresponding system memory window are inhibited.

D6 **REG**

REG Active. Default = 0.

0 = Access to the system memory will result in common memory on the PC Card being accessed.
1 = Access to the system memory will result in attribute memory on the PC Card being accessed.

D[5:0] **OFFSETA[25:20]**

Card Memory Offset Address A[25:20]. Default = 0.

High order address bits which are added to the system address bits A[23:20] to generate the memory address for the PC Card.

Note: This is only meaningful when there is a carry from the card memory offset low order address bits.

Name Card Detect and General Control Register

Type Read/Write

PCU Index 16H

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	SWCDINT	CDRSMEN	Reserved	Reserved	CFGRSTEN	DLY16INH

D[7:6] **Reserved**

Reserved bits. Default = 00.

D5 **SWCDINT**

Software Card Detect Interrupt. Default = 0.

If the Card Detect Enable bit is set to ‘1’ in the Card Status Change Interrupt Configuration Register, then writing a ‘1’ to this bit will cause a card detect card status change interrupt for the associated slot. The functionality and acknowledgment of this software interrupt will work the same way as the hardware generated interrupt. This bit will always read back as a zero.

The functionality of the hardware card detect card status change interrupt will not be affected. If card detect card status change from the previous state occurs on the *CD1 and *CD2 inputs, a hardware card detect card status change interrupt will be generated.

If the Card Detect Enable bit is set to zero in the Card Status Change Interrupt Configuration Register, then writing a ‘1’ to this bit has no effect.

D4 **CDRSMEN**

Card Detect Resume Enable. Default = 0.

If this bit is set to ‘1’, then once a card detect change has been detected on the *CD1 and *CD2 inputs, the internal *RIO signal will go from high to low and the Card Detect Change bit in the Card Status Change Register will be set to ‘1’. The internal *RIO output will remain low until either a read or a write of ‘1’ to the Card Detect Change bit in the Card Status Change Register (acknowledge cycle), which will cause the Card Detect Change bit to be reset to zero and the internal *RIO signal to go from low to high. The Card Detect Enable bit must be set to ‘1’ in the Card Status Change Interrupt Configuration Register in order to generate the *RIO.

If the card status change is routed to any of the IRQ signals, the setting of this bit to ‘1’ will prevent IRQ from going active as a result of a hardware card detect status change. Once the resume software has detected a card detect status change interrupt from *RIO (by reading the Card Status Change Register), the software should initiate a software card detect change so the card detect change condition will generate an active interrupt on the IRQ signal.

D[3:2] **Reserved**

Reserved bits. Default = 00.

D1 **CFGRSTEN**

Configuration Reset Enable.Default = 0.

0 = Configuration reset disable.
1 = When this bit is set to ‘1’, and both the *CD1 and *CD2 inputs go high, a reset pulse will be generated to reset the configuration registers for the slot to their default state. The registers involved are all I/O registers, all memory registers, Interrupt and General Control Register, and Address Window Enable Register.

D0 **DLY16INH**

16-bit Memory Delay Inhibit. Default = 0.

0 = When this bit is cleared to zero, and a system memory window is set up to be 16 bits, by setting the Data Size bit in the System Memory Address Mapping Start High Byte Register to ‘1’, the falling edge of the control strobes *WE and *OE will be delayed synchronously by SYSCLK.
1 = The control strobes falling edge will not be synchronously delayed.

Name Global Control Register

Type Read/Write

PCU Index 1EH

Description

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	EXWRBK	Reserved	Reserved

D[7:3] **Reserved**

Reserved bits. Default = 00000

D2 **EXWRBK**

Explicit Write Back Card Status Change Acknowledge. Default = 0.

0 = When this bit is cleared to zero, the card status change interrupt is acknowledged by reading the Card Status Change Register, and the register bits are cleared upon a read.
1 = Setting this bit to ‘1’ will require an explicit write of a ‘1’ to the Card Status Change Register bit in order to reset the bit.

D[1:0] **Reserved**

Reserved bits.

Name	Card Voltage Sense Register
Type	Read only
PCU Index	1FH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$\overline{VS2}$	$\overline{VS1}$

D[7:2] **Reserved**

Reserved bits. Default = 0.

D1 **$\overline{VS2}$**

Voltage sense 2 from card.

D0 **$\overline{VS1}$**

Voltage sense 1 from card.

D1	D0	Voltage Selection
0	0	3.3v/X.Xv Capable
0	1	X.Xv Only
1	0	3.3v Capable
1	1	5v Only

Name	Card Voltage Select Register
Type	Read/Write
PCU Index	2FH
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VSEL1	VSEL0

D[7:2] **Reserved**

Reserved bits. Default = 0.

D[1:0] **VSEL[1:0]**

Voltage select. Default = 0.

These bits control the VCC value that will be applied to the card when the PC Card Power Enable bit in Register 02H is Set.

D1	D0	Voltage Selection	$\overline{\text{VCC5}}$ Pin	$\overline{\text{VCC3}}$ Pin
0	0	5v	0	1
0	1	3.3v	1	0
1	0	OFF	1	1
1	1	3.3v	1	0

17 System Design

17.1 Introduction

This chapter provides design information for engineers incorporating the VG330 into a system. The chapter describes how to calculate timing values needed when designing a particular configuration of LCD panel into a system.

17.1.1 LCD Timing Calculations

The VG330 allows a great deal of flexibility in specifying the timing for the LCD clock signals LOCLK (Load Clock) and SHCLK (Shift CLock). SHCLK shifts the data on to the LCD panel and LOCLK latches a line of data to LCD panel. For each line of data shifted on to the LCD panel, a LOCLK pulse is generated to latch that line of data onto the panel in use. In most of the data sheets for the LCD panels the LOCLK and SHCLK are referred as CL1 and CL2, respectively. Figure 17-1 shows how the signals SHCLK, LOCLK, and FRAME (Frame) are interfaced to the LCD panel. Figure 17-1 shows the signals generated from the LCD controller in the VG330 chip and how these signals are interfaced to the panel in use.

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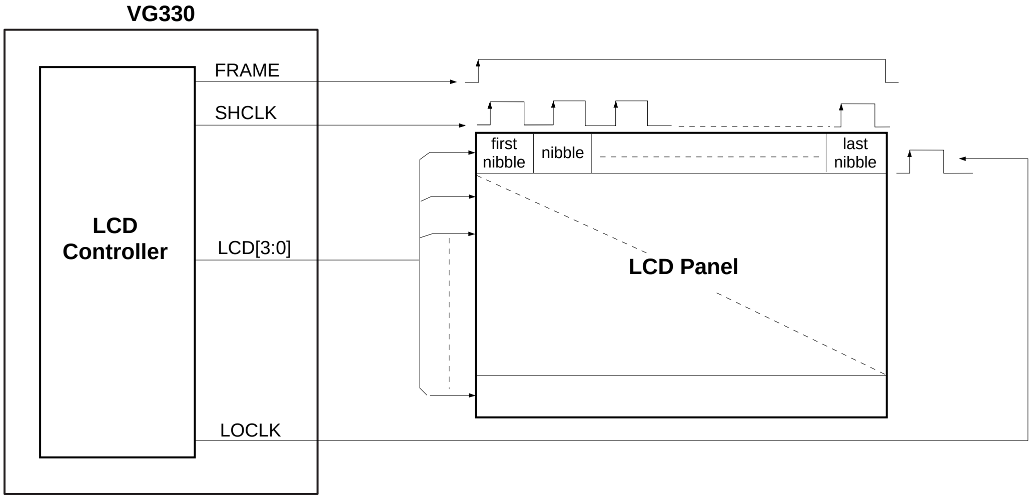


Figure 17-1 Signal Interface to LCD Panel

The SHCLK signal controls the rate at which data is shifted out to the Panel. Each SHCLK shifts one nibble out through the LCD[3:0] bus of the VG330 LCD controller. After enough data has been shifted to fill one line on the panel, the LCD Controller generates a LOCLK pulse to latch that data on the first line of the panel. Once the data has been latched, the LCD controller continues shifting the data out on the next line until the last line is reached. At this point, the LCD controller generates a FRAME signal, indicating the start of a new frame. FRAME remains high until the entire top line of the new frame is shifted out to the panel.

To understand programming of the registers for the VG330 LCD Controller, it is necessary to have a brief background of how various clocks are generated in the LCD controller. The LCD Controller has an internal divider that divides the maximum frequency CPU clock to generate a prescaled clock (PCLK). PCLK is used to generate the SHCLK and LOCLK timing signals to the LCD. The periods of the SHCLK and LOCLK signals are register programmable. The generation of the SHCLK and LOCLK signals can be best explained using a timing diagram. It is necessary to understand the definition of the LCD controller register bits T1[4:0], T2[4:0], T3[4:0] and T4[4:0] before going through the timing diagram.

Register Bits [4:0]

T1[4:0], T2[4:0], T3[4:0] and T4[4:0] correspond to the bits D[4:0] of the registers C6, C7, C8 and C9, respectively, which are accessed using the standard CGA index and data registers located at I/O addresses 3D4 and 3D5.

T1 [4:0]

T1[4:0] determines the period of the SHCLK in units of PCLK. The SHCLK period is defined as T1+1 PCLK periods. The minimum is 2 PCLK periods.

T2 [4:0]

T2[4:0] determines the high time of the SHCLK signal. The SHCLK signal high time is specified as (T2+1) PCLK periods. T2[4:0] must be set less than T1[4:0] for obvious reasons.

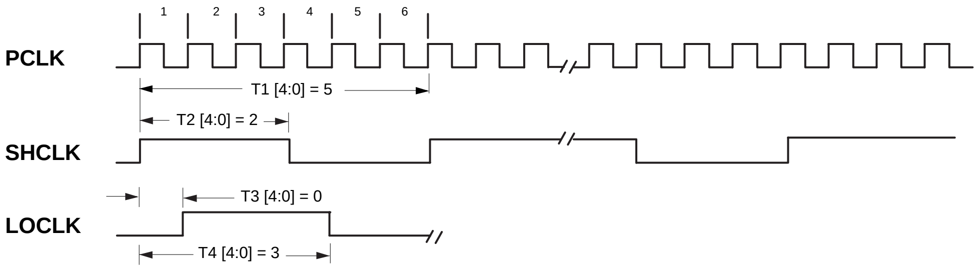
T3 [4:0]

T3[4:0] determines the delay between the rise of SHCLK and the rise of LOCLK. LOCLK goes high a delay of (T3+1) PCLK periods after SHCLK goes high.

T4 [4:0]

LOCLK goes low (T4+1) PCLK periods after SHCLK goes high, or would have gone high had it not been suppressed. T4[4:0] cannot be greater than T1[4:0].

Figure 17-2 shows the relationship between PCLK, SHCLK, and LOCLK for T1[4:0]=5, T2[4:0]=2, T3[4:0]=0, and T4[4:0]=3. It should be noted that one LOCLK pulse is generated for each line of data transferred on to the LCD.



330DXX01

Figure 17-2 Relationship of PCLK, SHCLK, and LOCLK

Deriving the Register Programming Values

This application note describes how to use the LCD data sheet timing information to derive the register programming values for the VG330. These are the steps you need to follow.

1. Evaluate LOCLKTYP[1:0]
2. Set T1[4:0]
3. Determine PCLK (Prescaled clock) Period.
4. Draw Desired Timing Diagram
5. Set T2[4:0]
6. Set T3[4:0]:
7. Set T4[4:0]:

Step 1—Evaluate LOCLKTYP[1:0]

The first step is to determine the bit settings D7 and D6 of the register C9, which are designated named LOCLKTYP[1:0] in the Registers section of this manual that describes the LCD Controller.

The C9 register is described below.

Name	LCD T4 Register
Type	Read/Write
PCU Index	C9H
Description	
Bits	

D7	D6	D5	D4	D3	D2	D1	D0
LOCLKTYP1	LOCLKTYP2	T4AMODE	T4D4	T4D3	T4D2	T4D1	T4D0

Examine the LCD data sheet timing diagram relationship between SHCLK and LOCLK.

a) If SHCLK must continue to run while LOCLK is generated, the LOCLKTYP[1:0] bits in the LCD C9 Register must be set to 00.

b) If SHCLK must stop in the low state for a period of time when LOCLK is generated, LOCLKTYP[1:0] must not both be 0.

Setting LOCLKTYP[1:0] to a nonzero value will stop SHCLK for 4 SHCLK periods at the end of each line. The value written into LOCLKTYP[1:0] controls the SHCLK to LOCLK delay. This will be discussed later—at this time, it is only necessary to determine whether LOCLKTYP[1:0] is zero or nonzero. If for some reason it is difficult to determine this now, make an assumption and proceed, and return to this section later to verify your choice.

Step 2—Set T1[4:0]

T1 [4:0] determines the period of SHCLK. As previously explained, SHCLK is the clock that shifts the data out to the LCD panel. The T1 [4:0] setting is determined by the register bit settings D[4:0] of the C6 register in the VG330. Remember the LCD controller registers are accessed through the standard CGA index and data registers 3D4 and 3D5.

The C6 register is described below.

Name LCD T1 Register
Type Read/Write
PCU Index C6H
Description
Bits

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CLKPS2	CLKPS1	CLKPS0	T1D4	T1D3	T1D2	T1D1	T1D0

The following paragraphs tell you how to determine the value of T1[4:0].

SHCLK is generated by dividing the maximum frequency CPU clock by a factor CLKDIV, which is determined using Equation 17-1.

$$CLKDIV = \frac{Xtal\ Freq \times LCD\ Data\ Bus\ Width}{Frame\ Rate \times (Columns + (LCT \times LCD\ Data\ Bus\ Width)) \times Rows}$$

Equation 17-1

In Equation 17-1, Xtal Freq is the maximum frequency CPU clock frequency and LCD data bus width is usually 4, but may be 2 or 1 for small panels. Frame Rate is the desired frame refresh frequency, Columns and Rows are the X and Y pixel dimensions of the LCD, and LCT is a constant equal to 0 if LOCLKTYP[1:0]=0, and is 4 if
LOCLKTYP[1:0] > 0.

After evaluating with Equation 17-1, you must round CLKDIV to the nearest integer that can be expressed, as shown in Equation 17-2.

$$CLKDIV = (2^N)xX$$
$$where\ 2 \le X \le 32$$

Equation 17-2

Rounding up increases the actual frame rate; rounding down decreases it.

There will often be a range of N and X values that satisfy Equation 17-2. Larger values of N minimize power consumption, but if X is too small, it may be difficult to meet other LCD timing specifications. Generally, N should be the largest value possible, such that X > 5. However, in later steps you may discover that your panel requires a larger value of X. If this is the case, you would have to repeat this process.

The integer value of CLKDIV is plugged back into Equation 17-1, which is then solved for the actual frame rate to verify that the actual frame rate is acceptable. If it is not, another nearby value of CLKDIV must be chosen and plugged back into Equation 17-1. When a satisfactory CLKDIV value has been found, the LCD T1 Register is then programmed such that CLKPS[2:0] = N and
T1[4:0] = X-1.

Two examples show how to determine the value of T1 [4:0].

In the first example, Xtal freq is 28.6 MHz, desired frame rate is 73 Hz, LOCLKTYP[1:0] is nonzero, LCD size is 640 x 480, and bus width is 4.

$$CLKDIV = \frac{28.6E6 \times 4}{73 \times (640 + 4 \times 4) \times 480} = 4.98$$

Equation 17-3

$$\text{Integer CLKDIV} = 5 = (2^0) \times 5, N = 0, X = 5$$
$$\text{actual frame rate 72.7 Hz}$$

Equation 17-4

$$CLKPS = [2:0] = 0, T1[4:0] = 5 - 1 = 4$$

Equation 17-5

In the second example, Xtal freq is 28.6 MHz, desired frame rate is 70 Hz, LOCLKTYP[1:0] is zero, LCD size is 240 x 128, and bus width is 4.

$$CLKDIV = \frac{28.6E6 \times 4}{70 \times 240 \times 128} = 53.1$$

Equation 17-6

$$\text{Integer CLKDIV} = 52 = (2^2) \times 13, N = 2, X = 13$$
$$\text{actual frame rate 71.6 Hz}$$

Equation 17-7

$$CLKPS = [2:0] = 2, T1[4:0] = 13 - 1 = 12$$

Equation 17-8

Step 3—Determine PCLK (Prescaled Clock) Period.

PCLK is an internal signal in the LCD controller. The SHCLK and LOCLK timing relationships are programmed in steps of one PCLK period. The PCLK period is calculated as shown in Equation 17-9.

$$PCLKperiod = \frac{2^{CLKPS[2:0]}}{Xtal\ freq}$$

Equation 17-9

Step 4—Draw Desired Timing Diagram

On a sheet of graph paper, draw a timing diagram showing the VG330 SHCLK and LOCLK outputs as you would like them to be. The diagram must be drawn according to the following rules, which assure that the VG330 can generate the desired timing. Of course, the timing must also satisfy the requirements of the LCD.

Rule 1—Each horizontal grid unit is equal to one PCLK period.

Rule 2—SHCLK and LOCLK edges must occur on horizontal grid units, not between them.

Rule 3—The period of SHCLK in horizontal grid units must be equal to the value of X from Equation 17-2. A SHCLK period is defined to begin and end on a rising edge.

Rule 4—LOCLK must go low in either of the two following SHCLK periods:

a) the same SHCLK period in which it went high

b) in the next SHCLK period after it went high.

Rule 5—SHCLK must either be:

a) continuous, or

b) continuous during each line, but suppressed for 4 SHCLK periods at the end of each line. That is, the SHCLK waveform will appear to be a continuous waveform with 4 pulses missing at the end of each line.

Rule 6—If SHCLK is suppressed, LOCLK can go high during one of the three following SHCLK periods:

a) the last SHCLK of the line

b) the first suppressed SHCLK period

c) the second suppressed SHCLK period

Rule 7—The rise or fall of LOCLK cannot be coincident with a rise of SHCLK or a suppressed SHCLK.

Step 5—Set T2[4:0]

The T2 [4:0] bits determine the high time of the SHCLK signal in units of PCLK. As explained earlier, whenever the PCLK count equals T2[4:0], SHCLK is clocked low. The T2 [4:0] setting is determined by the D[4:0] register bit settings of the C7 register in the VG330.

The C7 register is described below.

Name	LCD T2 Register
Type	Read/Write
PCU Index	C7H
Description	

Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	LCDW1	LCDW0	T2D4	T2D3	T2D2	T2D1	T2D0

Count the number of horizontal time units when SHCLK is high from step 4. Set T2[4:0] equal to this value, minus 1. Set the LCDW[1:0] bits (bits D[6:5] of the register C7 in the LCD controller), which stand for “LCD data bus Width”, equal to 00 for 4 bits wide, 01 for 2 bits wide and 10 for 1 bit wide, respectively.

Step 6—Set T3[4:0

The T3 [4:0] bits determine the delay between the rise of LOCLK to the rise of SHCLK in units of PCLK. The T3 [4:0] setting is determined by the D[4:0] register bit settings of the C8 register in the VG330. LOCLK goes high T3+1 PCLK periods after SHCLK goes high.

The C8 register is described below.

Name LCD T3 Register
Type Read/Write
PCU Index C8H
Description
Bits

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	VIDMODE	DBLSCAN	T3D4	T3D3	T3D2	T3D1	T3D0

Count the number of horizontal time units from the nearest preceding rise of SHCLK to the rise of LOCLK. If the timing relationship conforms to rule 6b or 6c, measure this time from the point where the nearest preceding SHCLK would have risen if it had not been suppressed. Set T3[4:0] equal to this value, minus 1.

Step 7—Set T4[4:0]

The T4[4:0] bits determine the delay between the fall of LOCLK to the rise of SHCLK. The T4 [4:0] setting is determined by the D[4:0] register bit settings of the C9 register in the VG330. LOCLK goes low T4+1 PCLK periods after SHCLK goes high.

The C9 register is described below.

Name LCD T4 Register
Type Read/Write
PCU Index C9H
Description Bits

D7	D6	D5	D4	D3	D2	D1	D0
LOCLKTYP1	LOCLKTYP2	T4AMODE	T4D4	T4D3	T4D2	T4D1	T4D0

Count the number of horizontal time units from the nearest preceding rise of SHCLK to the fall of LOCLK. If the timing relationship conforms to rule 6b or 6c, measure this time from the point where the nearest preceding SHCLK would have risen if it had not been suppressed. Set T4[4:0] equal to this value, minus 1.

If LOCLK conforms to rule 4a, program T4AMODE to 0. If LOCLK conforms to rule 4b, program T4AMODE to 1.

If SHCLK conforms to rule 4a, program
LOCLKTYP[1:0]=00. If LOCLK conforms to rule 6a, program LOCLKTYP[1:0]=01. If LOCLK conforms to rule 6b, program LOCLKTYP[1:0]=10. If LOCLK conforms to rule 6c, program LOCLKTYP[1:0]=11.

17.1.2 LCD Timing Specifications

The next subsections contain timing specifications for the following LCD panels:

- Sanyo LCM-5540-22NAK (640x480 Single Panel)
- Optrex DMF-50404 (480x320 1/320 duty cycle)
- Optrex DMF-50081 (320x240 1/240 duty cycle)

Sanyo LCM-5540-22NAK (640x480 Single Panel)

The Sanyo LCM-5540-22NAK has the following timing parameters:

1. LOCLKTYP[1:0] = 0
   T4 [7:6] = 0
2. CLKDIV = 286000000*4/(73* (640+4*4)*480) = 4.98
   N = 0, X = 5
3. T1 [7:5] = 0
   T1 [4:0] = 4
4. PCLK = 1/286000000 = 35 ns
5. T2 [6:5] = 0 (4 bits LCD data width)
   T2 [4:0] = 1
   T2 [7] = Reserved
6. T3 [4:0] = 0
   T3 [5] = Don’t care for VGA
   T3 [6] = 1
7. T4 [4:0] = 3
   T4 [5] = 0
   T4 [7:6] = 1

Figure 17-3 shows the timing parameters of the Sanyo LCM-5540-22NAK 640x 480 LCD panel.

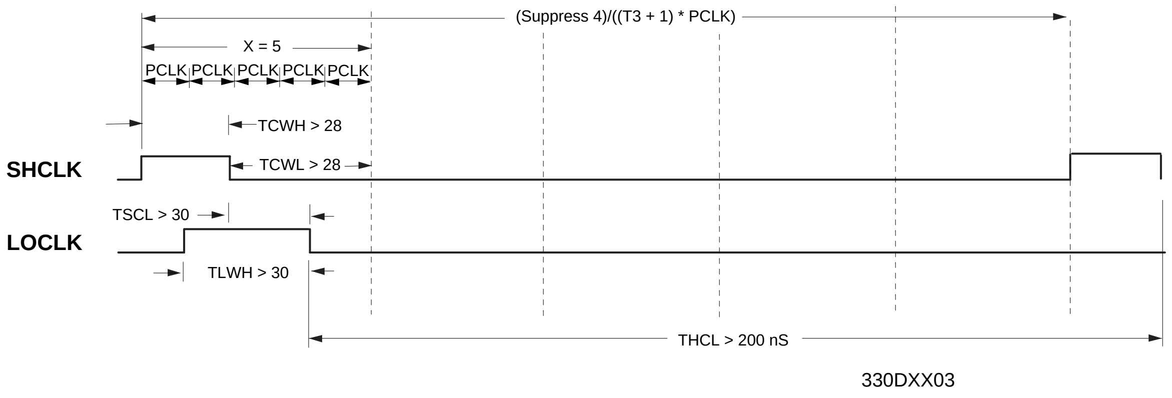


Figure 17-3 Sanyo LCM-5540-22NAK Timing

Table 17-1 gives the LCD register contents.

Table 17-1. LCD Register Contents

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1	0	0	0	0	0	1	0	0
T2	X	0	0	0	0	0	0	1
T3	X	1	0	0	0	0	0	0
T4	0	1	0	0	0	0	1	1

Horizontal Resolution Register = 640/4 - 1 = 159

Vertical Resolution Register = 480/2 - 1 = 239

Optrex DMF-50404 (480x320 1/320 Duty Drive)

The Optrex DMF-50404 has the following timing parameters:

1. LOCLKTYP[1:0] = 0
   T4 [7:6] = 0

2. Timing from Optrex spec: T = 0.0446 ms
   (1/T) / 320 = 70 Hz
   CLKDIV = 32000000 * 4 / (70*480*320) = 11.9 = 2^N * X
   (N = 0, X = 12) and (N = 1, X = 6) both satisfy the equation

   T1 [7:5] = 1 (CLKPS [2:0])
   T1 [4:0] = 5

3. PCLK = $2^{(CLKPS[2:0])}$ / 32000000 = 2 / 32000000 = 62 ns
4. T2 [6:5] = 0 (4 bits LCD data width)
   T2 [4:0] = Count the number of horizontal time units SHCLK is high - 1 = 3 - 1 = 2
   T2 [7] = Reserved
5. T3 [4:0] = Count the number of horizontal time units from preceding rise of SHCLK to the rise of LOCLK - 1 = 0
6. T3 [5]= Don’t care for VGA
   T3 [6]= VGA Enable Bit = 1
7. T4 [4:0] = Count the number of horizontal time units from preceding rise of SHCLK to the fall of LOCLK = 4
8. T4 [5]= 0
   If LOCLK goes low in the same SHCLK period in which it went high, set T4AMODE = 0
   If LOCLK goes low in the next SHCLK period after it went high, set T4AMODE = 1
9. T4 [7:6]= 0 LOCLKTYP [1:0] = 0 if continuous

Figure 17-4 shows the timing parameters of the Optrex DMF-50404 480x320 LCD panel.

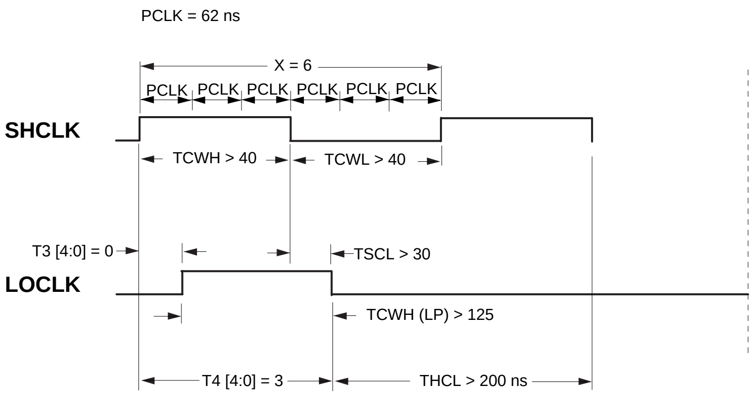


Figure 17-4 Optrex DMF-50404 Timing

Table 17-2 gives the LCD register contents.

Table 17-2. LCD Register Contents

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1	0	0	1	0	0	1	0	1
T2	X	0	0	0	0	0	1	0
T3	X	1	0	0	0	0	0	0
T4	0	0	0	0	0	1	0	0

Horizontal Resolution Register = 480/4 - 1 = 119

Vertical Resolution Register = 320/2 - 1 = 159

Optrex DMF-50081 (320x240 1/240 Duty Drive)

The Optrex DMF-50081 has the following timing parameters:

1. LOCLKTYP[1:0] = 0
   T4 [7:6] = 0

2. Timing from Optrex spec: T = 0.0595 ms
   1/T*240) = 70.02 Hz
   CLKDIV = 32000000 * 4 / (70*320*240) = 23.8 = 2^N * X
   (N = 0, X = 24), (N = 1, X = 6), and (N = 2, X = 6) all satisfy the equation

   T1 [7:5] = 2 (CLKPS [2:0])
   T1 [4:0] = 5

3. PCLK = $2^{(CLKPS[2:0])}$ / 32000000 = 4 / 32000000 = 125 ns

4. T2 [6:5] = 0 (4 bits LCD data width)

T2 [4:0] = Count the number of horizontal time units SHCLK is high - 1 = 3 - 1 = 2
T2 [7] = Reserved

5. T3 [4:0] = See Figure 17-5 below. Count the number of horizontal time units from preceding rise of SHCLK to the rise of LOCLK, then subtract 1.
There are two possibilities, 2 and 1. Either one will work—so either 1 or 0 will work here.

6. T3 [5]= Don’t care for VGA

T3 [6]= VGA Enable Bit = 1

7. T4 [4:0] = Count the number of horizontal time units from preceding rise of SHCLK to the fall of LOCLK = 4

8. T4 [5]= 0
If LOCLK goes low in the same SHCLK period in which it went high, set T4AMODE = 0
If LOCLK goes low in the next SHCLK period after it went high, set T4AMODE = 1

9. T4 [7:6]= 0 LOCLKTYP [1:0] = 0 if continuous

Figure 17-4 shows the timing parameters of the Optrex DMF-50081 320x240 LCD panel.

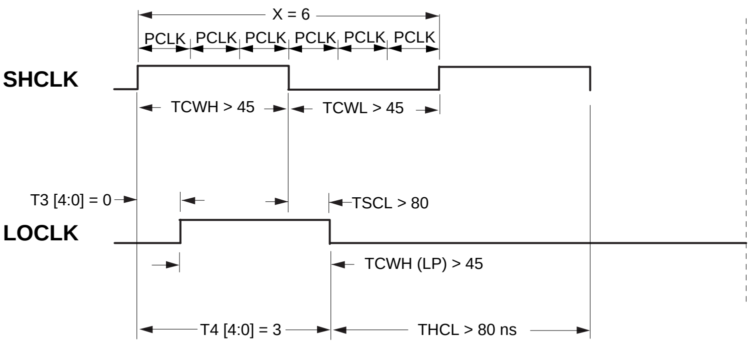


Figure 17-5 Optrex DMF-50081 Timing

Table 17-3 gives the LCD register contents.

Table 17-3. LCD Register Contents

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1	0	1	0	0	0	1	0	1
T2	X	0	0	0	0	0	1	0
T3	X	1	0	0	0	0	0	0
T4	0	0	0	0	0	1	0	0

Horizontal Resolution Register = 480/4 - 1 = 119

Vertical Resolution Register = 320/2 - 1 = 159

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